

Layout Design of LC VCO with Current Mirror Using 0.18 μm Technology

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ABSTRACT

This paper presents a new design of complementary oxide semiconductor voltage controlled oscillator (CMOS VCO) for improve tuning range and phase noise with low power consumption. Design is area efficient and easy to implement. Design is carried out in cadence and schematic editor using 180 nm technology. Simulation is done and performance results are reported. Results have been compared with earlier published work and improvements are obtained in this work.

Keywords: VCO, LC-Tank, Low Phase Noise, Low Power Consumption, Tuning Range, Spiral Inductor

1. Introduction

Today is increasing demand for wireless and multimedia applications keeps pushing the CMOS integrated wireless systems to support much communication standards (WLAN, GSM, UWB and DVB etc) [1]. As gigahertz-band communication is becoming more mature, the realization of a single chip transceiver becomes more demanding, with the need for lower cost, reduced size and less power consumption. As for the local oscillator signal generated from the integrated frequency synthesizer, the transceivers matched these standards need excellent phase noise performance and wide tuning range solving the frequency offset due to the variations of process, temperature and voltage [2]. So, CMOS voltage-controlled oscillator (VCO) will be challenging RF block. Especially, the higher close in phase noise due to higher $1/f$ noise in CMOS continues to be a challenge. As per demand for multi-band and multi-standard radios requires VCO's operating over a wider frequency range. Wireless standards specify the minimum level of the received signal, the maximum level of noise, the channel bandwidth, and the spacing between adjacent channels. Therefore, the maximum amount of acceptable phase noise on the oscillator can be calculated using the required signal to noise ratio after down conversion [3,4]. This paper presents a novel VCO architecture that can achieve low phase noise, low power consumption and enlarged tuning range. The low phase noise and enlarged tuning range are accomplished by adding capacitors

which is forming frequency tuning network.

2. Circuit Design and Implementation

Even though cross-coupled VCO's are widely used due to ease of implementation, the maximum noise generation instant coincides with maximum phase noise sensitivity, so this configurations do not use full potential of the LC tank. However in the balanced configuration, many components are required to produce a balanced circuit, so it consumes much current. Therefore, a new topology is demonstrated here, where both cross-coupled and balanced configurations produce better VCO characteristics. Furthermore, the a double cross-coupled circuit was built by combining these topologies which guarantees a rapid oscillation start up plus a reduction in unnecessary components. This simultaneously helps to reduce the chip size. It also has reduced noise up-conversion properties. In many published papers, a complementary oscillator circuit is the result of combining both PMOS and NMOS cross-coupled pairs in parallel to generate negative resistance. In the proposed VCO design we add the top current control architecture is employed to reduce the system power consumption and phase noise. VCO architecture will employ two current mirrors. Which balance the impedance in both the arm of the circuit and hence the current become the exact replica of the bias current. Because in case of a single current mirror the impedance is unbalanced resulting in different currents in the mirror arms which will improve the power

consumption and also has a negative effect on the phase noise performance of the circuit. In this design, current control mechanism reduce even harmonics in the drain current which as a direct impact on the noise component in the drain current which result reduction in phase noise [5,6]. The proposed design schematic view of VCO is presented in **Figure 1**.

This design achieves the negative devices by drawing minimum amount of current from the supply and reducing the total power consumption by the circuit while satisfying all the phase noise requirements of most communication standards. Here, novel current controlled architecture is used to shift the wave form and control shape of the output waveform by adjusting the transistor sizes for the current mirror. The phase noise is mainly determined by the quality value of tank higher the Q factor of the inductor, the closer it approaches the behavior of an ideal, lossless, inductor. The Q factor of an inductor can be found through the following formula [7,8]:

$$Q = \frac{W_0 L}{R} \tag{1}$$

The oscillation frequency of oscillator is given by:

$$F_{osc} = \frac{1}{2\pi\sqrt{LC}} \tag{2}$$

where L is the inductance of LC -tank and C is the capacitance.

Phase noise is most important parameter in VCO design therefore; phase noise performance is optimized by using lessons' formula given by Equation (3) [3,5].

$$L(f_m) = 10 \log \left\{ \frac{FKT}{2P_{avs}} \left[1 + \frac{f_c}{f_m} + \left(\frac{f_0^2}{2f_m Q_t} \right)^2 \left(1 + \frac{f_c}{f_m} \right) \right] \right\} \tag{3}$$

where $L(f_m)$ is the phase noise in dBc/Hz. Q_t is the loaded Q of the circuit, f_m is the frequency from the carrier, f_c is the flicker noise corner frequency, f_0 is the carrier (oscillator) frequency, T is the temperature in Kelvin, P_{avs} is the power through the resonator, F is the noise factor of the active device, K is the Boltzmann constant. An important concern in the design of VCOs' is the variation of the output phase and frequency as a result of noise on the control line. For a given noise in the output frequency is proportional to K_{vco} because of Equation (4) [9].

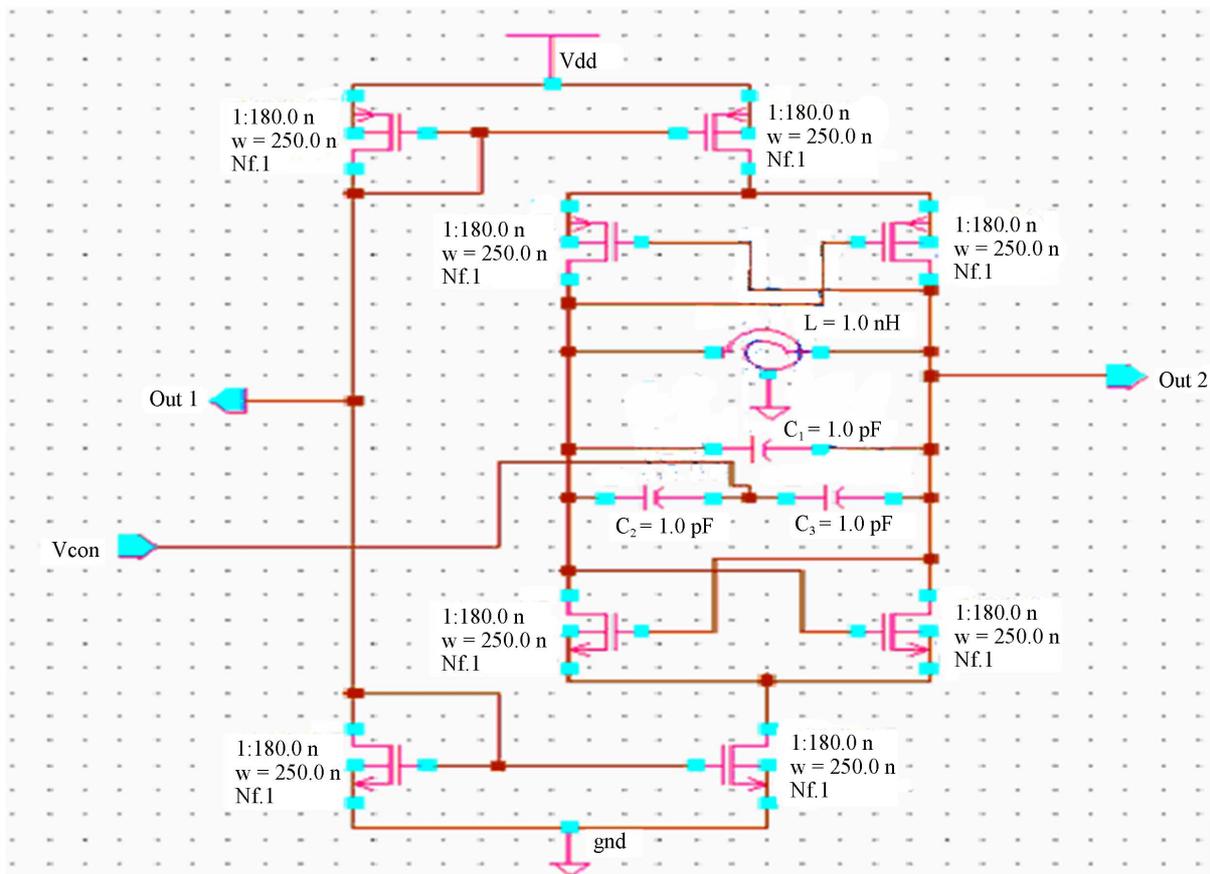


Figure 1. Schematic view of the present VCO design with current mirror.

$$W_{out} = W_0 + K_{VCO} \cdot V_{cont} \tag{4}$$

where, W_0 is the intercept at $V_{cont} = 0$, K_{VCO} is the gain or sensitivity of the circuit, and W_{out} is output.

$$\text{Maximum d.c power dissipation} = V_{supply} \times I_{bias} \tag{5}$$

A figure of Merit is a quantity used to characterize the performance of a VCO relative to other VCOs' of the same type. The power, phase noise, frequency of oscillation, offset from carrier tradeoffs all are taken in the FOM value [3]:

$$FOM = L(\Delta\omega) - 20 \log\left(\frac{\omega_0}{\Delta\omega}\right) + 10 \log\left(\frac{P_{diss}}{1mW}\right) \tag{6}$$

where, ω_0 is the oscillation frequency, $\Delta\omega$ is the offset from the carrier, $L(\Delta\omega)$ is the phase noise at the speci-

fied offset, P_{diss} is the DC power consumed by the VCO core. The Simple figure of merit (FOM) to examine various performances can be expressed as [10]:

$$FOM (dBF) = 20 \log(\text{freq}) - \text{phase noise} - 10 \log(\text{power}) \tag{7}$$

3. Simulation Results and Discussion

This work is carried out under the environment of cadence software and schematic editor (icfb &) is used for design entry, by using UMC 0.18 μm technology. In this design we have applied 2V as a supply at the center frequency of 3.3 GHz. Simulation have been done and obtained values are: the band width of 1.625 GHz, phase noise of -155.78 dBc/Hz @ 1MHz and -156.89 dBc/Hz @ 100 MHz and phase margin of 180° given in **Table 1**. Simulated output voltage responses of this design are presented in **Figure 2**. Phase noise is given in **Figure 3**,

Table 1. Results of VCO design.

Parameters	Reference [2]	Reference [11]	This design	
			General VCO (Without current mirror)	Proposed VCO (With current mirror)
Operating Voltage	2.5 V	3 V	2 V	2 V
Technology (CMOS)	0.5 μm	0.18 μm (TSMC)	0.18 μm (UMC)	0.18 μm (UMC)
Power consumption	15.5mW	15	12.72 mW	7.40 mW
Operating Frequency	0.661 - 1.27 GHz	2 GHz	3.3 GHz	3.3 GHz
Tuning Range	63%	10%	29.8%	4.024%
Phase Noise (dBc/Hz)	-106 @ 600 KHz	-131.9 @ 1 MHz	63.7 @ 1 MHz	-155.78 @ 1 MHz -156.89 @ 100 MHz
Bandwidth (GHz)	-	-	1.611	1.625
FOM (dBF)	-	-	141	367
Phase margin	-	-	180	180

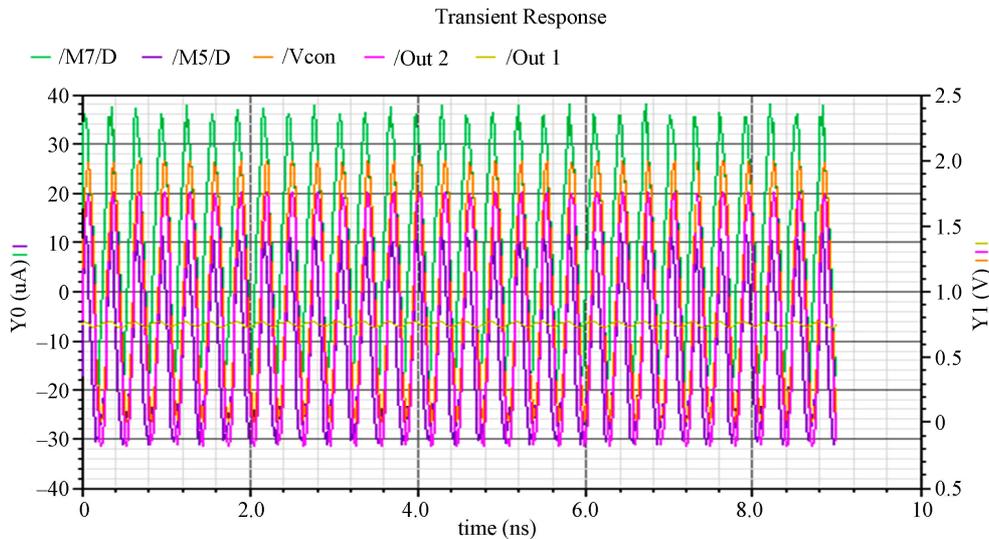


Figure 2. Simulation response of the output voltage.

with the power consumption of 7.40 mW at supply voltage of 2V and FOM is 367 dBf, **Figure 4** gives the graphical representation of frequency vs voltage. Finally we have designed the layout of the VCO and it is shown in **Figure 5**. Simulation results are verified with earlier published work as given in **Table 1**.

4. Conclusions

This design has improved the performance parameters of

the VCO. The realization of a single chip transceiver becomes more demanding, with the need for lower cost, reduced size and less power consumption. The VCO is implemented in cadence environment using 180 nm UMC technology. The design is simulated with different architecture *i.e.* without current mirror, and with current mirror, improvements are obtained in performance parameters *i.e.* power consumption is reduced by 2.78% - 5.3%. This paper focused on reasonable phase noise and

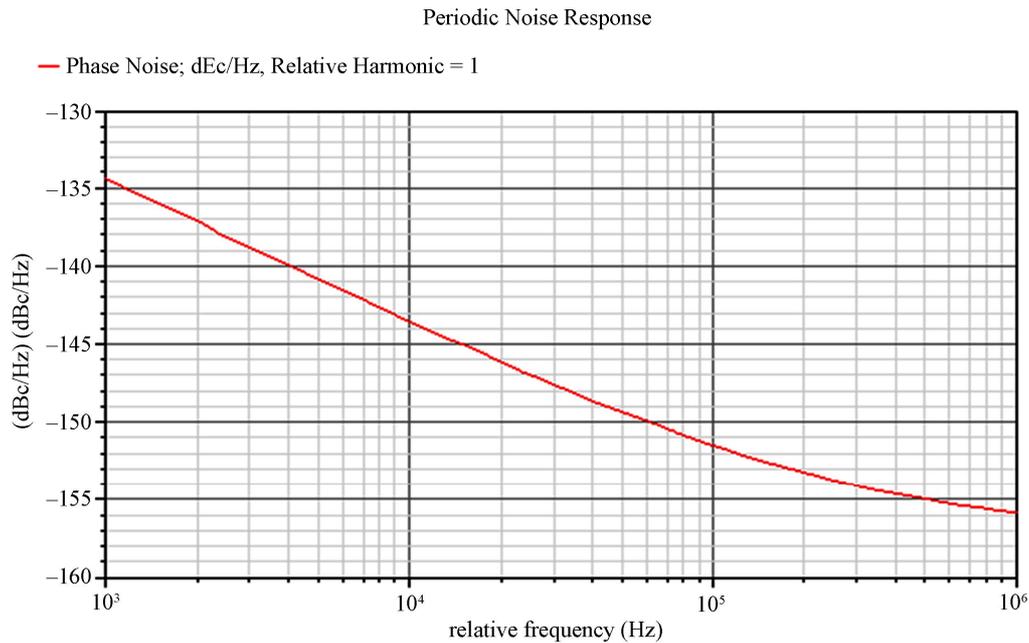


Figure 3. Simulation results of the phase noise @ 1 MHz.

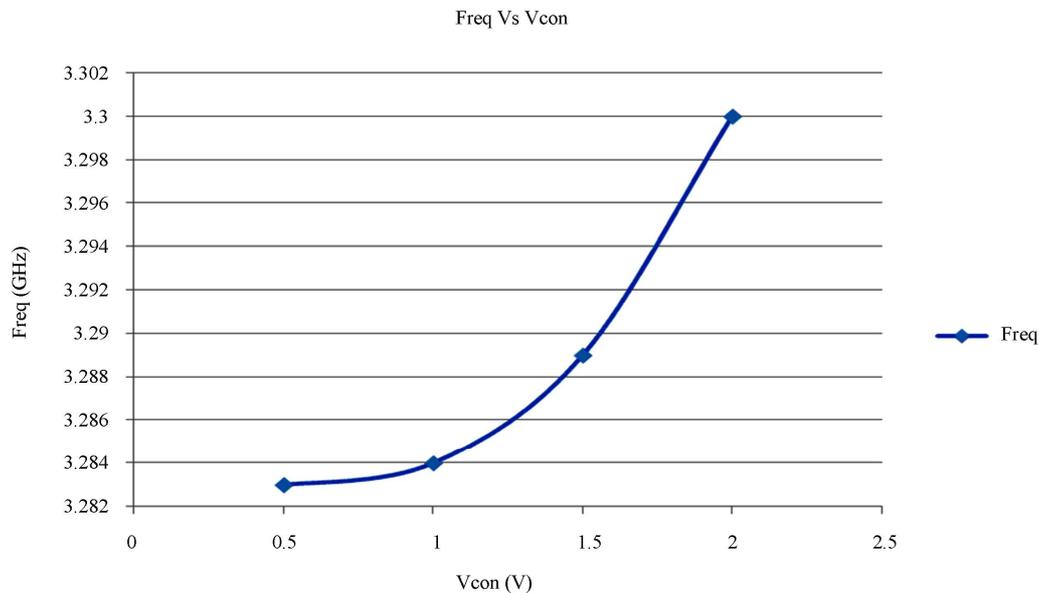


Figure 4. Graphical representation of Freq vs Vcon.

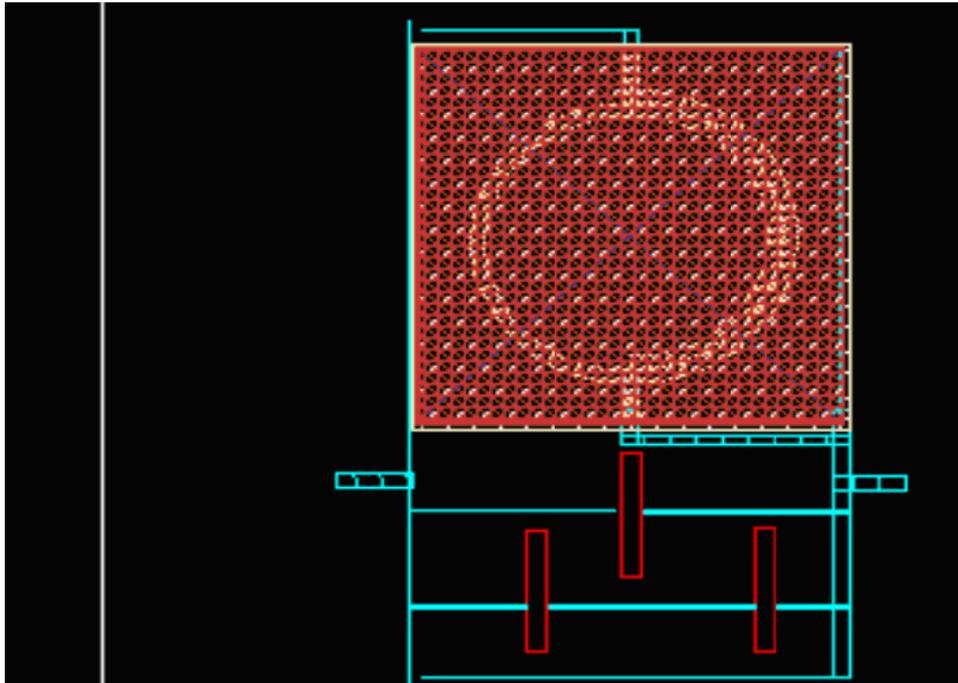


Figure 5. Layout design of VCO using current mirror.

tuning performance at the oscillation frequency of 3.3 GHz. Comparison of works are given in **Table 1** with earlier published work and improvements are observed.

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