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A New Zero-Voltage-Switching Push-Pull Converter

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ABSTRACT

A soft switching three-transistor push-pull（TTPP）converter is proposed in this paper. The 3rd transistor is inserted in the primary side of a traditional push-pull converter. Two primitive transistors can achieve zero-voltage-switching (ZVS) easily under a wide load range, the 3rd transistor can also realize zero-voltage-switching assisted by leakage inductance. The rated voltage of the 3rd transistor is half of that of the main transistors. The operation theory is explained in detail. The soft-switching realization conditions are derived. An 800 W with 83.3 kHz switching frequency prototype has been built. The experimental result is provided to verify the analysis.

Keywords: Push Pull Converter; Extra Transistor; Zero-voltage-switching

1. Introduction

The soft-switching technology can reduce device stress, switching loss, electromagnetic interference (EMI) and improve power density of the power electronic equipment. Over the last two decades, the most researches focus on the improved ZVS and ZVZCS phase-shifted full-bridge circuit [1-6] and their applications. But comparatively, the research on soft switching push-pull converter is very seldom. Taking LLC resonant technique for example, in recent years, LLC resonant converter based on half-bridge circuit, three- level circuit, full-bridge circuit and interleaved combined circuit [7-12] attracted lots of interest, owing to its full soft-switching realization for all power transistors and rectifier diodes. But in LLC resonant converters' family, the push-pull converter is exceptive. A push-pull converter has two transformer primary windings, which is impossible to have a LLC link inserted in the primary side. Converter in [13] shows soft switching behavior of the push-pull circuit with a LC resonant link in secondary side. But further research in [14] shows that there exists N-period resonant status in this type of the push-pull converter and its output will work as either constant voltage source or constant current source. Similarly, LCL resonant push-pull converter [15-17] where resonant components are located in either primary side or secondary side can also realize ZVS of power switches, but can not adjust its output voltage. Furthermore, the LCL resonant push-pull converter [18] with an additional parallel resonant inductor L_{sr} can realize ZVS for power switches and can adjust its output voltage by frequency modulation. But in order to improve boost ratio, the additional parallel resonant inductor L_{sr} has to be designed so small that extra power loss is become larger. Besides the above passive soft-switching push-pull converter, Active-clamped push-pull circuit in [19] can achieve ZVS for its main power switches, but its drawbacks are that the maximum duty cycle of main power switches is limited by active-clamped circuit. The three-level push-pull circuit [20] controlled by phase-shifted PWM mode can obtain ZVS condition for power switches, but its controller UC3875 is expensive. Both these two active soft-switching push-pull converters require four power switches and their driving logics is complex.

This paper proposes a three-transistor push-pull (TTPP) converter. ZVS can be achieved for all three transistors based on the proposed driving logic. The TTPP converter can be controller by a general PWM IC of SG3525.

2. Operation Principle

2.1. Converter Topology

The proposed TTPP converter is showed in **Figure 1**. An extra transistor Q_3 is inserted between the power source U_{in} and midpoint of two primary windings. Diodes D_1, D_2 and D_3 are body diodes of the transistors Q_1, Q_2 and Q_3 respectively. Capacitors C_1, C_2 and C_3 include the parasitic capacitor of power transistors and external parallel capacitors. The inductance $L_{leak\text{-}1}$ and $L_{leak\text{-}2}$ represent the leakage inductances of the primary winding P_1 and P_2 respectively.

2.2. PWM Mode

The PWM signals of the three power transistors are

showed in **Figure 2**. The duty cycle of the Q_1 and Q_2 are higher than 0.5, and they are 180º out of phase. The switching frequency of Q_3 is twice of that of Q_1 and Q_2.

1 and 0 represent switch on and switch off respectively. Neglecting the dead time, such as t_1~t_2, t_3~t_4, the operating status of the Q_1, Q_2 and Q_3 can be divided into four states, 101→110→011→110 in a complete cycle. To ensure voltage-second balance of the transformer in a switching cycle, the state 101 is lasts as long as the state 011.

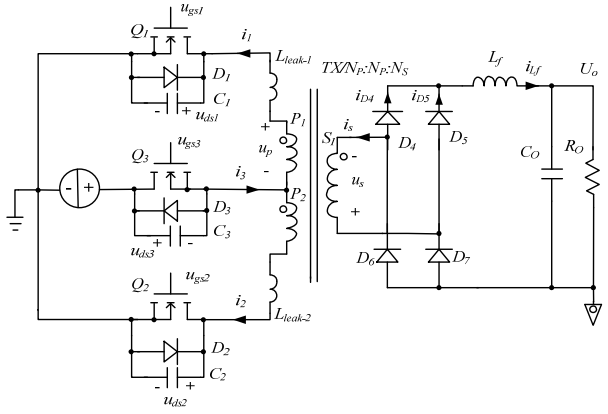


Figure 1. The proposed converter.

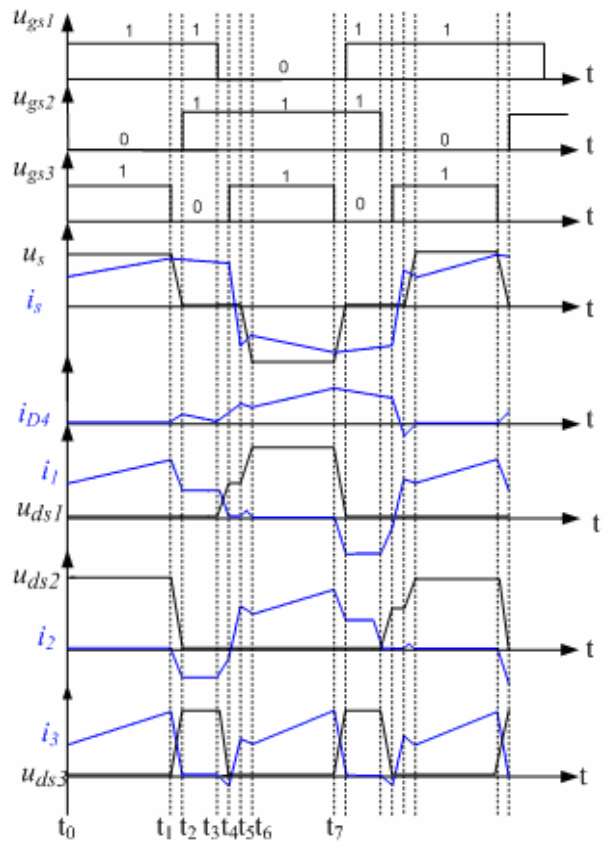


Figure 2. Main operation waveforms.

The state 101 and 011 are normal energy deliver stages from the primary side to the secondary side. Conversely, during state 110, the transistor Q_1 & Q_2 are both conducted and the energy is circulating in the primary side loop.

2.3. Operation Principle

To simplify the analysis of operation stage, the following conditions are assumed.

1) The voltage drop of the power MOSFETS and DIODES during on state is zero.

2) $C_1 = C_2 = C_3 = C_{leak}$.

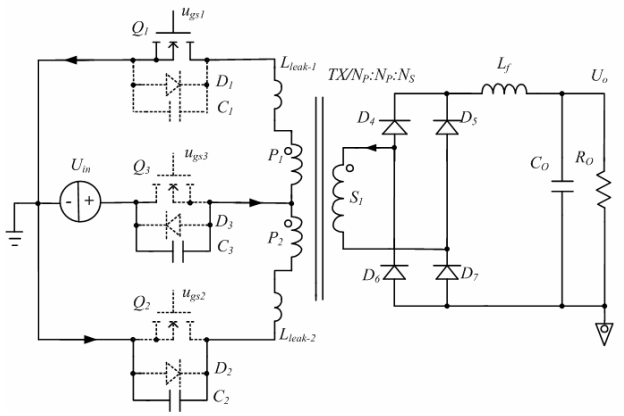
3) $L_{leak\text{-}1} = L_{leak\text{-}2} = L_{leak}$.

4) The output filter inductance can be modeled as a constant current source during the dead time.

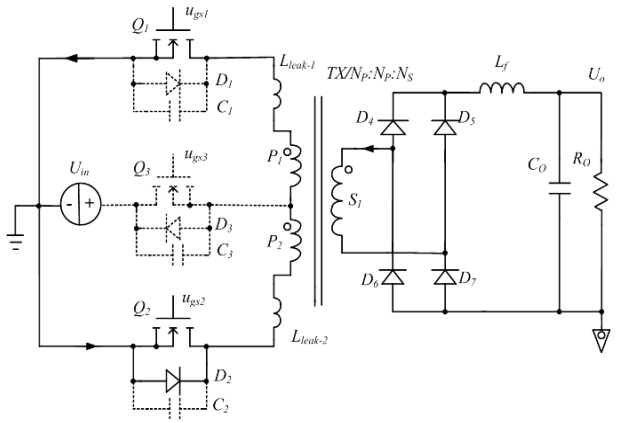
The operation process of the TTPP converter in half of cycle can be divided into six stages. The main operation waveforms are shown in **Figure 2**. **Figure 3** shows the equivalent circuit at different modes.

1) Mode 1 [t_1-t_2].

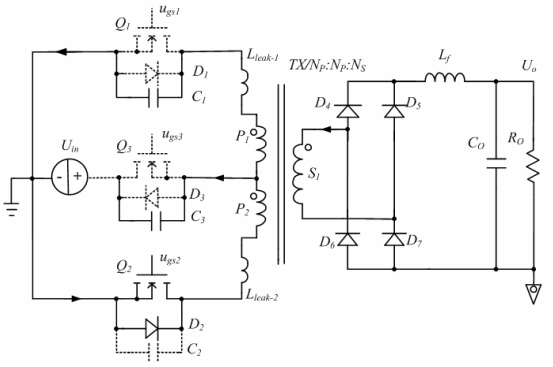
Before t_1, transistor Q_1 and Q_3 are both conducting, the energy transfer from U_{in} to the transformer secondary winding and the current of the filter inductance L_f increases. At t_1, Q_3 is turned off. If the capacitor C_3 is large



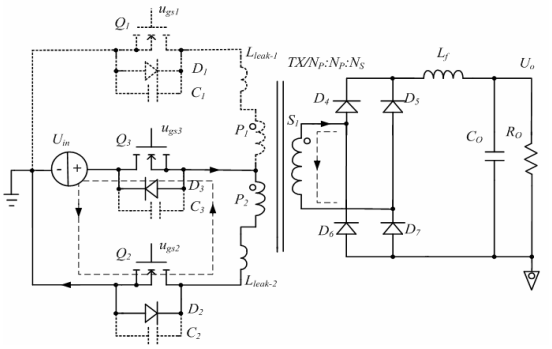
(a) [t_1-t_2]



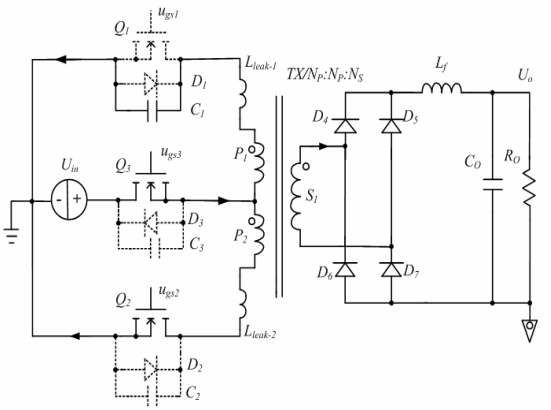
(b) [t_2-t_3]



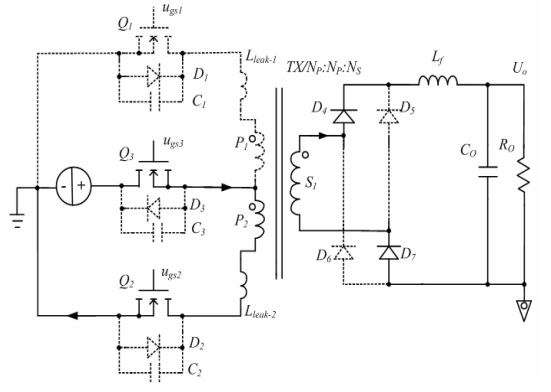
(c) [t_3-t_4]



(d) [t_4-t_5]



(e) [t_5-t_6]



(f) [t_6-t_7]

Figure 3. Equivalent circuit at different modes.

enough, the rising time of u_{ds3} is more than several time of falling time of i_{ds3}, Q_3 can achieve zero-voltage turn-off. In this mode, the inductance L_f will keep free-wheeling and be reflected to the primary side to resonant with capacitance C_3 and C_2. Because current through L_f is high enough, the voltage u_{ds3} will rise from zero up to U_{in} with u_{ds2} falling from $2U_{in}$ to zero. At the same time, the transformer primary side voltage u_P reduces to zero.

Assuming that the initial current of primary side loop in this mode is equal to I_p, the loop voltage equation and junction current equation in primary side can be established as

$$\begin{cases} U_{in} - u_{ds3} - u_p - L_{leak}\dfrac{di_1}{dt} = 0 \\ U_{in} - u_{ds3} + u_p - u_{ds2} - L_{leak}\dfrac{di_2}{dt} = 0 \\ I_p = i_1 - i_2 \\ i_3 = i_1 + i_2 \\ i_2 = C \cdot du_{ds2} / dt \\ i_3 = C \cdot du_{ds3} / dt \end{cases} \tag{1}$$

Right before t_2, transformer voltage u_p falls to zero. Combining this end condition with equation (1), the end status of this mode can be derived with approximation as in Equation (2),

$$\begin{cases} u_{ds2} = 0 \\ u_{ds3} = U_{in} \\ i_1 = I_P / 2 \\ i_2 = -I_P / 2 \\ t_2 - t_1 = 5CU_{in} / I_P \end{cases} \tag{2}$$

Meanwhile, in the secondary side, in general opinion, D_5&D_6 keep conducting and D_4&D_7 keep turn off. But in practical, because the transformer voltage fall down to zero quickly, the parasitic capacitor of the secondary side of the transformer will produce a discharge current i_{dis} which will cancel part of the current of the secondary side and reduce the current through D_5&D_6. So D_4&D_7 also conduct in order to keep the current of L_f constant. In this micro-commutation mode, the current of D_4&D_7 is so small that it neglected in most papers. In this paper, it is defined as micro-commutation mode.

2) Mode 2 [t_2-t_3].

At t_2 moment, the diode D_2 begins to conduct because u_{ds2} fall down to zero. This means that transistor Q_2 can achieve zero-voltage turn-on.

In this mode, D_2 and Q_1 are on and current circulates in the primary side. Neglecting the voltage-drop of D_2 and Q_1, the circulating current in the primary side maintain at $I_p/2$.

In the secondary side, L_f sustains negative voltage $-U_o$

and i_{Lf} begin dropping. This will drive the currents of D_4~D_7 reducing. It can be derived as:

$$\begin{cases} i_S = \dfrac{N_P}{N_S} \cdot I_P \\ i_{D4} + i_{D7} = i_{Lf} \\ i_S + i_{D7} = i_{D4} \\ i_{Lf} = i_{Lf}(t_2) - \dfrac{U_O \cdot dt}{L_f} \end{cases} \tag{3}$$

As a result, i_{D4} may fall down to zero.

3) Mode 3 [t_3-t_4]

At t_3, Q_1 is turned off. Q_1 can achieve zero voltage turn off due to C_1. The current i_1 flows through Q_1 decreasing rapidly, causing the secondary rectifier begin commutating. The current i_{D5}&i_{D6} decreases quickly and synchronously, i_{D4}&i_{D7} increase quickly. In the primary side, the leakage inductances of $L_{leak\text{-}1}$&$L_{leak\text{-}2}$ resonate with the capacitances of C_1&C_3. The voltage u_{ds1} increases while u_{ds3} falls down at the same time. The secondary current reflects the change of primary resonance current.

In this mode, the following equations can be derived,

$$\begin{cases} i_3 = i_1 + i_2 \\ i_1 = C\dfrac{du_{ds1}}{dt} \\ i_3 = C\dfrac{du_{ds3}}{dt} \\ U_{in} - u_{ds3} = L_{leak}\dfrac{di_1}{dt} + u_{ds1} \\ U_{in} - u_{ds3} = L_{leak}\dfrac{di_2}{dt} \end{cases} \tag{4}$$

when the energy of leakage inductance is large enough, u_{ds1} increases from zero to U_{in}, u_{ds3} decreases from U_{in} to zero , i_1 drops to zero, i_2 drops to equal i_3, and D_3 starts to conduct. As a result, it provides the Q_3 ZVS condition.

The time required for voltage u_{ds3} dropping to zero or voltage u_{ds1} to rise from zero to U_{in} can be simplified as

$$t_{34} = \frac{2CU_{in}}{i_1(t_3)/2} \tag{5}$$

4) mode 4 [t_4-t_5]

At t_4, the voltage u_{ds3} is zero, Q_3 is turned on and zero-voltage turn-on is achieved. In this interval, the voltage U_{in} applies on the leakage inductance $L_{leak\text{-}2}$. The current i_2 and i_3 can be expressed as,

$$i_2 = i_3 = i(t_4) + \frac{U_{in} \cdot dt}{L_{leak}} \tag{6}$$

with the change of i_2 and i_3, the secondary rectifier continues commutating. The current i_{D5}&i_{D6} decreases quickly and synchronously, i_{D4}&i_{D7} increase quickly. At the end of this stage, the currents i_{D5}&i_{D6} reach their peak reverse recovery current, accordingly the current i_2&i_3 change from negative across zero, until its value reflected to the secondary side reach the sum of i_{D4} and peak reverse recovery current i_{D5}.

5) Mode 5 [t_5-t_6]

At t_4, diode D_5&D_6 begin sustain reverse voltage quickly, leading the voltage of secondary winding begins be reverse quickly. As a result, the voltage of primary windings P_1 is also reversed with the secondary voltage. The magnetizing inductance L_m resonants with C_1. Voltage u_{ds1} rises from U_{in} to $2U_{in}$, u_p rises from zero to U_{in}.

In this mode, with the decreasing of reverse recovery current of D_5&D_6 , the current i_s, i_2 and i_3 also decrease synchronously. This mode finishes when i_{D5}&i_{D6} recovery to zero and u_p arrives U_{in}.

6) Mode 6[t_6-t_7]

In this mode, the converter run in a normal operation status and energy is transferred from input to output. The current of L_f increases linearly and the value can be expressed as follows,

$$i_{Lf} = i_{Lf}(t_5) + \frac{\left(U_{in} \cdot N_s / N_p - U_o\right) \cdot dt}{L_f} \tag{7}$$

At t_7, Q_3 is turned off; the converter begins the next half of cycle.

3. Design Guidelines

3.1. Duty Cycle Loss

According to the above analysis, the duty cycle α_3 of extra transistor Q_3 determines the ratio between U_o and U_{in}. But during t_5 to t_6, there is a duty cycle loss α_{loss}. It is derived approximately as,

$$\alpha_{loss} = \frac{t_{56}}{T_s} = \frac{i_3(t_6)}{L_{leak}T_s} \tag{8}$$

where T_s represents the switching period of Q_3. Then

$$\frac{U_O}{U_{in}} = (\alpha_3 - \alpha_{loss}) \cdot \frac{N_S}{N_P} \tag{9}$$

3.2. Voltage Stress of Power Switches

The voltage stress of main transistors Q_1&Q_2 is $2U_{in}$, while that of the extra transistor Q_3 is U_{in}.

3.3. Soft-switching Condition

A) Main transistors Q_1&Q_2

The ZVS condition of Q_1 and Q_2 is determined by L_f energy. In mode 1, u_{ds3} should rise from zero to U_{in} and u_{ds2} should fall from $2U_{in}$ to zero. So the condition of main transistor realizing soft-switching can be derived as

$$L_f I_{Lf}^2 > 5CU_{in}^2 \tag{10}$$

According to (14), the minimum load for obtain ZVS of Q_1 and Q_2 can be derived, as well as the minimum dead time t_1~t_2.

In addition, the turn-off loss of main transistor Q_1&Q_2 are far less than that in the traditional push-pull converter. In the traditional push-pull converter, the power switches are turned off at the peak current with a big turn-off losses. However, Q_1&Q_2 in this TTPP converter are turned off at half of peak current as that of traditional push-pull converter. Furthermore, the parallel capacitor of Q_1&Q_2 can reduce turn-off losses greatly.

B) Extra transistor Q_3

The ZVS condition of the extra transistor Q_3 is determined by the energy of leakage inductance. It can be expressed as,

$$L_{Leak} i^2(t_3) > 2CU_{in}^2 \tag{11}$$

Obviously, the ZVS of Q_3 couldn't be obtained easily under a light load or with small leakage inductance. In fact, adding a series inductance will be a recommended method to improve ZVS condition of Q_3.

4. Experimental Results

The performance of the TTPP converter has been verified with a prototype circuit operating at 83.3 kHz, 140 V~150 V input voltage, 180V output voltage and 800W power. The transformer is implemented with an EE42 core and windings with turn ratio of 24:24:42. Power MOSFETs of SPW20N60C3 and diodes of RHRP1560 are used in the prototype.

The tested gate signals of three power transistors and the secondary voltage of the transformer are shown in **Figure 4**. The logics relation of three driving signals is same as **Figure 2**. The secondary voltage is a three-level waveform.

Figure 5 shows the measured waveforms of the proposed converter at full load. It is obvious that Q_1 achieves zero-voltage turn-on and turn off at half of peak current as shown in **Figure 5(a)**. The extra Q_3 also obtain zero-voltage turn-on as showed in **Figure 5(b)**. **Figure 5(c)** shows that the secondary current has a quick drop

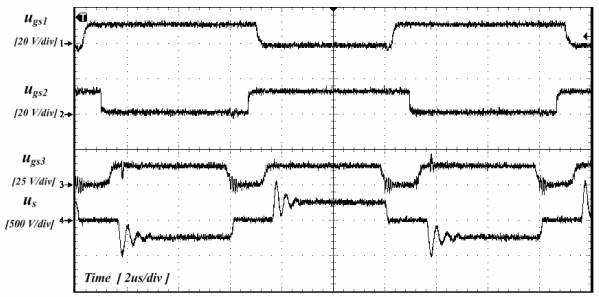
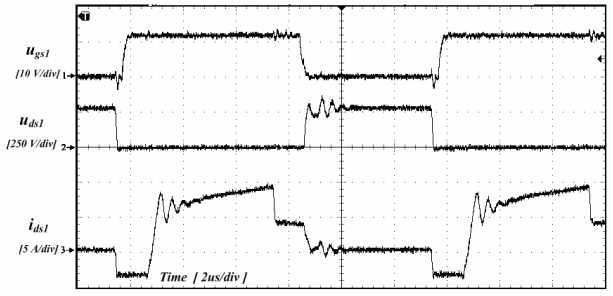
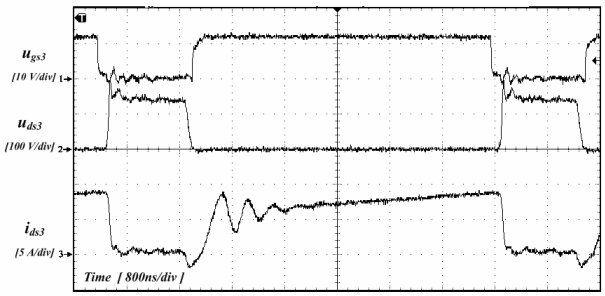


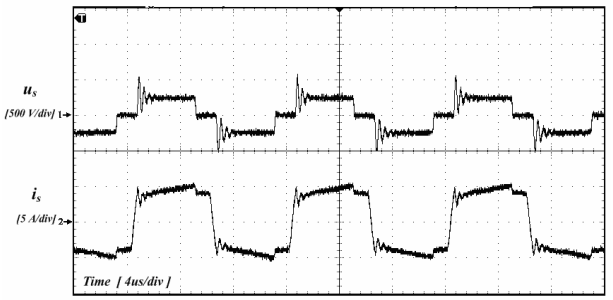
Figure 4. Three driver signals and secondary voltage waveforms.



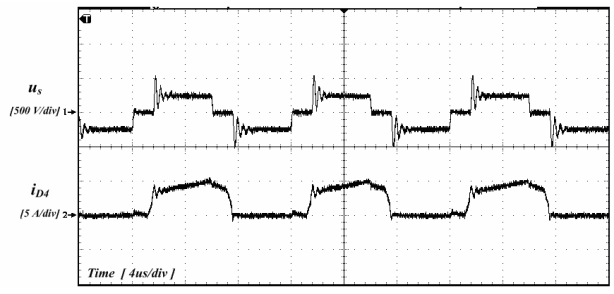
(a) u_{gs1}, u_{ds1}, i_{ds1}



(b) u_{gs3}, u_{ds3}, i_s



(c) u_s and i_s



(d) u_s and i_{D4}

Figure 5. Experimental waveforms with full load.

when Q_3 turns off. This phenomenon is produced by discharger current of parasitic capacitor of transformer as described in mode 1. The micro-commutation process of four diodes as Q_3 turn-off is also showed as i_{D4} in **Figure 5(d)**. In addition, the duty cycle loss can be found in **Figure 5(c)**.

The main transistor Q_1 also achieves ZVS under 250 W load as shown in **Figure 6**. Q_3 can no longer achieve zero-voltage turn-on at 450w load as shown in **Figure 7**,

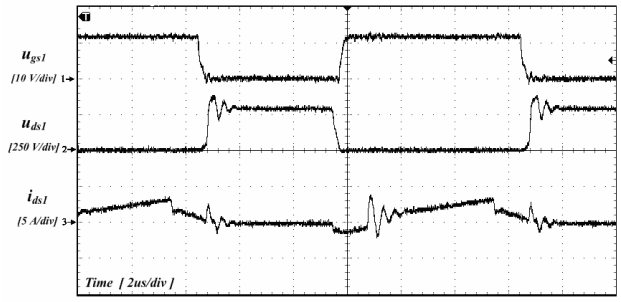


Figure 6. u_{gs1} ,u_{ds1} and i_{ds1}waveforms with 250 W load.

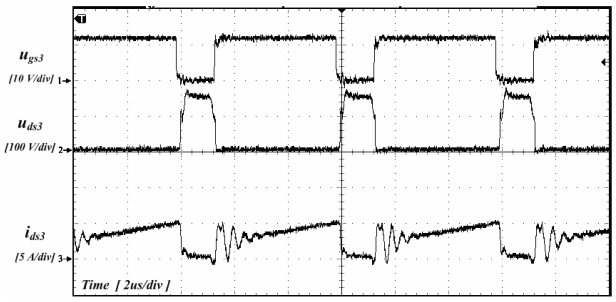


Figure 7. u_{gs3} ,u_{ds3} and i_{ds3} waveforms with 450 W load.

but only hard switching on as u_{ds3} drops to 100 V.

The measured efficiency of this TTPP converter at full load is 94.8%.

5. Conclusions

A TTPP converter which can achieve ZVS is presented in this paper. It only requires an extra transistor to be inserted between the input power source and midpoint of two primary windings in traditional push-pull converter. Adopting phase-shifting concept, the logic of the three driving signals is similar to that in phase-shift full-bridge converter. So this TTPP converter has a similar operation theory as phase-shifting full-bridge converter. Its two primitive power switches can obtain wide range ZVS. The extra power switch can achieve ZVS based on the energy of the leakage inductance. Its transformer waveform is as same as that in phase-shifting full-bridge circuit. As a result, this TTPP converter has a characteristic between traditional push-pull converter and phase-shifting full-bridge converter. It could be applied in many fields.

6. Acknowledgements

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