

Optimizing the Stage Resolution of a 10-Bit, 50 Ms/Sec Pipelined A/D Converter & Its Impact on Speed, Power, Area, and Linearity

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ABSTRACT

At high speeds and high resolution, the Pipeline ADCs are becoming popular. The options of different stage resolutions in Pipelined ADCs and their effect on speed, power dissipation, linearity and area are discussed in this paper. The basic building blocks viz. Op-Amp Sample and Hold circuit, sub converter, D/A Converter and residue amplifier used in every stage is assumed to be identical. The sub converters are implemented using flash architectures. The paper implements a 10-bit 50 Mega Samples/Sec Pipelined A/D Converter using 1, 1.5, 2, 3, 4 and 5 bits/stage conversion techniques and discusses about its impact on speed, power, area, and linearity. The design implementation uses 0.18 μm CMOS technology and a 3.3 V power supply. The paper concludes stating that a resolution of 2 bits/stage is optimum for a Pipelined ADC and to reduce the design complexity, we may go up to 3 bits/stage.

Keywords: Switched Capacitor Sample and Hold Circuit; 1.5 Bits/Stage; Linearity; Power; Redundancy; Folded Cascode Op-Amp

1. Introduction

Although many Pipelined ADC architectures are discussed in literature, the number of bits/stage conversion was always a designer's choice. Many designers preferred a stage resolution of 3 bits just to reduce the design complexity. This paper discusses the options of number of bits/stage conversion techniques in Pipelined ADCs and their effect on area, speed, power dissipation and linearity. The paper examines 1, 1.5, 2, 3, 4 and 5 bits/stage conversion to implement a 10-bit Pipelined ADC. In the analysis, all the basic blocks are assumed to be identical.

The rapid advancements in electronics has resulted in digital revolution with telephony switching systems in 1970's and continued with digital audio in 1980's and digital video in 1990's. This is expected to prevail in the present multimedia era and even can influence in future systems. Since all electrical signals are analog in nature and since most signal processing is done in the digital domain therefore, A/D and D/A Converters have become a necessity. Flash ADC makes all bit decisions in a single go while successive approximation ADC makes single bit decision at a time. Flash ADCs are faster but area increases exponentially with bit length while successive

approximation ADC is slow and occupies less area.

Between these two extremes many other architectures exist deciding a fixed number of bits at a time such as pipeline and multi step ADCs. They balance circuit complexity and speed. **Figure 1** shows recently published high speed ADC architecture applications and resolution versus speed. In general, three architectures are suitable for three important areas of usage. For example, over sampling converter is used exclusively to achieve high resolution (greater than 12 bits at low frequencies). For medium speed with high resolution multi step and Pipeline ADCs are promising. At extremely high frequencies, flash ADCs survive but only at low resolution.

Figure 2 shows resolution versus speed depicting this trend. Most architecture known to date is not likely to achieve a resolution of 12 bits at over 100 MHz using even 180 nm to 90 nm technologies. However, two high speed architectures, namely multi step, pipelined and folding are potential architectures to challenge in times to come.

1.1. Flash ADC

The straightforward approach for A/D Conversion is to compare the input with all divided levels of the reference voltage and this is used in flash ADC. The conversion

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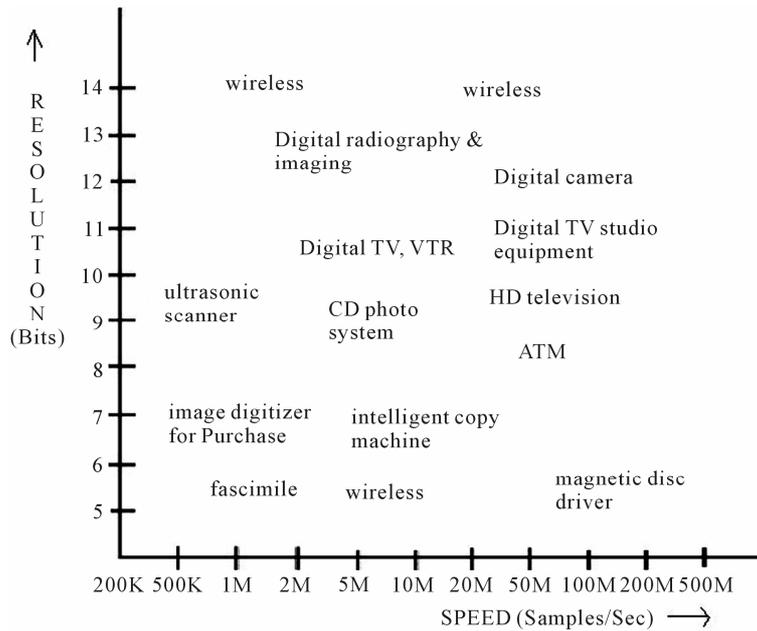


Figure 1. Speed versus resolution.

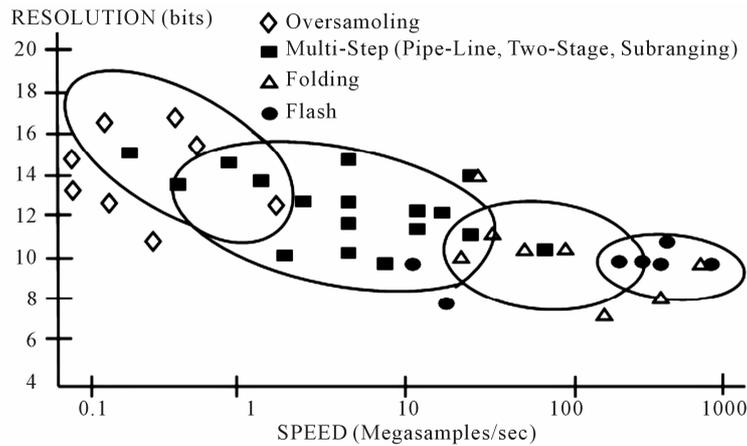


Figure 2. Performance of recently published ADCs.

completes in a single step. Therefore, flash ADC is the fastest of all ADCs. **Figure 3** shows flash ADC technique. As the output of comparator set is thermometer coded, the priority encoder is required. The performance is decided by the comparator resolution and the accuracy of voltage divisions. Practically, the exponential growth of the number of comparators and resistors with increased bit size limits the usage of flash ADCs. An N bit flash ADC requires 2^{N-1} comparators and 2^N resistors. Also with increased bit length, the comparators present significant capacitive loading on the Sample and Hold circuit thus reducing the speed of conversion.

As the comparators number increases and also the capacitive loading, the power consumption also becomes high. Therefore, flash converters are preferred for bit length less than 8 only. Flash ADCs are preferred as

coarse and fine quantizers in multi step and Pipeline ADCs.

1.2. Multi Step ADC

Instead of making all bit decisions at a time as in flash ADC or single bit decision at a time as in successive approximation ADC, we can resolve a few bits at a time as it makes the system simpler and easily manageable [1].

It also allows us to use digital error correction mechanism. This is adopted by the multi step ADC architecture. Here only a single Sample and Hold circuit is used and every stage requires a coarse ADC, DAC and a residue amplifier as shown in **Figure 4**. We need to use multi phase clocking scheme to complete conversion in one clock cycle. In the multi step architecture, number of

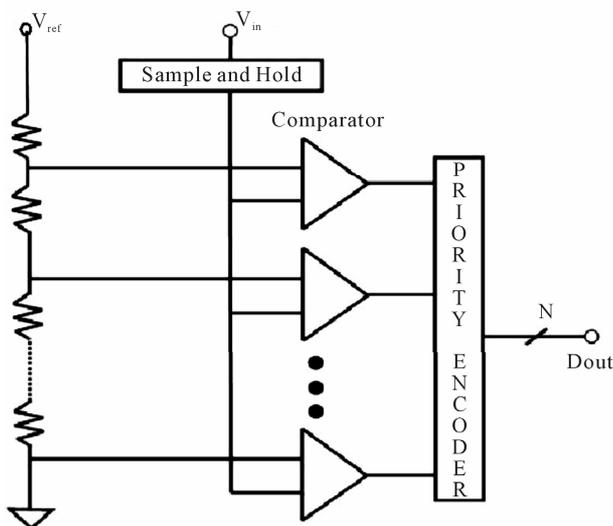


Figure 3. Flash ADC architecture.

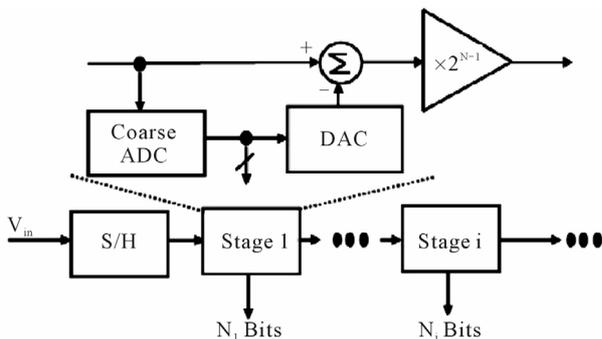


Figure 4. Multi step ADC architecture.

steps are usually limited to two due to the difficulty in multiphase clocking. Also it doesn't reduce speed much and can use standard two phase clocking.

1.3. Pipeline ADC

Although simpler and manageable, as the number of bits/stage increase, the complexity of two steps ADC still grows exponentially. For resolution of 10 bits and above, the complexity reaches a maximum and hence the need for pipelining the sub ranging blocks arises.

Figure 5 shows the Pipeline ADC architecture. It looks similar to multi step ADC architecture except that every stage uses a separate Sample and Hold circuit.

Since Sample and Hold circuits are clocked by alternating clock phases, therefore, in every clock phase, a stage must perform the bit decision and amplify the difference signal to generate the residue for the next stage. Pipelining the residue greatly simplifies the ADC architectures. The complexity now grows linearly with the number of bits to resolve and hence is becoming popular. Here, the overall performance is limited by the accuracy of the residue amplifier. The potential error sources are

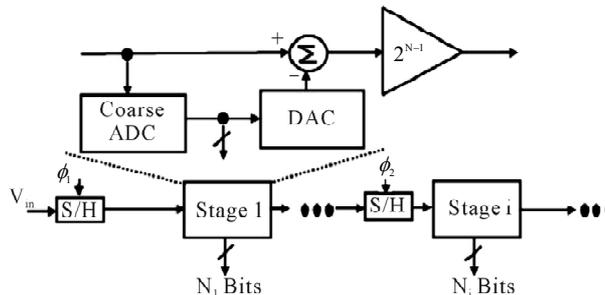


Figure 5. Pipeline ADC architecture.

the settling behavior of the amplifier, ADC/DAC resolution and gain error of residue amplifier.

2. Types of Pipelined ADCs

2.1. One Bit/Stage Pipeline ADC

The simplest case of Pipeline ADC is to resolve 1 bit per stage as shown in Figure 6.

Each stage here performs the following operations:

The sampled signal is compared with $V_{ref}/2$ and the output of each comparator becomes the converted bit for that stage.

If $V_{in} > V_{ref}/2$, the output of comparator = "1", then $V_{ref}/2$ is subtracted from the held input signal and the difference is passed to the amplifier with a gain of 2. The result is passed as input to Sample and Hold circuit of the next stage.

In Pipeline ADC architecture, the MSB stage must be carefully designed. A slight error in first stage propagates through the converter and hence can result in a much bigger error at the end of conversion. The succeeding stages can be less accurate. The comparator and summer offsets together must be less than 1/2 LSB to keep the ADC accurate.

2.2. Bits/Stage Pipeline ADC

Using cascaded lower resolution stages [2-4], the Pipelined ADCs get their final resolution. For example, a 12-bit ADC can use a cascade of four 3-bit stages. Many designers are comfortable with 3-bit flash ADCs. However, 1.5 bits/stage is also becoming increasingly popular. There is an advantage of going for minimum stage resolution for high speed converters. It minimizes the inter stage gain required, which in turn maximizes the bandwidth, since gain bandwidth product is a constant for a given technology.

A 1.5 bits/stage is a 1 bit/stage into which some redundancy is added to compensate for device tolerances and imperfections [5]. A digital error correction mechanism later eliminates this redundancy. The 1.5 bits/stage uses two analog comparison levels V_u & V_L instead of a single level as in 1 bit/stage. Because of the use of gain of

two, they must lie between $+V_{ref}/2$ and $-V_{ref}/2$. A common choice is $V_L = -V_{ref}/4$ and $V_u = +V_{ref}/4$. The MDAC architecture and its voltage transfer characteristics are shown in **Figure 7** which is highly nonlinear. The input voltage range is divided into three sections. The low range (L) below V_L , mid range (M) between V_u and V_L and the upper range (U) above V_u , as shown in the **Table 1**. The implementation details of 1.5 bits/stage is shown in **Figure 7(a)**. A resistor string provides voltage division to create reference voltages V_u and V_L .

All other high accuracy operations such as multiply-by-two are achieved by capacitor ratios. The Sample and Hold circuit and multiply-by-two amplifier can be combined to form a Multiplying DAC (MDAC). The cascaded MDAC outputs are passed through latches before feeding them to the redundancy bit removal circuit as shown in **Figure 8**.

Redundancy Bit Removal Algorithm

The probable error sources in data converters include offset voltages in comparators and Op-Amps, gain error in amplifier, nonlinearity in converter and others. Many

of these errors are compensated by this algorithm [3,4].

Each 1.5-bit pipelined stage produces a 2-bit output code B1B0. Using redundancy bit removal algorithm, this is reduced to final 1 bit per stage code. For a resolution of 3 bits, the input voltage range of $+2 V$ is divided into 8 equal slots and **Table 2** shows input voltage, the code generation of each stage and corresponding stage residue voltages. To generate the final code, the two bit codes generated by each stage are added in a predetermined way. For example, as shown in **Table 2**, for $V_{in} = 0.8 V$, the codes generated by successive stages are 10, 01 and 00. These bits must be added as follows to generate the final 3-bit code.

Table 1. Implementation details of Figure 7(a).

V_{in}	Range	B_1	B_0	DAC output	Analog residue output
$V_{in} > V_u$	U	1	0	$+V_{ref}$	$2 V_{in} - V_{ref}$
$V_L < V_{in} < V_u$	M	0	1	0	$2 V_{in}$
$V_{in} < V_L$	L	0	0	$-V_{ref}$	$2 V_{in} + V_{ref}$

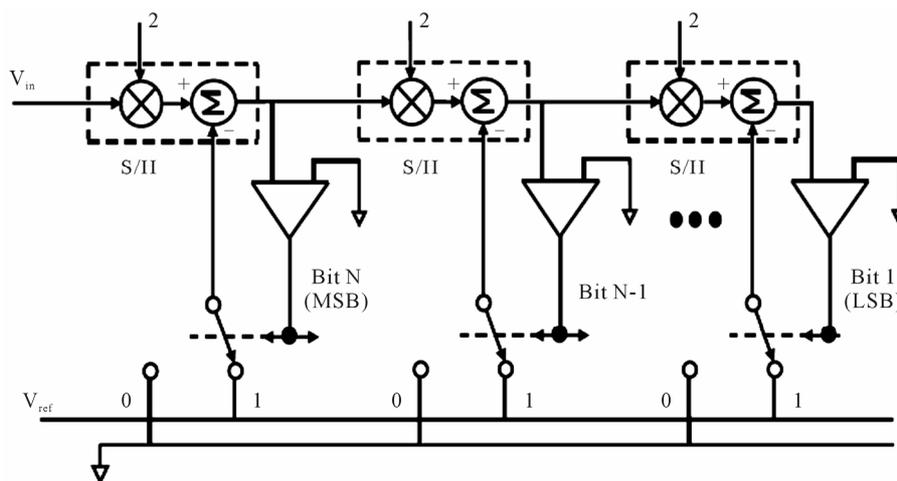


Figure 6. One bit/stage Pipeline ADC architecture.

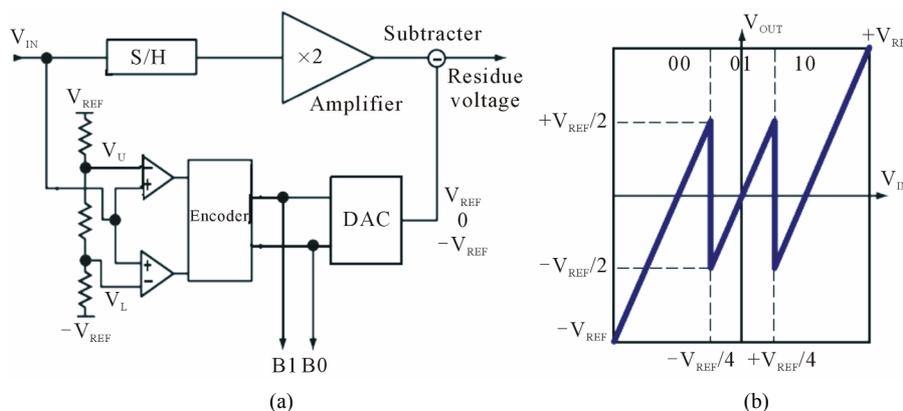


Figure 7. 1.5 Bit conversion technique. (a) MDAC; (b) Transfer characteristics.

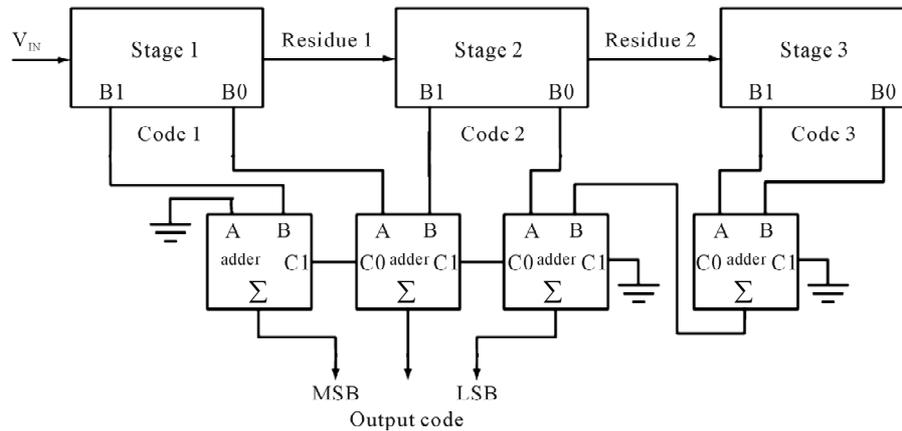


Figure 8. Implementation of redundancy bit removal algorithm.

Table 2. Development of error corrected output code.

V_{IN} (V)	RANGE (1)	CODE (1)	RES (1)	RANGE (2)	CODE (2)	RES (2)	RANGE (3)	CODE (3)	OUTPUT CODE
1.80	U	10	1.60	U	10	1.20	U	10	111
1.23	U	10	0.46	M	01	0.92	U	10	110
0.80	U	10	-0.40	M	01	-0.80	L	00	101
0.30	M	01	0.60	U	10	-0.80	L	00	100
-0.26	M	01	-0.52	L	00	0.96	U	10	011
-0.70	L	00	0.60	U	10	-0.80	L	00	010
-1.30	L	00	-0.60	L	00	0.80	U	10	001
-1.60	L	00	-1.20	L	00	-0.40	L	00	000

$$\begin{array}{r}
 1\ 0 \\
 +\ 0\ 1 \\
 +\ \underline{0\ 0} \\
 \hline
 1\ 0\ 1\ 0
 \end{array}$$

Discard LSB and the final digital code is 101 for the case $V_{in} = 0.8\text{ V}$ as shown in row 3 of Table 2.

The circuit implementation is shown in Figure 8.

2.3. Two Bits/Stage and Above

The 10-bit Pipelined ADC is implemented in 5 stages with 2 bits/stage, and in 4 stages using 3 bits/stage converting 3, 3, 3 and 1 bit respectively in consecutive stages [6]. Using 4 bits/stage conversion, the ADC is implemented in 3 stages converting 4, 4, 2 bits in successive stages and so on. All the sub converters are implemented using flash architectures already discussed.

3. Implementing the Pipelined ADC

The design issues of various building blocks are discussed in this section. The same blocks are used in dif-

ferent stages and the analysis is done with respect to area, speed of conversion, power dissipation and linearity.

3.1. Folded Cascode Op-Amp

Modern integrated CMOS Op-Amps are designed to drive capacitive loads. For capacitive loads, it is not necessary to use a buffer at the output (for providing a low impedance node). Therefore, it is possible to design Op-Amps at larger voltage swings and higher speeds than those which drive pure resistive loads [7-9]. These improvements are achieved with a single high impedance node at the output that drives only capacitive loads. For folded cascode Op-Amps the compensation is achieved by load capacitance C_L itself and it provides dominant pole compensation. As C_L increases, the Op-Amp stability improves but gets slowed down. The schematic of folded cascode Op-Amp is shown in Figure 9. The basic idea of folded cascode Op-Amp is to apply the opposite type PMOS cascode transistors to the input differential pair of NMOS type. The design of Op-Amp is becoming increasingly difficult as supply voltages and transistor channel lengths are scaled down. There are several

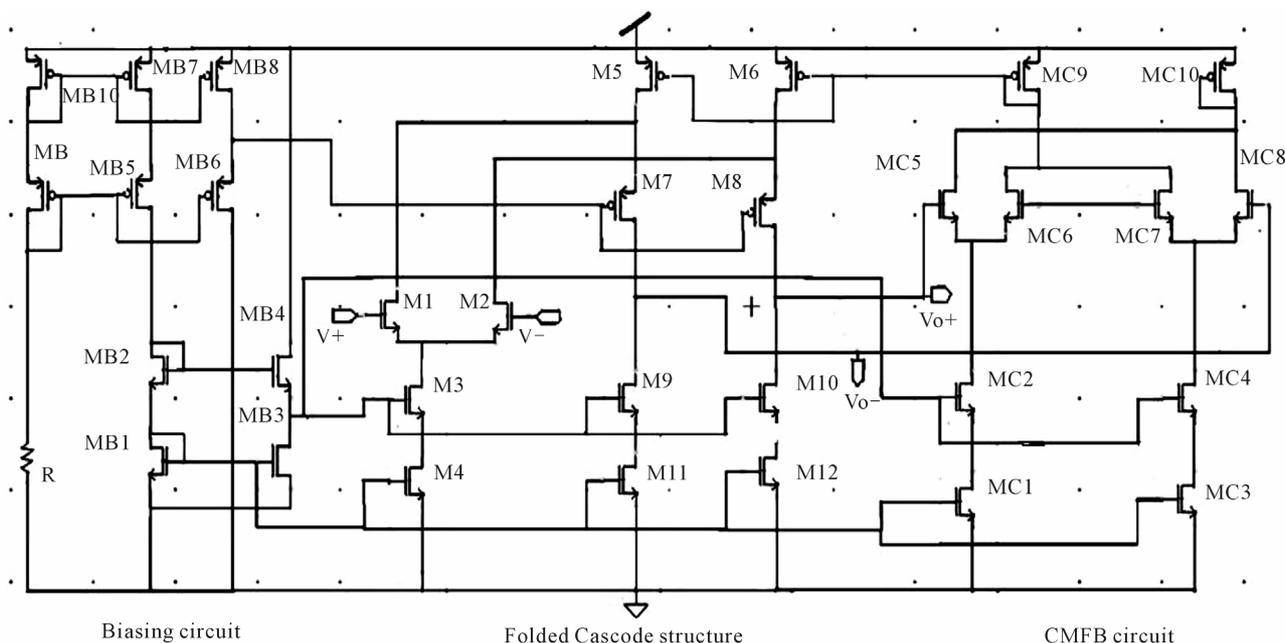


Figure 9. Folded cascode Op-Amp.

Op-Amp topologies possible viz. Two stage CMOS Op-Amp, regulated cascode Op-Amp, folded cascode Op-Amp and Telescopic cascode Op-Amp etc. A two stage CMOS Op-Amp is preferred where high gain and large output swing are required. However, the addition of second stage reduces unity gain frequency and hence speed of operation. A telescopic cascode Op-Amp offers better power and bandwidth criterion but has severe drawback of reduced output swing and hence not preferred for low voltage applications. Folded cascode Op-Amp provides higher output swing compared to telescopic cascode Op-Amp and better PSRR and speed over two stage Op-Amp. Hence folded cascode Op-Amp is used here.

This arrangement allows the output to be taken at the same bias levels as that of input signal. Even though it is a single stage, the gain is reasonable since the gain is decided by the product of input transconductance and the larger output impedance. The design uses band gap reference and common mode feedback circuit (CMFB). The Op-Amp results of **Figure 10** shows a unity gain frequency of 200 MHz at 88° phase margin and a gain of over 70 dB and 300 MHz at 72° phase margin for the same gain.

3.2. Sample and Hold Amplifier

The fully differential Sample and Hold implementation is shown in **Figure 11**. We can determine the input/output relationship of Sample and Hold circuit by evaluating the charge stored on C_i and C_f .

And the expression for output can be written as

$$V_{out} = V_{out+} - V_{out-}$$

$$= \left(1 + \frac{C_i}{C_f}\right)(V_{in+} - V_{in-}) - \frac{C_i}{C_f}(V_{ci+} - V_{ci-}) \quad (1)$$

If $C_i = C_f$, then a gain of two is achieved [10]. By connecting V_{ci+} and V_{ci-} to $+V_{ref}$ and $-V_{ref}$, we can get $2 V_{in+}$, $(2 V_{in+} + V_{ref})$ and $(2 V_{in-} - V_{ref})$ required for A/D Conversion. The simulated results of **Figure 12** show a sampling rate of 100 Msps. The power dissipation is seen to be 8 mW for 3.3 V supply.

3.3. Comparator

The comparator has three stages, the differential stage, decision making stage and the level restoring stage as shown in **Figure 13**. The simulation results of **Figure 14** show the comparator delay as 3.28 nS.

3.4. DAC Unit

The design uses a simple two way analog switch for 1-bit DAC and a current steering R-2R ladder DAC for higher number of bits. The resistor string is shared between the flash sub converter and the DAC to minimise the area [7].

4. Results

4.1. Effect of Bits/Stage on Area

If the total area of ADC is A_{tot} and area of one stage is A_s , then the total area is given by

$$A_{tot} = \left(\frac{N-r}{n-r}\right) A_s \quad (2)$$

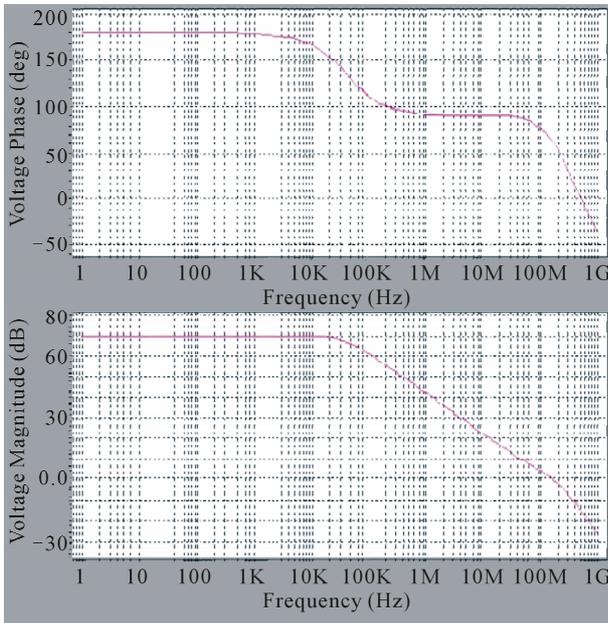


Figure 10. Gain & phase margin of FC Op-Amp.

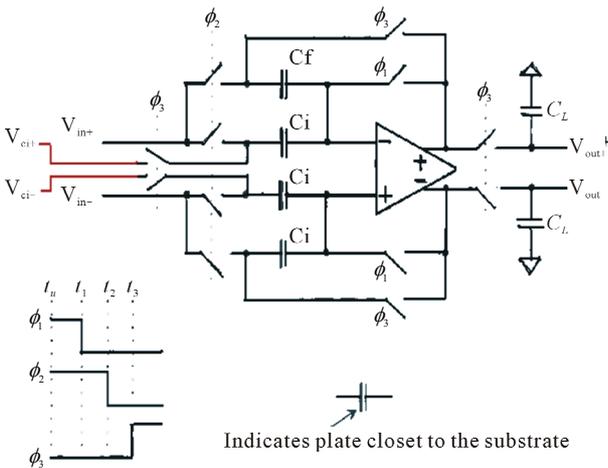


Figure 11. Switched capacitor S/H circuit.

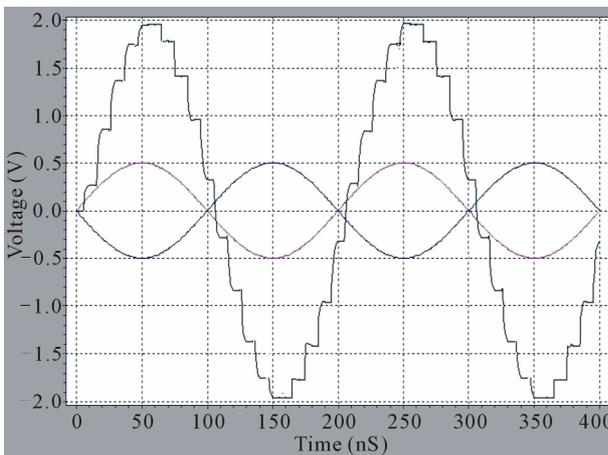


Figure 12. Sample and Hold output at 100 Msp.

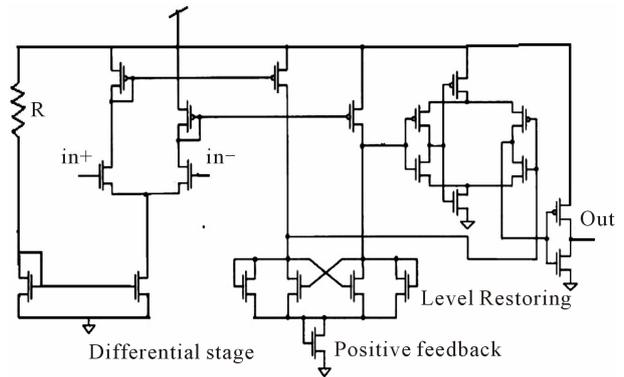


Figure 13. A high speed comparator.

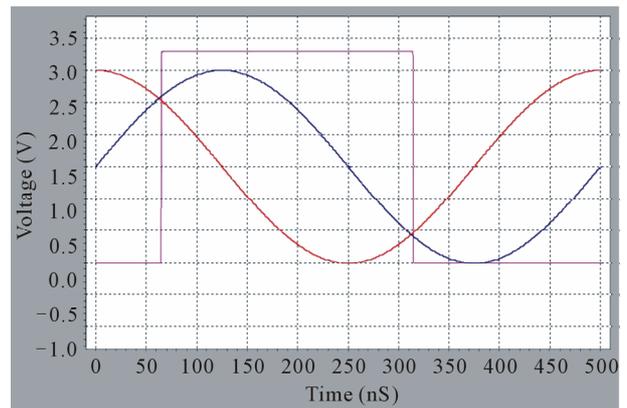


Figure 14. Simulation results of comparator.

where

- N : Number of bits,
- n : Number of bits converted per stage and,
- r : Redundancy.

A_{tot} doesn't include the area occupied by the digital error correction, bias generation, clock generation and I/O pads. These areas are independent of n . The area of one stage includes the areas of comparator, DAC unit and that of sample & hold.

$$A_s = A_{comp} (2^{N-1}) + A_{DAC} + A_{SH} \quad (3)$$

A_{SH} is observed to be almost proportional to $2n$. As n increases, the numbers of comparators increase and the delay increases. Therefore to reduce the settling time for the given load, the transconductance of the amplifier must be increased proportionally [4]. To increase the transconductance, the area of Sample and Hold and power dissipation must proportionally increase. If redundancy is introduced, then A_{SH} can be made independent of n (as incomplete settling is allowed). If n is decreased, then number of stages will increase and A_{SH} will increase. Therefore, A_{SH} will dominate for small values of n and if n is large, then A_{comp} dominates over A_{SH} . Figure 15 shows the area distribution of Pipelined ADC.

The normalized area as a function of bits/stage is

shown in **Figure 16** where we see that the area reduces as we reduce the number of bits/stage showing a dip at 2 bits/stage.

4.2. Effect of Bits/Stage on Conversion Frequency

Since the sub ADCs use flash architectures, only two phase clocking is required for conversion. During phase 1, the first stage samples the input while the remaining odd stages samples the residue outputs of even stages. During phase 2, the even stages sample the outputs of odd stages. Therefore, the minimum duration of clock phase is set by the maximum settling time of the Sample and Hold amplifier [12].

If the two phases are of equal duration, then the maximum frequency of conversion F_c of ADC

$$F_{cmax} \leq \frac{1}{2(t_{smax})} \tag{4}$$

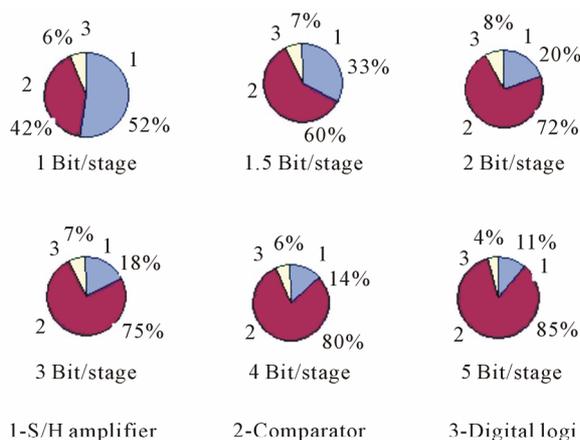


Figure 15. Area distributions among the blocks.

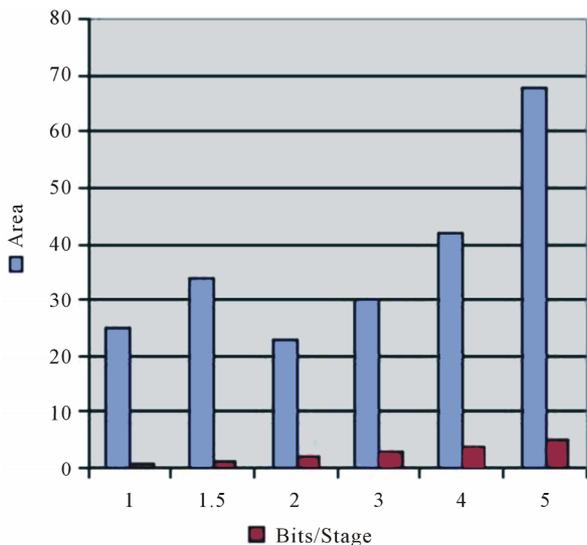


Figure 16. Normalized area vs bits/stage.

where t_{smax} is the maximum settling time of Sample and Hold amplifier.

If the Sample and Hold amplifier has a single pole transfer function (dominant pole compensation), and if unity gain frequency is f_u , and if the input is a unit step function, then the gain of Sample and Hold amplifier is given by

$$A(t) = 2^{n-r} (1 - e^{-t/\tau}) \tag{5}$$

where

$$\tau = \frac{2^{n-r}}{f_u} \tag{6}$$

The first term of Equation (5) represents the ideal gain and the second term is because of incomplete settling. Even though Sample and Hold amplifiers are assumed to be identical, their settling times will not be identical and it is observed that the second stage Sample and Hold amplifier has maximum settling time t_{smax} .

$$t_{smax} = t_{s2} \approx (N - n + r) 2^{n-r} \frac{\ln 2}{f_u} \tag{7}$$

Substituting Equation (7) into Equation (6) gives

$$F_{cmax} \leq \frac{f_u}{(N - n + r) 2^{n-r+1} \ln 2} \tag{8}$$

Referring to Equation (8), the maximum frequency of conversion decreases for an increase in the bits/stage. Hence to increase the conversion frequency, the bits/stage must be minimized. The conversion frequency rates for the different bits/stage combinations are shown in **Figure 17**.

4.3. Effect of Bits/Stage on Power Dissipation

In ADCs the power is dissipated in Sample and Hold amplifier, sub converter, digital logic and biasing networks. The power dissipated in digital logic and biasing networks is much smaller than that in Sample and Hold amplifiers and sub converters. For reduced bits/stage, power dissipation in Sample and Hold amplifiers dominates while for increased bits/stage, the sub converter power dissipation dominates over Sample and Hold amplifiers. The power dissipation curves for various bits/stage conversions are shown in **Figure 18**.

4.4. Effect of Bits/Stage on Linearity

The error sources in Pipelined ADCs are offset, gain and non-linearity errors in Sample and Hold amplifiers, sub converters and DACs. The offset and gain errors can be compensated simply by scaling Rf/Ri or Ci/Cf in the amplifiers and offsetting the input to the ADC. Hence they are not so important in the determination of optimum

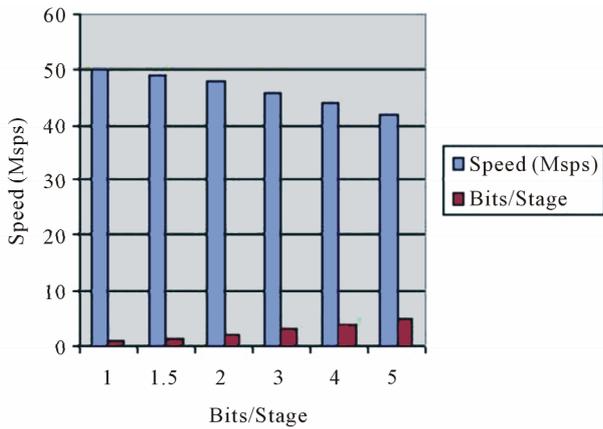


Figure 17. Frequency conversion rates vs bits/stage.

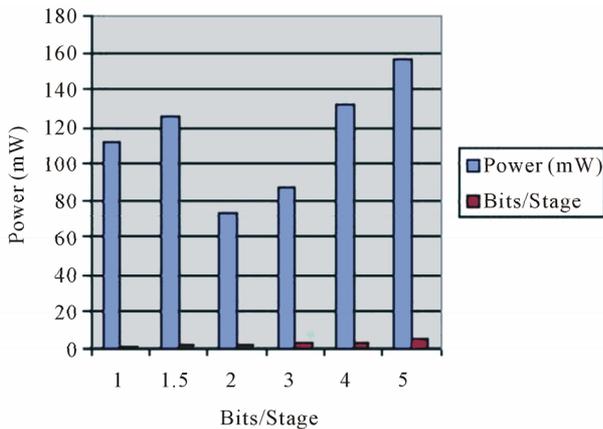


Figure 18. Power dissipation vs bits/stage.

number of bits/stage conversion. However, the non-linearity error is more difficult to compensate. Figure 19 shows the signal flow model of a pipelined ADC with n stages and error sources $e_1 \dots e_m \dots e_n$. Here e_m represents the error of stage m and the error includes gain, offset, quantization and non-linearity errors.

The total error when reflected back into the input can be represented as

$$e_{input} = e1 + \sum_{m=1}^{n-1} \frac{e_{m+1}}{A^m} \tag{9}$$

Equation (9) shows that as gain A increases, the effects of non-idealities of all stages after the first stage becomes smaller. Therefore, to limit the error of ADC to less than $\pm 1/2$ LSB,

$$e_m \leq \frac{\text{Full Scaleoutput}}{2^{N+1}} A^{m-1} \tag{10}$$

If the error in all stages are identical, i.e. $e = e_m$, then (9) becomes

$$e_m = e \left(1 + \sum_{m=1}^{n-1} \frac{1}{A^m} \right) = e \cdot M \tag{11}$$

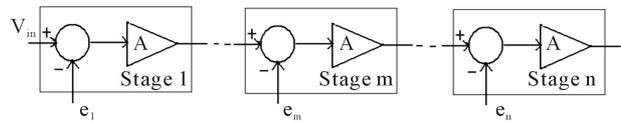


Figure 19. Signal flow graph of Pipelined ADC.

Referring to Equation (11), it is clear that the total error of all stages is equal to the first stage error multiplied by a factor M , which in turn depends on the gain A of the Sample and Hold amplifier. If $A = 1$ then $M = n$ and if $A \gg 1$ then $M = 1$. The boundary condition between these two cases is with $A = 2$ gives $M = 2$. Therefore, to make the first stage error to dominate over all other errors, the number of bits/stage must be chosen so that A is ≥ 2 . Hence, more the number of bits/stage less is the non-linearity error in Pipelined ADCs. The sub converter and DAC errors can be eliminated by using redundancy and digital error correction mechanism and hence not considered here.

5. Conclusion

With pipelining, the maximum conversion frequency is seen to be almost independent of the number of stages. This allows the bit/stage is to be chosen to fulfill other requirements. This paper concludes that minimizing the bits/stage maximizes the conversion frequency and also minimizes the power dissipation and area requirements and the optimum value is 2 bits/stage. The effect of bits/stage on linearity is seen to be small but the linearity is seen to improve if we can increase the number of bits/stage. Confining the bits/stage to two, we get optimum results with respect to area, speed, power dissipation and linearity.

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