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Design of a Low Power Low-Noise Amplifier with Improved Gain/Noise Ratio

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Abstract

This work details the development of a broad-spectrum LNA (Low Noise Amplifier) circuit using a 65 nm CMOS technology. The design incorporates an inductive degeneracy circuit, employing a theoretical approach to enhance gain, minimize noise levels, and uphold low power consumption. The progression includes a shift to a cascode structure to further refine LNA parameters. Ultimately, with a 1.8 V bias, the achieved performance showcases a gain-to-noise figure ratio of 16 dB/0.5 dB, an IIP3 linearity at 5.1 dBm, and a power consumption of 3 mW. This architecture is adept at operating across a wide frequency band spanning from 0.5 GHz to 6 GHz, rendering it applicable in diverse RF scenarios.

Keywords

LNA, Degeneracy, Noise Figure, Linearity, Power Consumption, Gain

1. Introduction

In an RF reception chain, the Low Noise Amplifier (LNA) plays a critical role, since it brings the useful signal from the receiving antenna to a high-level signal that will be correctly processed by the blocks located downstream of the RF chain. Positioned upstream (**Figure 1**), it requires higher gain, and its noise factor significantly determines the overall noise factor of the system.

When designing LNAs, four main types exist regardless of the technology used [2]: resistance termination, resistive feedback, 1/gm termination, and inductive degeneration. Unlike other architectures, the last one adapts perfectly without adding noise to the system.

Recent research indicates a predominant preference for employing the LNA architecture with inductive degeneration, for example: [3] focuses on designing

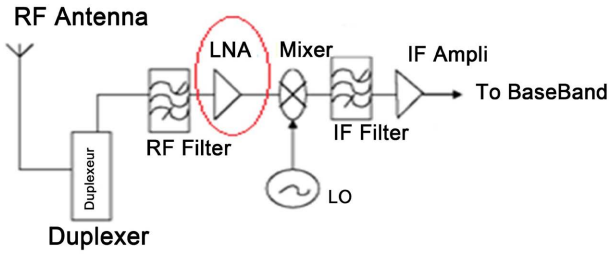


Figure 1. LNA in RF reception chain [1].

for high linearity while maintaining low power consumption in biomedical instruments, the objective of this following work [4] is to enhance the gain without deterioration in other parameters by cascode LNA using an extra capacitor, another study centers on a PVT compensation to reduce the sensitivity of the circuit to PVT variations [5], then a novel configuration in an inductor-less ultra-wideband LNA for cognitive radio systems [6] [7] proposes a technique to enhance linearity for large input signals with a new composites transistor, then [8] uses the Advanced Compact MOSFET (ACM) model alongside a Lookup Table (LUT) to encompass transistor behavior across various operational modes, enabling seamless integration into digital computing environments.

The present work utilizes the inductive degeneracy source in the LNA topology as a reference by adopting a theoretical approach that allows for an adjustment between gain and noise figure while maintaining low power consumption. The LNA designs developed in this paper are based on 65 nm CMOS technology, beginning with a simple structure and then refined through a second assembly employing a two-stage structure.

2. Methodology for Enhancing Gain-to-Noise Ratio

2.1. Circuit Gain

The LNA structure with inductive degeneration, being illustrated by **Figure 2**, whose general gain formula is expressed by Equation(1):

$$G = \frac{V_{out}}{V_{in}} \tag{1}$$

The signal V_{in} being received from the antenna, the gain (G) increases if the amplitude of the signal V_{OUT} increases. According to the **Figure 2**: knowing that V_{DS} is the voltage between the drain and the source of the MOSFET transistor, and that V_{DS} is the potential of its source:

$$V_{out} = V_{DS} + V_S \tag{2}$$

The CMOS works in the ohmic zone then [9]:

$$V_{DS} = R_{on} I_{DS} \quad \text{where} \quad R_{on} = \frac{1}{\mu_n c_{OX} \frac{W}{L}\left(V_{GS} - V_{tn}\right)} \tag{3}$$

With Ids is the Drain-Source current

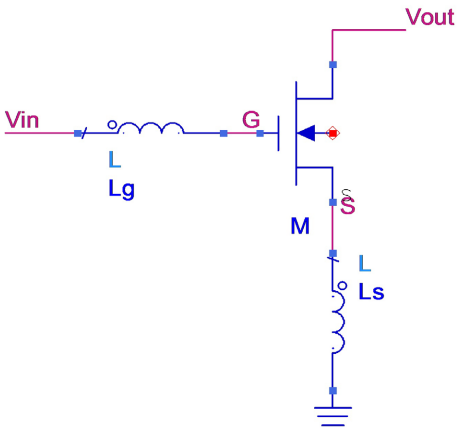


Figure 2. Basic assembly of the LNA circuit.

The voltage V_S is across the terminals of the inductance L_s, I_s represents the current flowing through it, where I_g represents the gate G current (**Figure 2**):

$$V_s = L_s \omega I_s \tag{4}$$

$$I_S = I_G + I_{DS} \tag{5}$$

And

$$I_G = \frac{V_{in}}{(L_G + L_S)\omega} \tag{6}$$

According to Equation (1), and knowing that the input signal V_{in} (**Figure 2**) is fixed by the antenna, increasing the gain G is directly linked to increasing the amplitude of the output signal V_{OUT}, since this latter is the sum of the voltages V_{DS} and V_S (Equation (2)). Therefore, an enhancement in V_{OUT} amplitude is attributed to the improved V_{DS} and V_S.

Depending on the chosen technology (CMOS 65 nm), the length L of the MOSFET channel is set at 65 nm, while keeping the other parameters fixed, the choice of a relatively wide MOSFET channel (W) will improve the V_{DS} voltage amplitude.

Regarding the voltage V_S:

$$V_S = L_S \omega I_S \tag{7}$$

From Equation (6) and Equation (7), it's enough to fix the impedance L_g and increase L_s, in other words; current Is is increased if I_g is increased. We can keep (L_s + L_g) low; if we set Ls to a value, we can minimize the value of L_g (L_s is fixed, L_g is small, W is large).

We can keep the sum L_s + L_g small; if we fix L_s to a value, we can minimize the value of L_g (L_s is fixed, L_g is small, W is large).

2.2. Technique for Enhancing Gain

In order to improve the gain of the chosen LNA circuit, we can add an impedance Z in series (**Figure 3**), which will improve the V_{OUT} voltage relative to **Figure 2**.

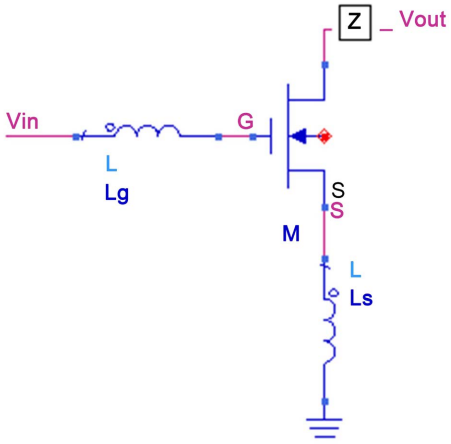


Figure 3. Basic layout of the LNA circuit after inserting Z.

Since V_{in} is fixed by the antenna, if we increase V_{OUT}, according to **Figure 3**, V_{DS} will be:

$$V_{DS} = R_{on} I_{DS} + |Z| I_{DS} \tag{8}$$

In terms of noise, it's crucial to study the impact of noise associated with the C, L, and R components of impedance Z through simulation. Ideally, introducing only a resistor R whose noise impact is comparatively lower than that of L and C would be preferable.

2.3. Technique for Noise Minimization

The noise figure (NF) is generally represented by formula (Equation (9)), N_{OUT} represents the amplitude of the noise signal at the output, N_{in} is the noise at the input, and G represents the gain of the circuit:

$$NF = \frac{N_{out}}{N_{in}} \cdot \frac{1}{G} \tag{9}$$

N_{in} depends on the V_{in} input signal, according to Equation (9), to reduce the noise figure we can increase the gain G while reducing N_{OUT}, to do this, we can adjust the parameters of the MOSFET and the impedances L_s and L_g within the circuit.

Generally, there are three types of noise in a MOSFET transistor [9]: $1/f$ noise, noise induced in the grid: which can be neglected because the Cgs capacity is quite low, and noise of the drain current: in the ohmic zone the latter has no great effect.

According to Equation (10) [9], to have fairly a low $1/f$ noise, simply increasing the value of W slightly, this method has no influence either on the gain or on the power consumed by the circuit.

$$\overline{i_{nf}^2} = \frac{K}{f} \frac{g_m^2}{WLC_{ox}^2} \Delta f \tag{10}$$

3. Simulation Results

3.1. Basic Inductive Degeneration Circuit

The M1 and M2 MOSFETs in Figure 4 are chosen from the BSIM4 65 nm model, the channel width of NMOS M1 is 10 μm, The voltage and bias resistance are respectively set at 1.8 V and 1 kΩ. The impedances L_g and L_s are respectively equal to 0.5 nH and 10 nH.

Figure 5 and Figure 6 illustrate the signals $V_{in}(t)$ and $V_{OUT}(t)$:

From Figure 7 and Figure 8: at 1.9 GHz (cellular telecommunications for example), the simulation leads to a gain G of 13.7 dB, a noise figure NF equal to 1.6 dB and the 3rd order interception point (IIP3) corresponds to 2.4 dBm.

From Figure 9, the power consumption of the circuit will be around 3 mW (V_{dd} =1.8 V I_{DC} =1.524 mA).

3.2. Inductive Degeneration Circuit in Cascode Configuration

As illustrated in Figure 10, this structure allows both on-board adaptation and low noise, additionally, share the bias current and thus increase efficiency [2].

Maintaining the same values of frequency, amplitude, and DC component of the input signal V_{in} as mentioned in the previous paragraph. Thus, by sharing the same bias current (R2 = 1 kΩ) between both MOSFETs 1 and 3 (chosen to be identical with L = 65 nm and W = 10 um). This allowed, following simulations in various modes (using Agilent ADS tool),to observe the responses: Figures 11-15, respectively represent the time-domain responses of signals V_{in} and V_{out} , the gain and noise figure, the third-order intercept point, and the power consumed by the cascoded LNA circuit.

3.3. Comparison of Results for the Two Selected Structures

The table below (Table 1) summarizes the values obtained in simulation for these two different proposals, compared with the typical characteristics of an LNA circuit [10]. It is noticeable that the cascode inductive degeneration circuit maintains a low power consumption and exhibits both a better linearity and a good gain/noise ratio.

4. Comparison with Recent Works

The table below (Table 2) summarizes the simulation results of the last proposed circuit (proposed work 2) and compares them, within a similar frequency range, with those of some more recent achievements, including the typical characteristics [10] of LNA, and the work done by the simple inductive degeneration LNA (Proposed work 1) (section 2, paragraph 1). Our introduced LNA demonstrates notably: an elevated IIP3 (thanks to the cascoded configuration), and among the best voltage gains, a minimal noise figure. Positioning it as a superior choice for low-noise, controlled consumption, high-gain, and linearity receiver designs.

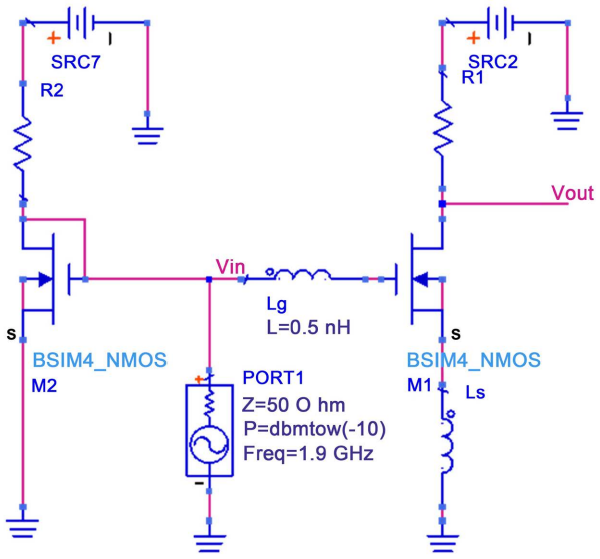


Figure 4. Proposed LNA (ADS tool) with inductive degeneration, simple circuit.

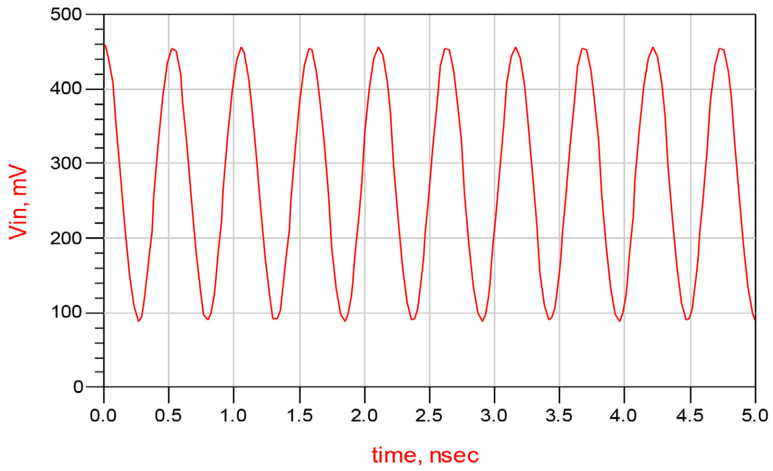


Figure 5. Input signal.

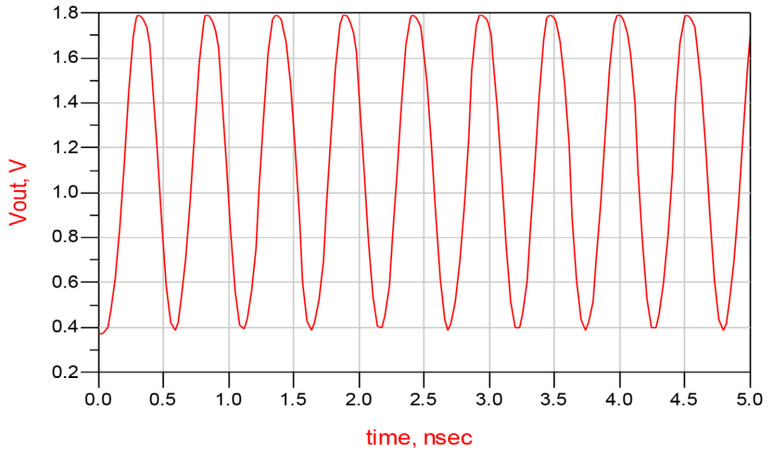


Figure 6. Output signal.

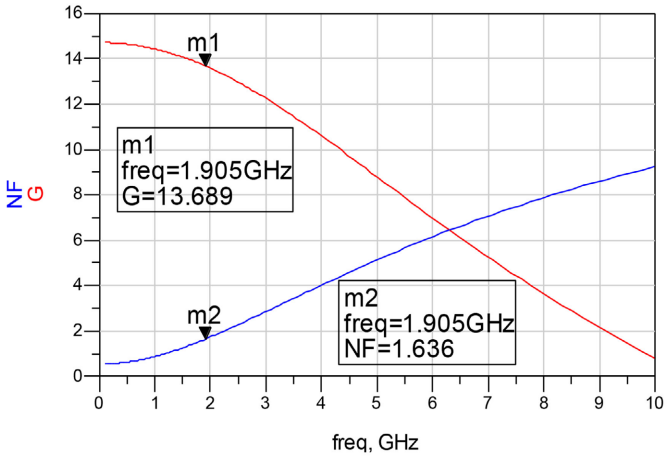


Figure 7. Gain and noise figure (first proposed circuit).

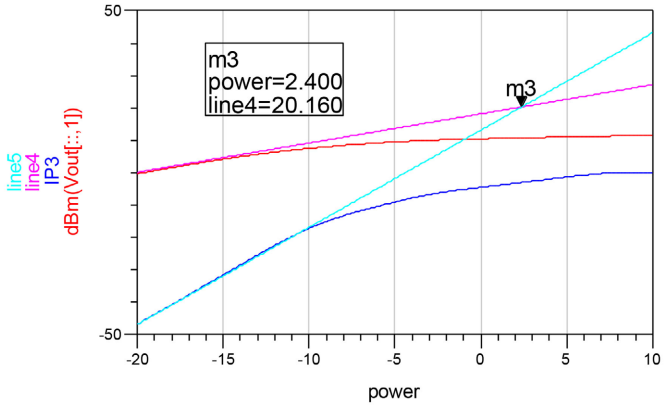


Figure 8. Linearity (first proposed circuit).

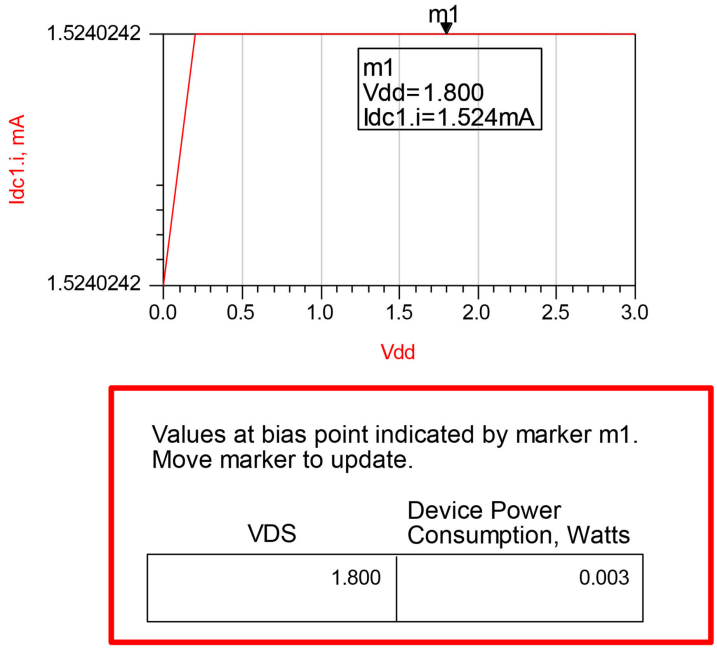


Figure 9. Power consumption (first proposed circuit).

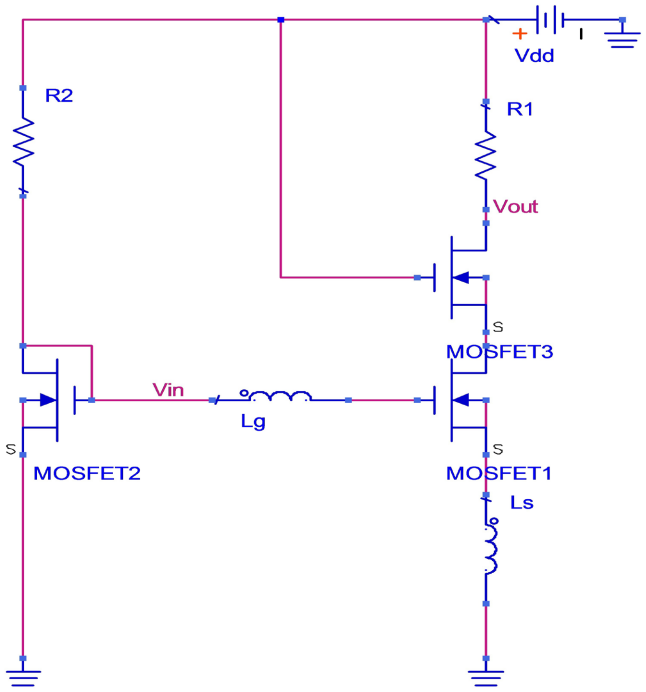


Figure 10. Proposed LNA with inductive degeneration, cascode circuit.

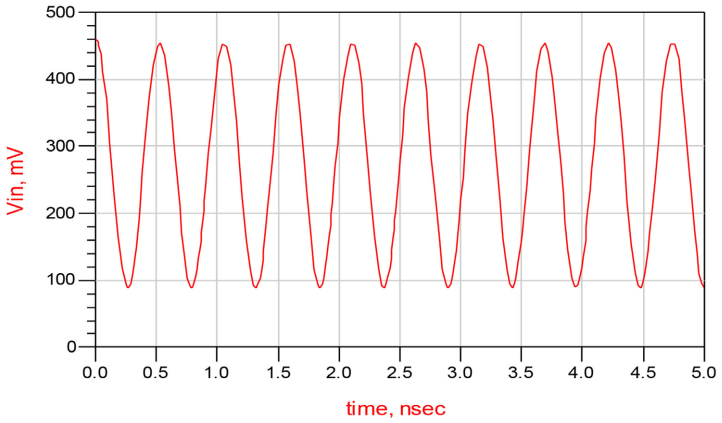


Figure 11. Input signal of cascoded circuit Vin(t).

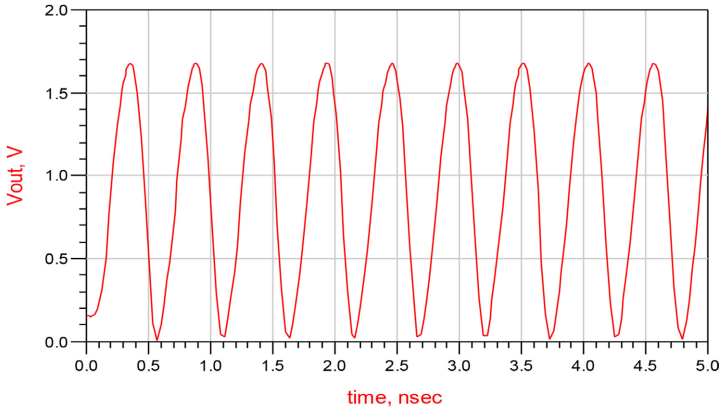


Figure 12. Output signal of cascoded circuit, Vout (t).

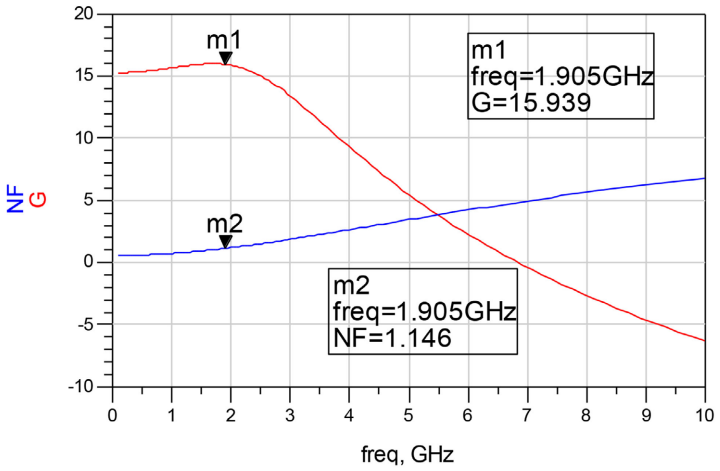


Figure 13. Gain G and noise figure NF of the cascoded LNA circuit.

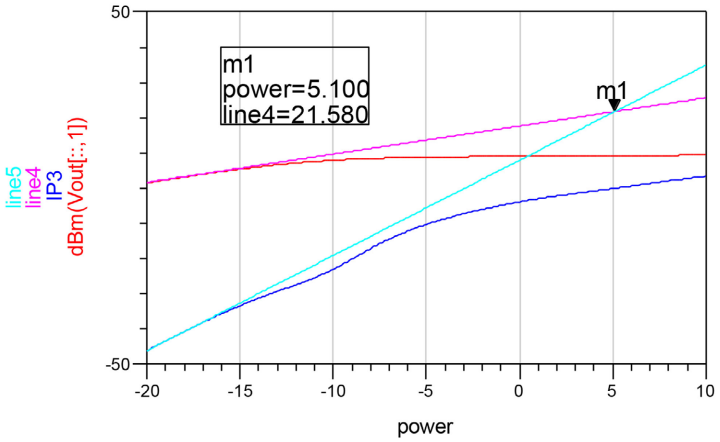
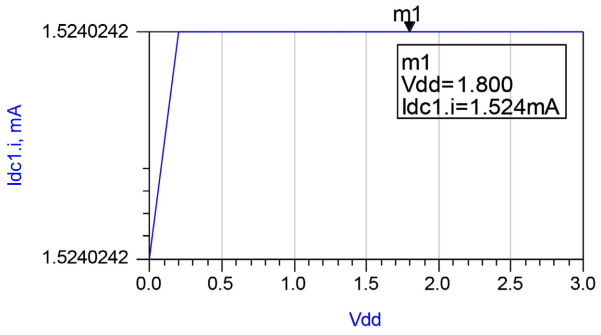


Figure 14. Linearity of the cascoded LNA circuit.



Values at bias point indicated by marker m1.
Move marker to update.

VDS	Device Power Consumption, Watts
1.800	0.003

Figure 15. Power consumption of the cascode LNA circuit (3 mW).

Table 1. Summary of results compared with typical values.

Reference	Technology	RF (GHz)	Gmax (dB)	NFmin (dB)	IIP3 (dBm)	P (mW)	Impedance (Ω)
Typical characteristics [10]	-	-	15	2	−10	-	50
LNA inductive degeneration	65 nm	0.5 - 6	14.7	0.5	2.4	3	50
LNA inductive degeneration (Cascoded)	**65 nm**	**0.5 - 5.4**	**16**	**1**	**5.1**	**3**	**50**

Table 2. Summary of results compared with recent works.

Reference (1st Author)	Year	Technology	Frequency (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	P (mW)	Vdd (V)	S/M
Proposed Work 2	**2023**	**65 nm**	**1.9 (0.5 - 6)**	**16**	**1.1**	**5.1**	**3**	**1.8**	**S**
Proposed Work 1	**2023**	**65 nm**	**1.9 (0.5 - 6)**	**13.7**	**1.6**	**2.4**	**3**	**1.8**	**S**
Typical [10]	-	-	-	15	2	-10	-	-	-
Didem Erol As [3]	2023	40 nm	2.4	11.5	3.38	-0.7	1	-	S
F. Gozalpour [4]	2023	180 nm	2.4	15.5	2.42	0.84	3.2	1.2	S
S.Nejadhasan [5]	2022	65 nm	2.32	15.4	2.3	−14.05	0.57	0.35	S
M. M. Farahani [6]	2023	180 nm	0.05 - 10.8	10.6	2.24	−2.3	6.12	1.8	Post-Layout
W. Liu [11]	2022	0.25 μm	4 - 15	17 - 21	1.6 - 2.1	<−7	266.5	-	Post-Layout
E. Salighe [7]	2023	0.18 μm	0.85 - 0.95	11.9	2.46	24	5.4	-	Post-Layout
G. Britton [8]	2022	28 nm	2*	~17*	~3*	~−1*	0.8	-	Post-Layout
S. Babak Hamidi [12]	2023	0.18 μm	2	31	3.6	−11	-	-	M
BM. Jafari [13]	2020	65 nm	1.4 - 4.5	25.7	2.7	10.1	0.87	0.8	S
M. Mudavath [14]	2020	45 nm	1-5	32.5	0.9	3.74	16.9	1.2	S

S: Simulation Result; M: Measurement Result; *: observed results from simulation figures.

5. Conclusions

The theoretical approach focuses on optimizing LNA voltage gain by introducing an impedance Z in series with the MOSFET's Drain and adjusting parameters based on characteristic equations. Managing noise figure involves addressing prevalent noise types, particularly $1/f$ noise linked to MOSFET parameters (W and L). Precision tuning of these parameters effectively mitigates this noise.

The initial simulation of a simple inductive degeneration circuit demonstrated the effectiveness of the adopted technique. This led to a subsequent transition towards an advanced cascode structure to consider linearity. The comparative simulation of the final circuit with other studies showcased the performance advantages of this approach, particularly in terms of gain-to-noise ratio (16/0.5 dB), linearity (5.1 dBm), and power consumption (3 mW). As a result, this pro-

posed design demonstrates applicability across a wide frequency band (0.5 - 6 GHz).

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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