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A 5 MS/s 12-Bit Successive Approximation Analog-to-Digital Converter

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Abstract

With the continuous development of science and technology, digital signal processing is more and more widely used in various fields. Among them, the analog-to-digital converter (ADC) is one of the key components to convert analog signals to digital signals. As a common type of ADC, 12-bit sequential approximation analog-to-digital converter (SAR ADC) has attracted extensive attention for its performance and application. This paper aims to conduct in-depth research and analysis of 12-bit SAR ADC to meet the growing demands of digital signal processing. This article designs a 12-bit, successive approximation analog-to-digital converter (SAR ADC) with a sampling rate of 5 MS/s. The overall circuit adopts a fully differential structure, with key modules including DAC capacitor array, comparator, and control logic. According to the DAC circuit in this paper, a fully differential capacitor DAC array structure is proposed to reduce the area of layout DAC. The comparator uses a digital dynamic comparator to improve the ADC conversion speed. The chip is designed based on the SMIC180 nm CMOS process. The simulation results show that when the sampling rate is 5 MS/s, the effective bit of SAR ADC is 11.92 bit, the SNR is 74.62 dB, and the SFDR is 89.24 dB.

Keywords

Successive Approximation, Analog-to-Digital Converter, Segmented, Capacitor Array

1. Introduction

Almost all signals in nature exist in analog form. However, digital signals, with their superior accuracy and processing speed far superior to analog signals, are more commonly used in electronic devices. Therefore, analog-to-digital conver-

ters (ADC) inevitably become bridges connecting the analog and digital domains [1]. Compared with other ADC structures, successive approximation analog-to-digital converters (SAR ADC) have the advantages of simplicity, low power consumption, small area, and ease of integration [2] [3]. As electronic products continue to develop towards ease of use, portability, and long endurance, SAR ADC with this characteristic are gradually showing significant advantages. Therefore, designing SAR ADC with high accuracy (greater than or equal to 12 bits) and medium speed (greater than or equal to 1 Ms/s) is of great significance [4] [5].

Since the linearity and area of the ADC are mainly related to the layout of the DAC, the SAR ADC needs a compact DAC array with good matching performance. [6] [7] propose different structures to save chip area, but increase circuit complexity. According to the DAC circuit in this paper, a fully differential capacitor DAC array structure is proposed. The comparator uses a digital dynamic comparator to improve the ADC conversion speed.

2. Basic Principles of the Circuit

The structure of the SAR ADC designed in this paper is shown in **Figure 1**. The main modules are comparator, analog-to-digital converter CDAC and SAR control logic. Its working principle is: the positive and negative input differential analog signal, through the DAC composed of capacitor arrays, completes the sampling of the input voltage value, and maintains the voltage value for a period of time for subsequent sampling and quantification processing, and at the same time clears the registers in the control logic zero. After the sampling process is finished, it enters the conversion stage. At this time, the conversion control signal will become high level, and the clock signal will set the highest position of the register to 1, so that the output of the register is 100...000. This digital quantity is converted by the D/A converter into corresponding analog voltage. The positive input and negative input are compared by the comparator. After the comparison is completed, the successive approximation logic will adjust the DAC output according to the comparison result, gradually reducing the difference between the input signal and the DAC output signal. This process will be repeated bit by bit., until all the bits are determined. Once all the bits are determined, the ADC completes the conversion of the analog signal to the digital

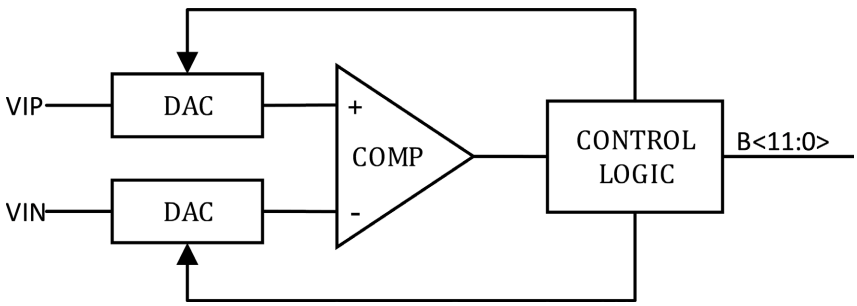

Figure 1. The structure of SAR ADC.

signal, and converts the input signal into a corresponding digital output.

3. Module Design

3.1. Capacitor Array Design

The SAR ADC is a typical high-resolution ADC, its capacitance array is the most important unit, and the conversion performance of this unit will directly determine the whole system conversion performance [8] [9]. The DAC has two main functions. One is to act as the sampling capacitor in the sampling circuit, and the other is to generate a reference voltage for comparison with the input voltage. The DAC converts the parallel or serial binary signal (comparator output signal) into a certain analog signal by using the reference voltage and approximates the input signal in turn.

The traditional capacitance array is shown in **Figure 2**, but as the number of ADC bits increases, the total capacitance required for a traditional binary DAC increases exponentially [10], An N-bit DAC requires a capacitance size of C total = 2^N * Cu, where Cu is the unit capacitance，so the total capacitance required for a 12-bit DAC is about 2048. In addition, the mismatch between capacitors is a new problem. Conventionally, the mismatch of each capacitor in DAC array becomes smaller with a larger unit capacitance or an advanced process, but it increases the cost [11] [12]. So, this traditional structure is not suitable for the SAR ADC designed in this paper.

In order to effectively reduce the number of capacitors in DAC, this article proposes a new DAC structure as shown in **Figure 3**. The total number of capacitors required by this structure is 286, which is 86% less than that of conventional capacitor arrays.

In this article, the 12-bit capacitor array is divided into high six bits and low six bits, and an additional 1 bit capacitor is added to achieve full scale quantization range. In a DAC capacitor array, if the low capacitance is equivalent to Ceq, the capacitance seen from the Ceq top plate needs to be equal to high. Therefore, the low six bits are composed of a unit capacitance and two times the unit capacitance in series and parallel to meet the binary relationship.

When sampling, the sampling switch is first closed, and the upper plates of the capacitor array at both positive and negative ends are connected to the common

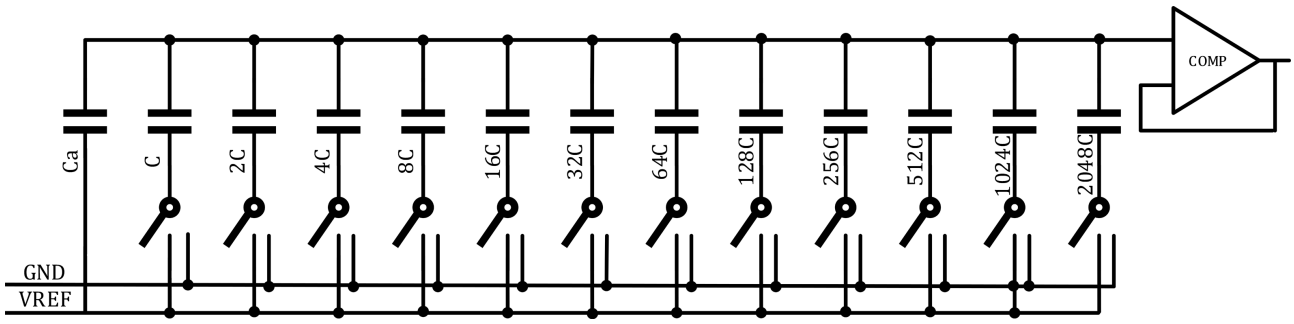

Figure 2. Traditional caps array.

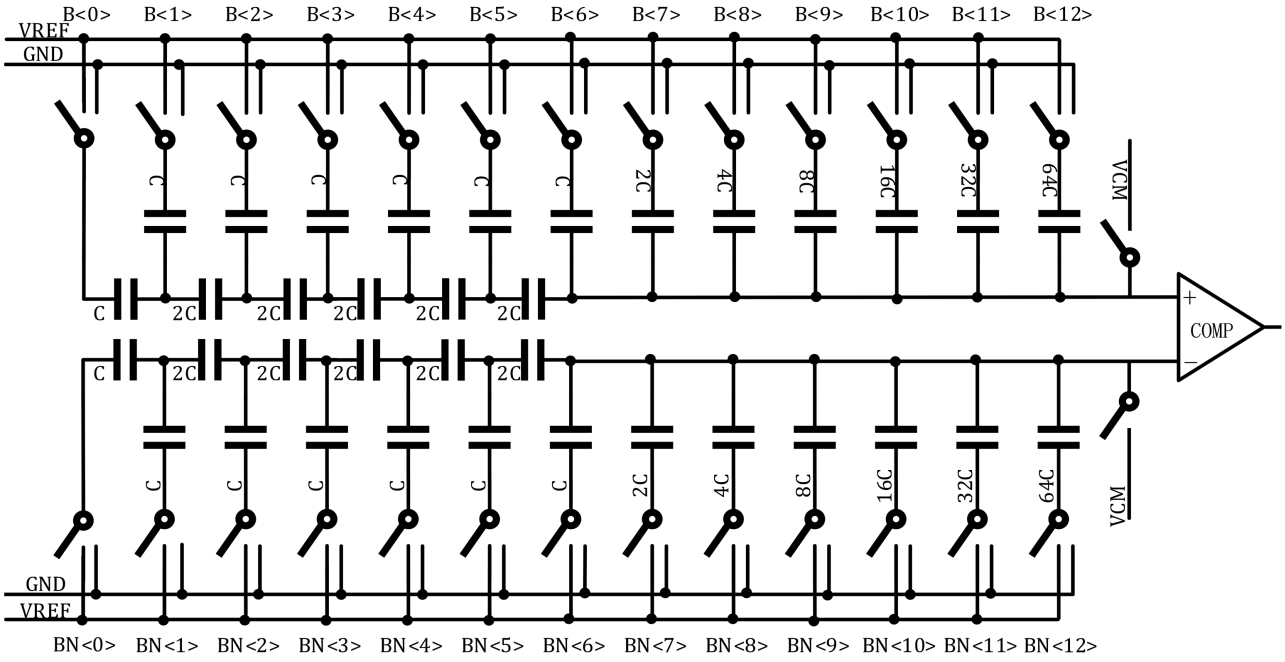

Figure 3. New DAC structure.

mode level VCM, while the lower plates are respectively connected to the input signals Vinn and Vinp, where Vinn and Vinp are

$$Vinn = Vin/2 + VCM$$

$$Vinp = -Vin/2 + VCM$$

$$Vin = Vinp - Vinn$$

At the first conversion, the numerical code is 1000_0000_0000, control the P-terminal voltage output Vpop = VCM − Vinp + 1/2Vref = −1/2Vin + 1/2Vref, and the N-terminal output voltage Vnup = VCM − Vinn + 1/2Vref = 1/2Vin + 1/2Vref. If the value is greater than 0, then Vinp >Vinn, the digital code is set to 1, otherwise set to 0, the purpose is to pull the larger value of the two down, pull the smaller value up, and finally both tend to common mode level VCM.

3.2. Comparator Design

In SAR ADC, the function of the comparator is to compare the output size of the positive and negative capacitive DAC, and then input the comparison result to the logic circuit successively to achieve the effect of controlling the DAC output voltage successively approximation. The structure of the comparator designed in this paper is shown in **Figure 4**.

When CLKN is at high level, M0 is turned off, M3 and M4 are on, V1 and V2 are output at low level. At this time, M5, M6, M9, M7, M8, M12 are all on, and R and S are output at high level. The COMPP result remains unchanged.

When CLK_COMP is at low level, M0 is on, and M3 and M4 are off. If Vp > Vn, the current flowing through M1 is less than the current flowing through M2. At this point, the voltage on V1 is less than the voltage on V2, and the R and S

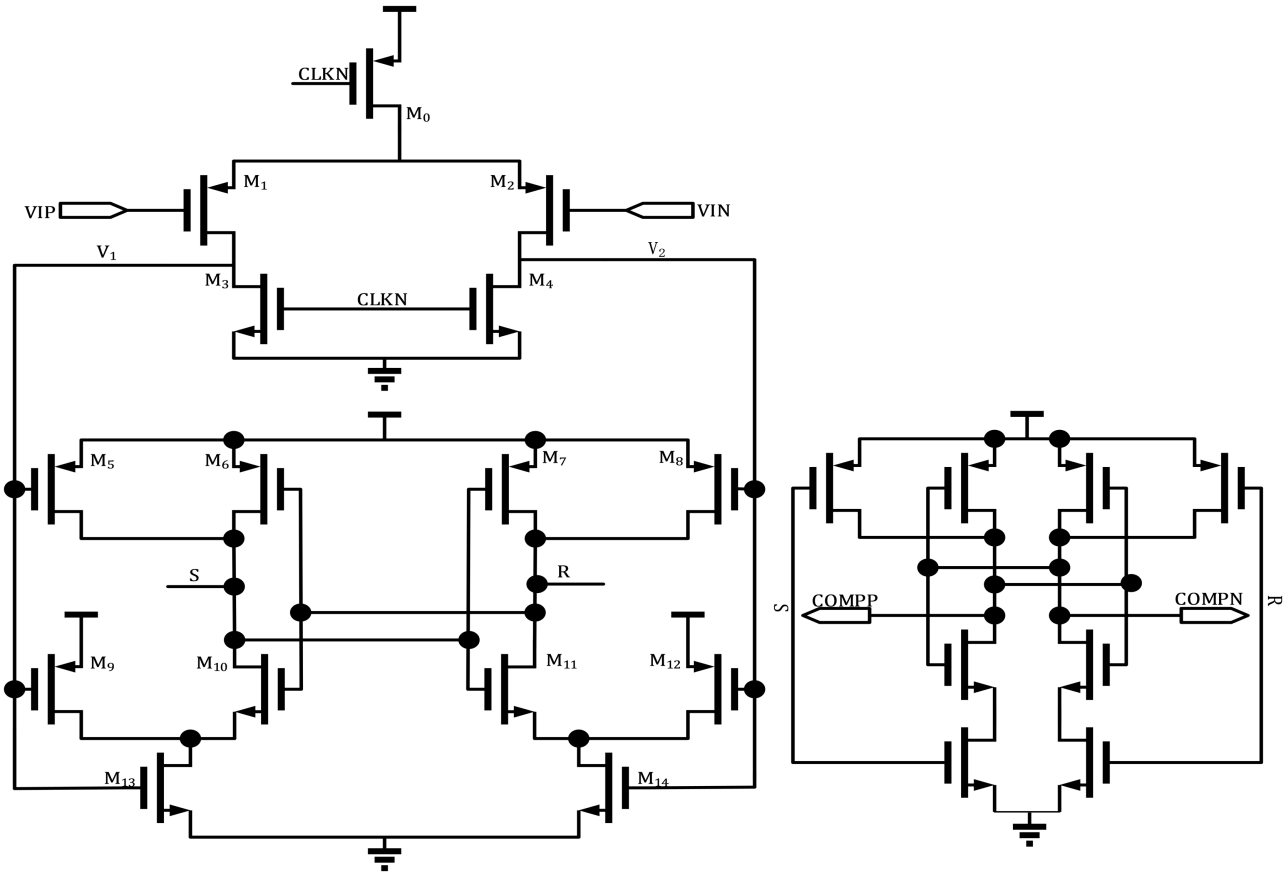

Figure 4. Comparator.

outputs are 0 and 1, respectively. After passing through the RS latch, the comparator outputs a low level. Similarly, if Vp < Vn, the comparator results in a high level.

3.3. Control Logic Design

SAR ADC completes the conversion of analog input value to digital output code through a successive approximation logic algorithm, which is implemented by the SAR ADC logic circuit. The SAR logic circuit diagram adopted in this paper is shown in **Figure 5**.

Among them, CONV is the conversion signal, COMPP is the comparator result, CLKB<12:0> is the clock of the flip-flop, provided by the clock generation circuit, the data register composed of 13 D flip-flops is used to store the comparator output result, and B<12:0> is the digital output code.

During the sampling phase, the CONV signal is low, and other modules other than the sampling hold circuit are in the reset state. At the end of sampling, the CONV becomes high and the ADC enters the conversion phase. When the comparator comparison is complete, if COMPP = 1, then when CLKB<12> arrives, the first D flip-flop in the data register is triggered, storing the comparator's first comparison result, that is B<12> = 1, while B<11> is set to 1. If COMPP = 0, then B<12> = 0, and B11 is 1. After the data is changed, the

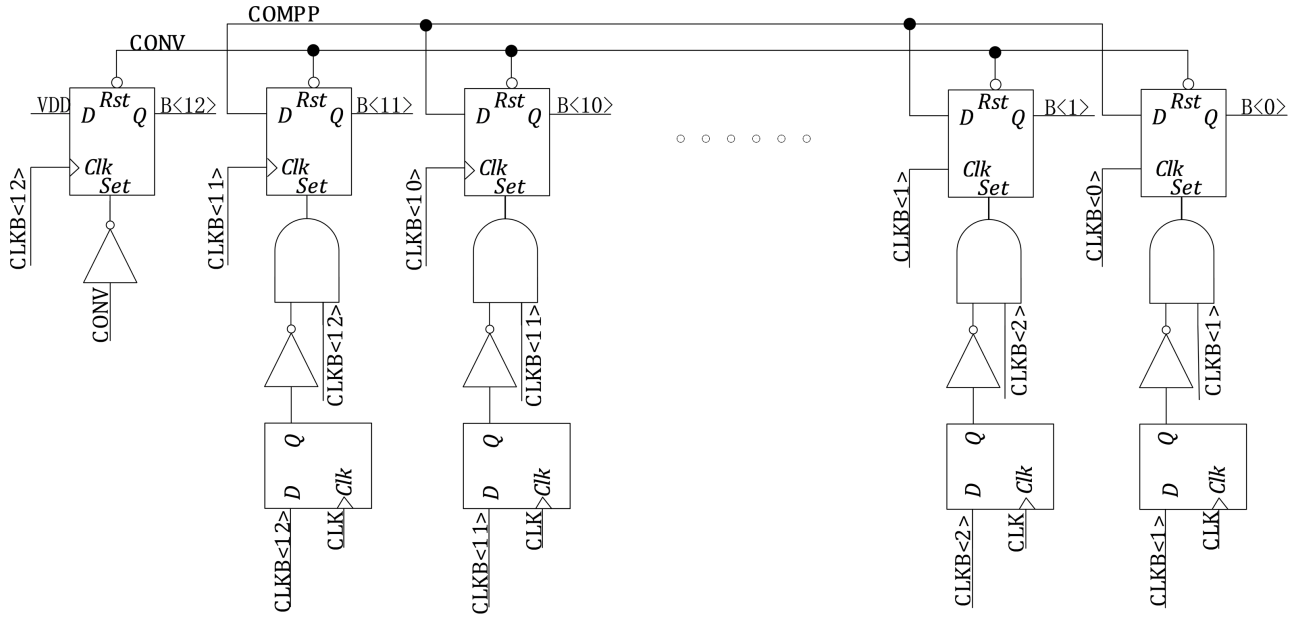

Figure 5. Control logic.

pad potential under the capacitor will continue to be controlled, and after the DAC and comparator, the digital code in the register will be updated, and so on until the 12 comparisons are completed.

4. Simulation Result

Based on SMIC 180 nm CMOS process, SPECTRE in Cadence software is used for SAR ADC dynamic simulation. Set the clock signal to 5 MHz, the reference voltage VREF to 1.8 V, the sampling period to 5, the sampling number to 512 points, and the input sine wave signal frequency to 48.828125 KHZ. After connecting the output digital code to the ideal DAC, the simulation results are obtained as shown in the figure below. **Figure 6** is the output of ideal DAC, **Figure 7** is the output waveform of capacitive array DAC, and **Figure 8** is the FFT spectrum diagram.

The design results of this paper are compared with the results of references, as shown in **Table 1**. Among them, [13] has the same sampling rate as the one designed in this article, but the resolution is lower than that in this article.

5. Summary and Prospect

In this paper, a 12-bit successive approximation analog-to-digital converter is designed, which covers the main modules of SADR ADC. By analyzing the whole circuit, a new capacitor array structure is proposed, which can improve the capacitor matching and reduce the capacitor area greatly. The whole circuit adopts SMIC 180 nm process, and cadence software is used for simulation and verification. According to the results, the 12-bit resolution can be reached.

For higher accuracy of the ADC, however, the influence of the capacitor mismatch are becoming ever more obvious, so the design of capacitor mismatch

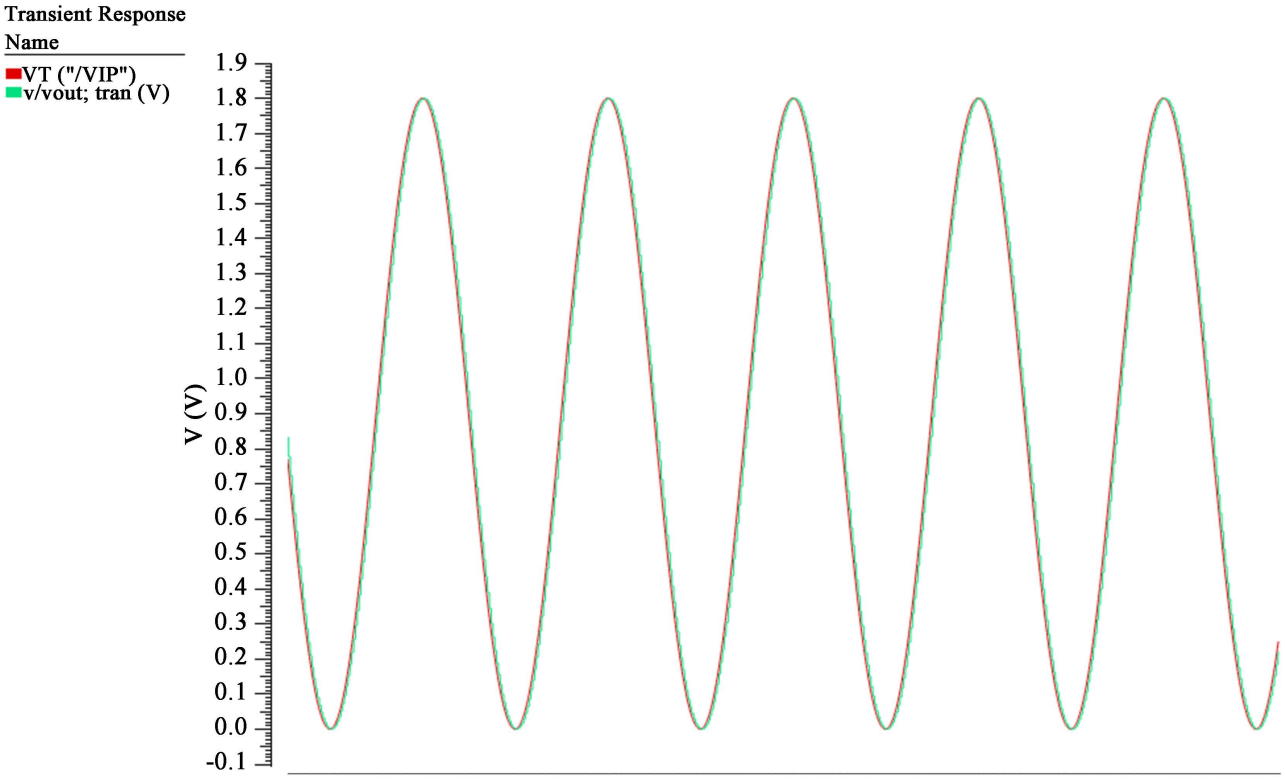

Figure 6. ADC vout.

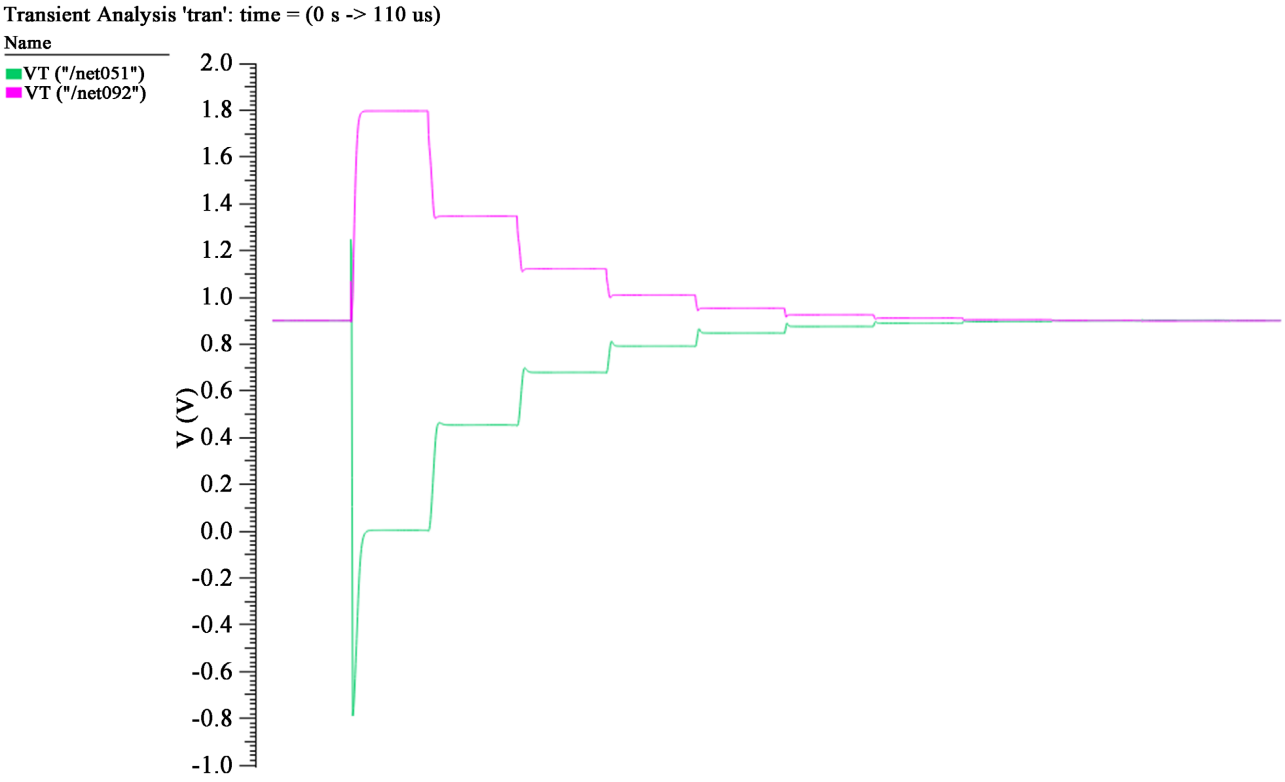

Figure 7. Capacitive array DAC.

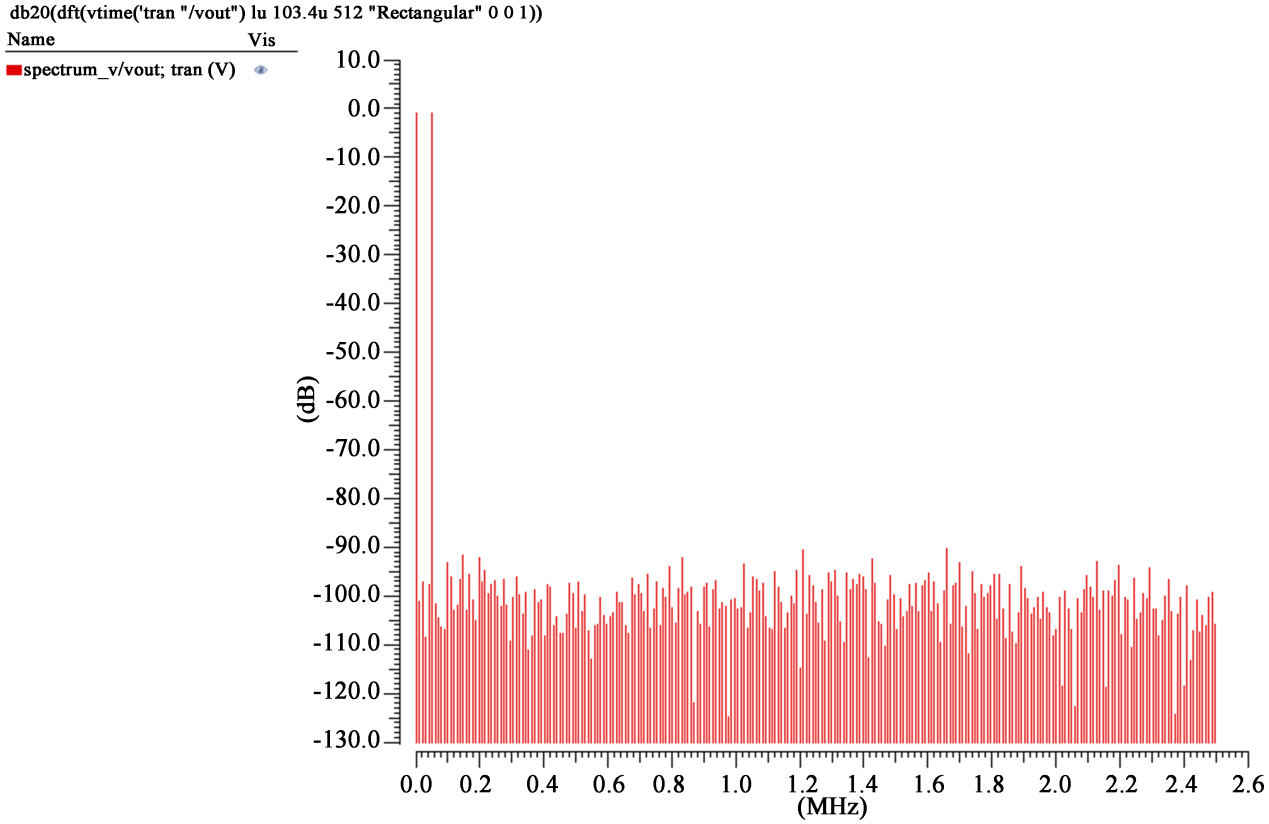

Figure 8. FFT spectrum diagram.

Table 1. The results of the comparison.

Specification (Unit)	[10]	[12]	[13]	This work
Process (nm)	130	180	180	180
Sampling rate (MS/s)	0.001	10	5	5
Supply voltage (V)	1	1.8	1.8	1.8
Resolution (bit)	12	12	10	12
ENOB (bit)	10.47	9.42	9.13	11.92
SFDR (dB)	78.5	67.6	72.2	89.2

calibration method is necessary. Secondly, with the rapid development of electronic products and communication systems, the sampling rate of 5 MS/s often fails to meet the actual application needs, and the sampling speed can be improved by time interweaving technology.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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