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Multi-Channel Low-Noise Analog Front Design

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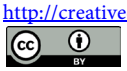

Abstract

With the development of digital nuclear pulse processing technology, the requirements for the analog front-end circuit of digital energy spectrometers are getting higher and higher. Not only need to reduce the noise caused by the device as much as possible, but also need to meet the needs of multi-channel data acquisition. This article based on VGA (Variable Gain Amplifier) has designed a multi-channel low-noise analog front-end circuit to meet the functional requirements of the energy spectrometer while reducing the signal transmission in the analog front-end circuit as much as possible. The circuit noise is strictly controlled to ensure the signal-to-noise ratio of signal transmission. AD9255 is used for waveform digitization, and the input range is 100 μV-2 V_{PP}. After testing, the circuit has a wider gain range and better noise control. Input 100 μV_{pp} signal when the analog front-end gain is 24 dB, and its signal-to-noise ratio can reach 1:1.

Subject Areas

Electric Engineering, Nuclear Engineering

Keywords

Low Noise, Multi-Channel, VGA

1. Introduction

With the continuous development of digital nuclear pulse signal analysis technology, the requirements for precision in nuclear detection are getting higher and higher [1] [2]. At the same time, as the collection system needs to realize more and more functions, the demand for multi-channel is increasing [3]. The analog front-ends currently on the market cannot balance low noise and multi-channels. In response to the above requirements, this article designs a four-channel low-noise analog front end for the digital nuclear pulse signal analysis

system. Compared with multi-board card acquisition, the system reduces the complexity of communication between boards, has a higher degree of integration, and improves system stability and anti-interference ability.

2. Overall Design

The analog front-end circuit mainly includes input buffer, low-pass filtering, gain adjustment, DC offset adjustment and ADC The circuit design block diagram is shown in Figure 1.

2.1. Input Buffering and Low-Pass Filtering

The input buffer circuit is used to achieve impedance matching between the preamplifier and the analog front end [4], and at the same time to amplify the power of the input signal to improve the signal driving capability [5]. Use LMH6626 operational amplifier as the system input buffer amplifier for input impedance matching and power amplification. The LMH6626 has a bandwidth of 1.5 GHz, an input voltage noise density of 0.92 nV/√Hz, and an input offset voltage of 700 μV. The high bandwidth and low noise characteristics of this operational amplifier are suitable for input buffers.

The LFCV-45+ low-pass filter is used to filter out the input high-frequency interference and white noise. LFCV-45+ is a 7-order filter based on LTCC with a cut-off frequency of 45 MHz. The stop band suppression can reach 50 dB.

2.2. Gain Adjustment Circuit

Using AD8264 VGA as the main amplifier, AD8264 is a 4-channel, linear dB variable gain amplifier, each channel integrates a preamplifier and differential output buffer, the gain range is 24 dB, the large signal bandwidth reaches 80 MHz, the input voltage The noise density is 2.3 nV/√Hz, and the input current noise density is 2 pA/√Hz. The differential output buffer with common mode and offset adjustment can be directly coupled with the high-speed ADC. The internal structure of AD8264 is shown as in Figure 2.

2.3. DC Offset Adjustment Circuit

Using AD5671 DAC as hardware gain and DC offset adjustment drive, AD5671 is 8 passways, 12Bit voltage output type digital-to-analog converter. Built-in 2.5 V reference voltage source, temperature drift is lower than 2 ppm/˚C. AD5671 adopts I^2C interface to carry on communication, can carry on hardware gain and

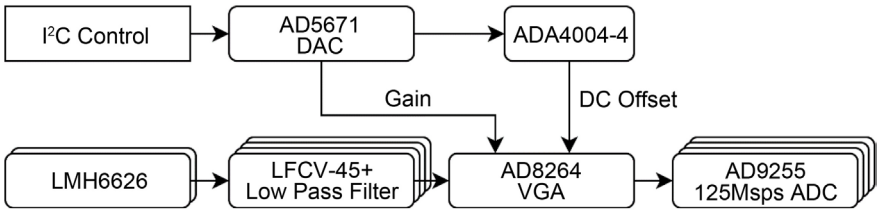

Figure 1. Block diagram of overall design.

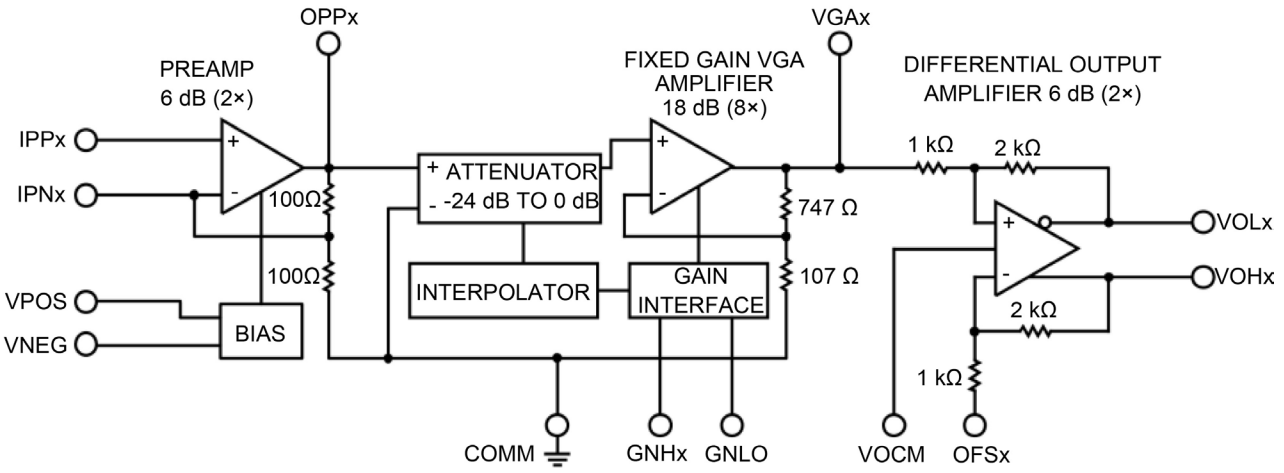

Figure 2. AD8264 internal structure.

DC offset adjustment through FPGA.

Using ADA4004-4 operational amplifier as the DC offset adjustment buffer, the ADA4004-4 integrates a 4-channel operational amplifier, the input voltage noise density of each channel reaches 1.8 nV/√Hz, the slew rate is 2.7 V/μs, and the temperature drift is controlled within 0.7 μV/˚C, very suitable for use as a reference voltage source output buffer. Each channel of ADA4004-4 is connected to the DAC at the positive input terminal, and the reverse input terminal is connected to the DAC output reference source to form a differential output and eliminate common mode noise [6]. The output end is connected to the reverse end of the AD8264 differential output buffer operational amplifier to realize positive and negative bipolar DC offset adjustment.

2.4. ADC and Differential Anti-Aliasing Filter

Select AD9255 14bit 125Msps ADC to realize the conversion from analog to digital, AD9255 SNR reaches 78.3dBFS@70MHz, SFDR reaches 93dBc@70MHz, uses parallel port for data transmission, standard SPI interface for functional configuration, its internal structure is shown in Figure 3 shown.

Since the performance of the ADC is affected by the frequency of the input signal, the analog bandwidth should be limited while meeting the sampling frequency requirements, and the Nyquist sampling theorem should also be met to ensure distortion-free reconstruction of the signal [7]. The design of the fully differential anti-aliasing filter used in this article is shown in Figure 4.

Resistors $R1$, $R2$ and capacitor $C1$ together form a fully differential anti-aliasing filter, and its bandwidth calculation is shown in Equation (1).

$$F = \frac{1}{2\pi(R1+R2)\times C1} \tag{1}$$

Among them, F is the filter bandwidth, in Hz; $C1$ is the differential filter capacitor, in F; in the filter design process, the value of $C1$ should be greater than or equal to 10 times the sampling capacitor of the analog-to-digital converter. $R1$

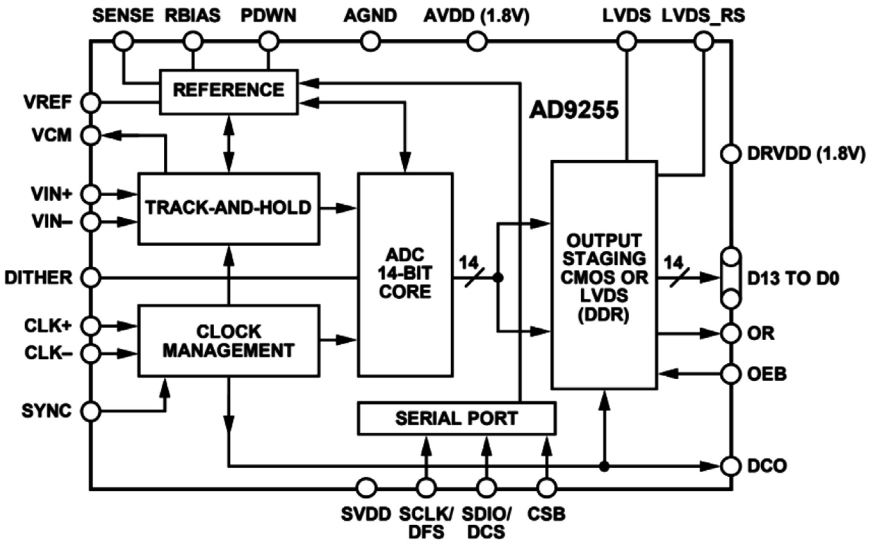

Figure 3. AD9255 internal structure.

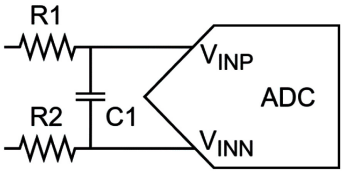

Figure 4. Fully differential anti-aliasing filter.

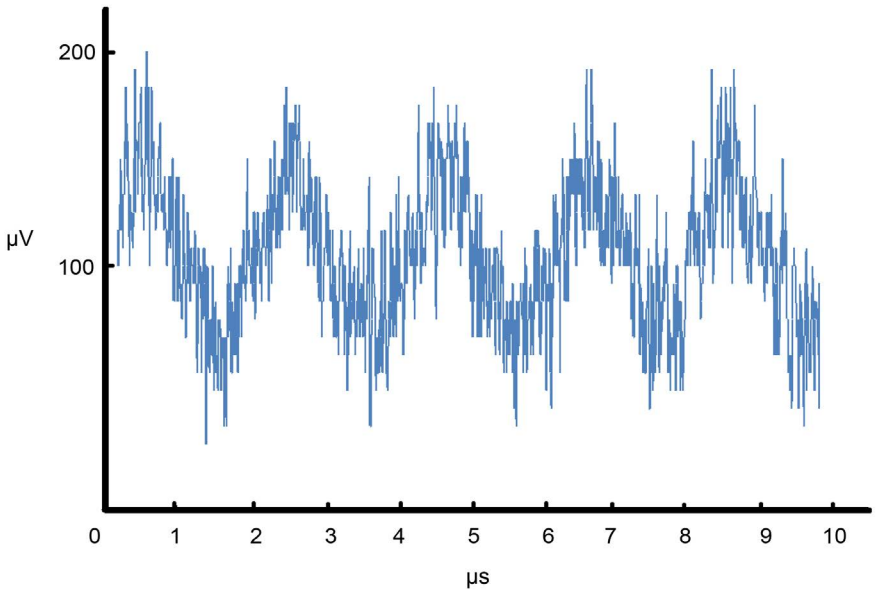

Figure 5. Input 500 kHz 100 μV_{PP} sinusoidal waveform when the circuit gain is 24 dB.

and $R2$ are isolation resistances, the unit is Ω; the choice of isolation resistance needs to balance the stability and distortion of the design, which are generally ohmic. This text chooses $R1 = R2 = 20\ \Omega$, $C1 = 40$ pF, the bandwidth of this filter is calculated as 100 MHz.

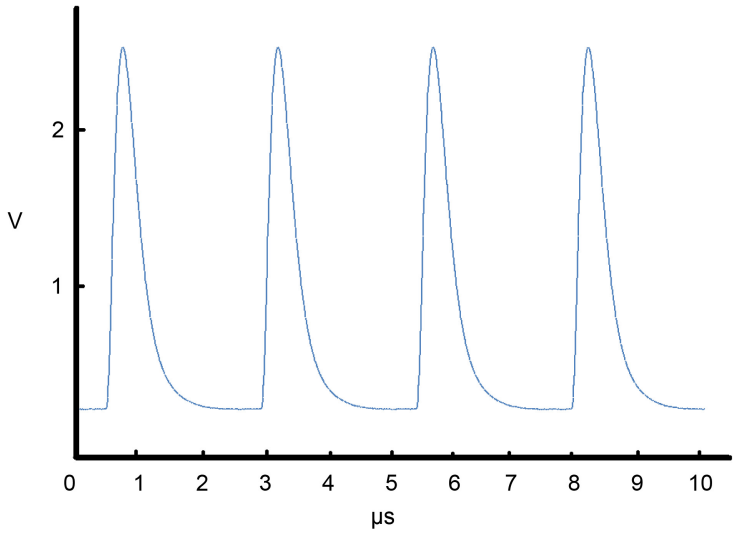

Figure 6. Input 500 kHz 2 V_{PP} Gamma waveform when the circuit gain is 0 Db.

3. Test

Use Suin TFG6300 signal generator to carry on the minimum resolution ability test, adjust the circuit gain to 24 dB, input 500 kHz, 100 μV_{PP} sine wave, the output signal is shown as in Figure 5.

Use RIGOL DG992 to carry on the nuclear pulse signal test, adjust the circuit gain to 0 dB, input 500 kHz, 2 V_{PP} Gamma signal, the output signal is shown as in Figure 6.

It can be seen from Figure 5 and Figure 6 that the circuit structure takes into account both gain and noise, and has a wider gain adjustment range while ensuring the signal-to-noise ratio of small signals.

4. Conclusion

This paper designs a multi-channel analog front-end circuit for a precision multi-channel pulse amplitude analyzer. After testing, it can clearly distinguish 100 μV_{PP} signals when the gain is 16, and the input range can reach up to 2 V_{PP}, which has a wide signal input range, can meet the input requirements of different detectors. The circuit has a high input bandwidth, can be adapted to ADC with different sampling rates, and can be applied to occasions with different time resolution accuracy.

Conflicts of Interest

The author declares no conflicts of interest regarding the publication of this paper.

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