Journal of Power and Energy Engineering, 2023, 11, 1-16
https://www.scirp.org/journal/jpee
ISSN Online: 2327-5901
ISSN Print: 2327-588X

Design and Implementation of Smart Power Voltage and Frequency Synchroniser in Power Distribution System

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How to cite this paper: Prah, I.K.M. and Attachie, J.C. (2023) Design and Implementation of Smart Power Voltage and Frequency Synchroniser in Power Distribution System. *Journal of Power and Energy Engineering*, **11**, 1-16.
https://doi.org/10.4236/jpee.2023.114001

Received: February 9, 2023
Accepted: April 18, 2023
Published: April 21, 2023

Abstract

Voltage and frequency are usually considered and assessed independently in the design and operation of electrical networks. However, these two are linked. Each and every malfunctioning electrical system has an impact on both voltage and frequency. This paper presents the opportunity for monitoring the distributed electrical energy by means of a system that monitors, controls, and provides a breakpoint based on high or low voltage and frequency tripping mechanism that avoids any damage to the load. The designed system comprised a switch mode power supply (SMPS), a direct digital synthesizer (DDS), and PIC16F876A microcontroller techniques for stable voltage and frequency outputs. Proteus design suite version 8.11 software and Benchcope SDS1102CN were used for modeling and simulation. The hardware prototype was implemented at a telecom cell site for data capturing and analysis. Test results showed that the implementation of the prototype provided stable and constant outputs of 222 V/50 Hz and 112 V/60 Hz which constituted 99% and 99.8% efficiency for voltage and frequency performance respectively. The paper also discusses different technologies that can be adopted by the system to mitigate voltage and frequency effects on customer appliances.

Keywords

Switch Mode Power Supply, Direct Digital Synthesis, Pulse Width Modulation, H-Bridge Mosfet, Microcontroller, Filtering, and Rectification

1. Introduction

Power quality issues in the distribution system are typically manifested as voltage, current, or frequency irregularities that cause customer equipment to mal-

function or fail. Due to the output loss, this frequently causes financial losses in commercial and industrial processes. There are various power-producing units connected to the grid to supply power to the load in order to meet commercial and industrial demand [1]. By maintaining specific voltage and frequency ranges, these generation units must deliver power to meet grid requirements [2]. Moreover, efforts are being made to use a traditional automatic voltage regulator to adjust variations in the energy supply voltage. The majority of AVRs on the market today attempt to control the input voltage within a certain range. This creates a mostly unstable or fluctuating mains input voltage into a reasonably steady voltage, although it does little to nothing to deal with small voltage variations, spikes, and frequency deviations of about ±5% for100%.

In [3], the authors developed a system that utilized a step-down transformer and zero-crossing detector to continuously measure the mains supply voltage level and frequency. The supply voltage was scaled by a factor to a level safe for measurement using an ADC through an 8051-based microcontroller by the step-down transformer with known transformation ratio. The output pulses from the zero-crossing detector were timed to match the frequency of the main supply. The microcontroller measured the pulse duration and displayed it along with the voltage level on an LCD. The microcontroller used a relay to activate a lamp indicator each time the mains supply voltage and frequency were outside of tolerance. In [4], the author implemented high performance voltage stabilizer which helps to detect inappropriate voltage levels and correct them to produce a reasonably stable output. It is composed of switching transistors and relays to control the power provided to ac loads, and it has LEDs for indicating the state of the system, 240 - 220 VAC/120 - 110 VAC switch, and voltmeter displaying load voltage, heatsink, and fans for cooling the system. The system protects electrical equipment and machine against voltage surge.

This paper focuses on the problems associated with voltage and frequency instabilities in the power distribution system by utilizing modern technologies with the ability to deliver power in more efficient ways and respond to wide-ranging conditions and events. A smart power voltage and frequency synchroniser is therefore needed to optimise the supply voltage and frequency from lower or higher to normal 220/110VAC and 50 Hz/60 Hz respectively.

2. Design Theories and Principles

2.1. SMPS Transformer Design

Due to the increasingly complex requirements of contemporary electronics designs, designing magnetic components for SMPS can be difficult. There are various steps in the design process. A major decision that needs to be prioritized is choosing a core type and size. The essential criteria for selecting the core size are the flux density, the maximum output power, power transformer, switching topology, frequency, and core materials with a permeability within 2500 [5]. There are varieties of core types readily available in the market. However, the E and EE

cores are the most used since it is less expensive compared to other core types available. The core size is based on the number of turns and output power. It is preferable to choose a larger gap before a larger core size, because heat radiation is reduced, losses are reduced, and parasitic capacitances are reduced in a smaller core.

The relation for flux density is written in the form:

$$B_{\max} = \frac{A_L \times N \times I_{p.\text{peak}}}{A_{\text{core}}} \tag{1}$$

The transformer output power is determined by the formula:

$$P_O = 0.5 \times L_p \times I_{p.\text{peak}}^2 \times F_S \tag{2}$$

Rearranging Equation (2) the peak current is expressed as:

$$I_{\text{peak}} = \sqrt{\frac{2 \times P_O}{L_P \times F_S}} \tag{3}$$

The variables involved in estimating the appropriate core size for power output is given in the relation:

$$A_W A_{\text{core}} = \frac{P_O \times 10^4}{K_f \times K_u \times B_{\max} \times J \times F_S} \tag{4}$$

The number of primary turns is expressed as

$$N_{\text{primary}} = \frac{V_{\min(\max)} \times 10^8}{4 \times F_S \times B_{\max} \times A_{\text{core}}} \tag{5}$$

The secondary/primary turns ratio is given in the form:

$$\frac{N_P}{N_S} = \frac{V_P}{V_S} \tag{6}$$

The primary inductance is calculated by the formula:

$$L_P = \frac{\eta \times \left(V_{\min} \times D_{\max}\right)^2}{2 \times P_O \times F_S} \tag{7}$$

2.2. Direct Digital Synthesis

Across a large frequency range, direct digital synthesis (DDS) is a frequency-accurate approach. It is a method for generating a time-varying digital signal, then converting it to an analog sine wave waveform [6]. In DDS, instantaneous voltage samples of a waveform reference are taken at fixed intervals, digitized, and stored in Microcontroller memory. To reproduce the waveform, the digitized voltage samples are read from the Microcontroller memory and fed to a DAC at the frequency they were originally sampled at. The DAC output is filtered to produce the original waveform. The microcontroller dual PWM modules were used as a DAC for this purpose. Once set up, the PWM module will generate square waves whose duty cycle is set by a value.

The waveform, number of samples, and interval must first be decided on. In

the case of this paper, a half-cycle sine wave was used. The sampling interval chosen is 50 μs (20 kHz). Two different sets of samples were taken and stored. One set of samples is for generating 110 V, 60 Hz AC voltage while the other is for 220 V, 50 Hz AC voltage. The 110 V, 60 Hz samples are 42 in number while the 220 V, 50 Hz samples are 40. Figure 1 illustrates the DDS process.

A half-cycle sine wave is sampled at fixed intervals. At each sample, the instantaneous volage of the waveform with reference to a peak voltage (V_{peak}) was calculated using the formula:

$$Y_{\text{value}} = V_{\text{peak}} \times \sin\left(\frac{\text{Sample point}}{\text{Number of sample point}} \times 180^{\circ}\right) \tag{8}$$

2.3. Pulse Width Modulation

Based on advanced technology in solid-state power electronic devices and microprocessors, numerous pulse-width modulation (PWM) approaches have been created for a variety of industrial applications [7]. The primary goals of PWM are output voltage control and output voltage harmonic content reduction. There are a variety of PWM techniques, including single pulse width modulation, multiple pulse width modulation, phase displacement control, sine wave, harmonic injection, space vector, and hysteresis modulation [8]. However, in this paper, a microcontroller-based method is adopted. Microcontroller PIC16F876A has an inbuilt PWM module that is set up by programming and configuring certain registers linked to the PWM hardware module. The microcontroller generates the pulse width signal, then a digital logic is employed to create a phase shift that will be used to drive all inputs of the H-Bridge.

3. Proposed Methodology

3.1. Design Concept and Criteria

The design and implementation of the proposed smart power voltage and frequency synchroniser in the power distribution system started with mapping out the necessary circuit blocks and their interconnections. The resulting block diagram is shown in Figure 2.

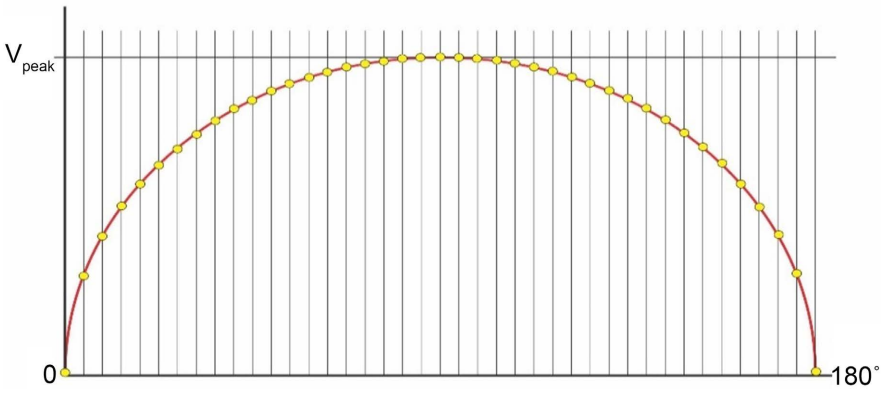

Figure 1. Illustration of the DDS process.

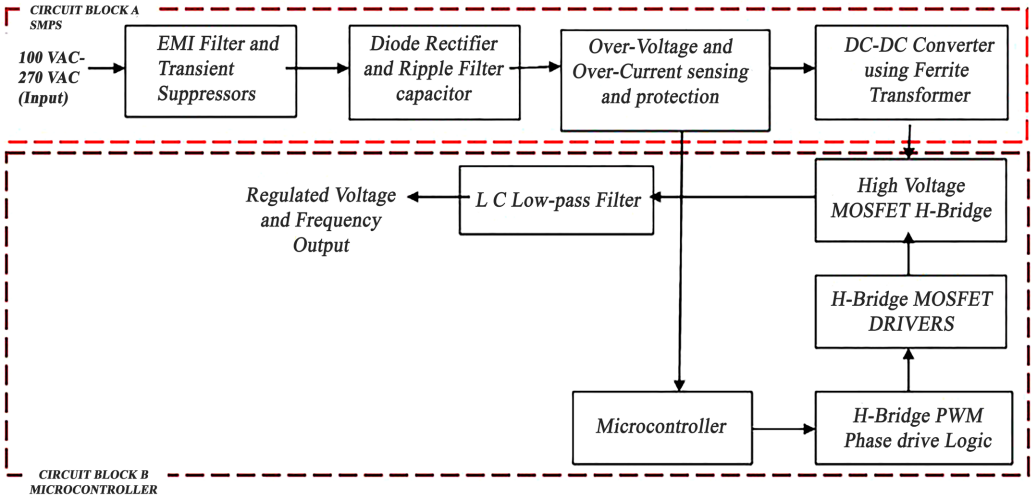

Figure 2. Block diagram of proposed design.

From Figure 2, unregulated mains voltage within the range of 100 V AC - 270 V AC enters the system. Electromagnetic interference (EMI) filter and Transient suppressors minimize EMI noise going in and out of the system. A diode rectifier converts the AC main voltage to DC and filters it through an electrolytic capacitor. The resulting voltage output is within the range of 141 V to 381 V DC. It is fed to a DC-to-DC converter through over voltage and over current sensing protection circuit. The protection circuits shut down the system when the current and voltage levels are out of range and also provide feedback to the DC-DC converter for a closed-loop operation. Output from the DC-to-DC converter is a clean 325 V DC power. This is connected to an H-bridge circuit built around high voltage MOSFETs. The H-bridge MOSFET configuration is used to convert the high voltage DC to AC using PWM. The microcontroller is responsible for generating the appropriate PWM signal used to drive the H-bridge. The microcontroller uses Direct Digital Synthesis to generate a Pulse Width Modulated Sine wave signal. This signal is highly stable in frequency and has a fixed amplitude. Combination logic is used to derive a complementary drive signal from the microcontroller generated PWM. The complementary drive signal is fed to the H-bridge MOSFET drivers which buffer the signals to drive the H-bridge MOSFETs. The H-bridge voltage output is fed through a single pole LC filter which removes all high-frequency noise and delivers a clean and stable voltage output to power devices and loads.

3.2. Power System Parameters

The design and construction of the circuit in circuit block A is a key component in the operation of this research work. This circuit utilized the half-bridge topology and is responsible for ensuring a stable output DC voltage with fluctuating or unstable AC input voltage. It takes in an AC voltage within the range of 100 V to 270 V and produces a stable regulated 310 V DC output. The design specification of the SMPS is shown in Table 1.

Table 1. Power parameters for the half-bridge SMPS.

Parameters	Symbol	Value	Unit
Output Power	W	200	Watt
Voltage Input Range	VAC	100 - 270	Volt
Voltage Output Range	VDC	310	Volt
Switching Frequency	kHz	100	kilohertz
Efficiency	η	80	%

3.3. Half-Bridge Topology

Taking into consideration the above specification, the half-bridge SMPS topology was used. The half-bridge topology is normally used for the power output of 100 W to 500 W. It also presents minimal stress on switching MOSFETs. In this paper, IR2110 was used for the MOSFET switch driver. Figure 3 shows the topology for the design.

In the half-bridge topology, two power switches SW1 and SW2 are turned ON and OFF alternately by a controller labeled Control in Figure 3. The power switches are connected in series with one terminal of a high-frequency transformer T joined to the midpoint of the switches. The other terminal of T is connected to the midpoint of a series connection of Capacitors C1 and C2. The arrangement of C1 and C2 places the midpoint at one-half the supply voltage Vin. Thus, only half of the voltage supplied appears across the primary winding of Transformer T. In operation, when the controller turns on power switch SW1, current flows from the +ve terminal of Vin through the Transformer T and to the midpoint of C1 C2. After a half cycle, the controller turns off SW1 and then turns on SW2. When SW2 is turned on, current flows in the opposite direction from the midpoint of C1C2 to the –ve terminal of Vin. This causes an alternating voltage across the primary of the high-frequency transformer causing a voltage to appear on the secondary. The output voltage level of the transformer is dependent on the primary turns n1 and secondary turns n2 ratio. Diode bridge Ds on the output rectifies the voltage while in inductor L0 and Capacitor Cout filters the rectified voltage to a clean DC.

3.4. Research Flow Chart

The flowchart presented in Figure 4 summarizes the proposed methodology for the design and implementation process.

3.5. Design Criteria Circuits

Figure 5 shows the complete schematic diagram of the design criteria circuits for the smart power voltage and frequency synchroiser in power distribution system. The schematic diagram presents the underlying circuitry and interconnections of the earlier mentioned circuit models and other enabling components.

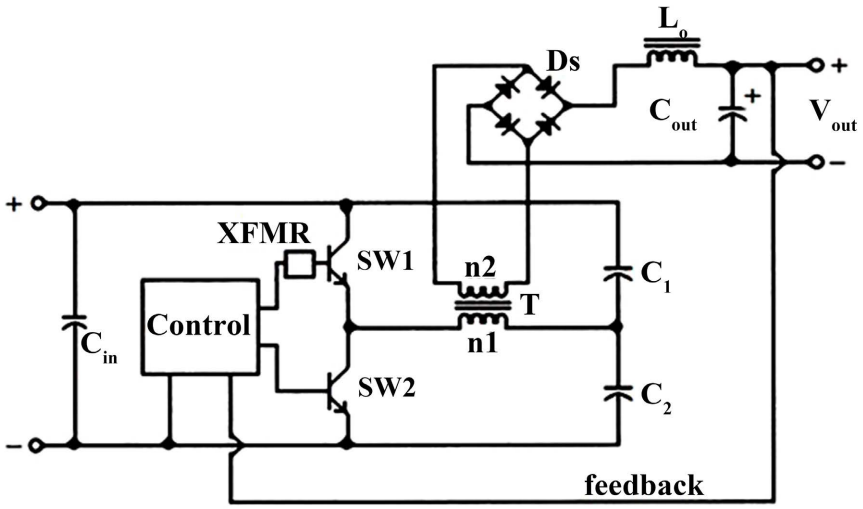

Figure 3. Half-bridge topology.

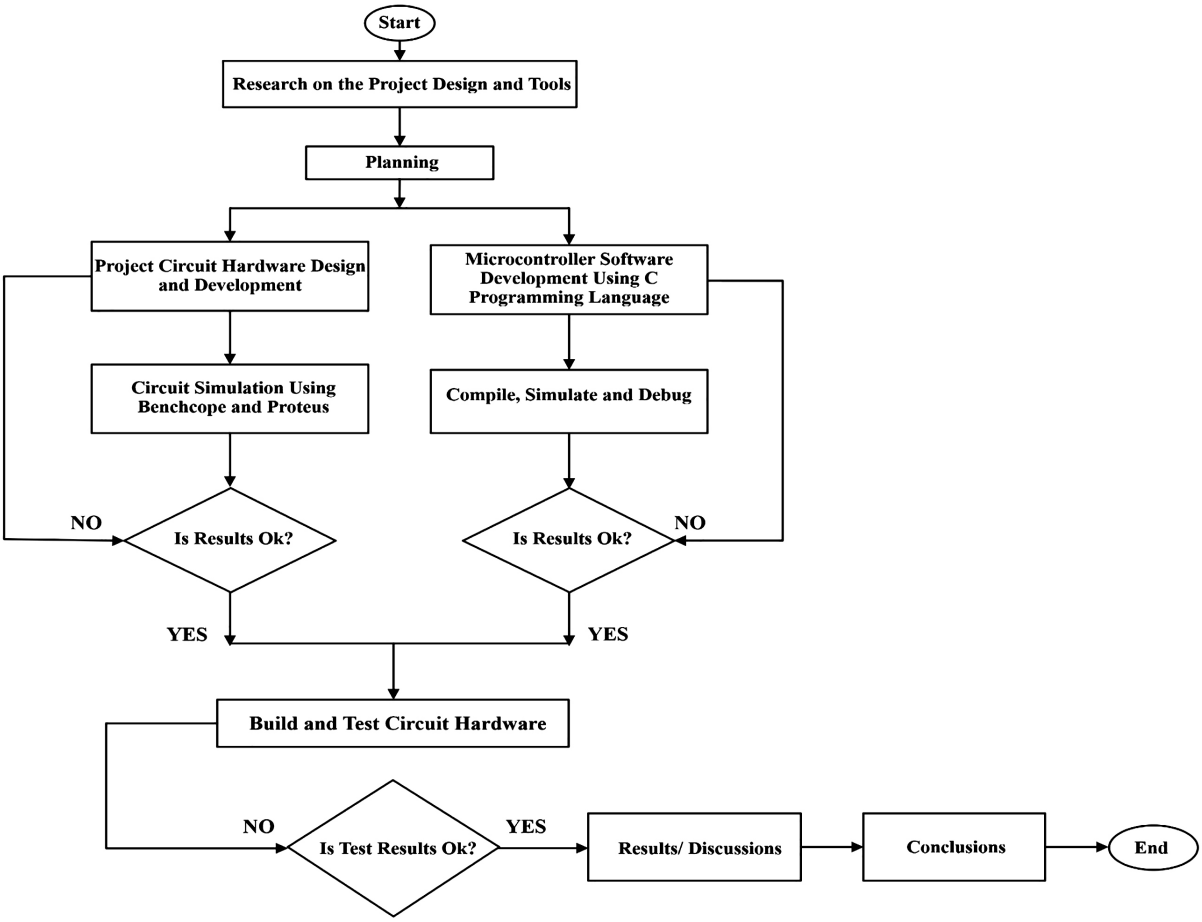

Figure 4. Proposed flow chart for the research.

4. Results and Discussions

4.1. 220 V/50 Hz Simulation

The image in Figure 6 shows the circuit simulation of 220 V/50 Hz AC input in

Proteus. From the simulation results, it was realised that when SW1 is opened the LCD display the visual output and input mains voltage and frequency respectively as instructed.

The drive signals fed to each of the gates of the MOSFETs in the H-bridge is shown in Figure 7. Waveforms D and C are the SPWM signals which drive the

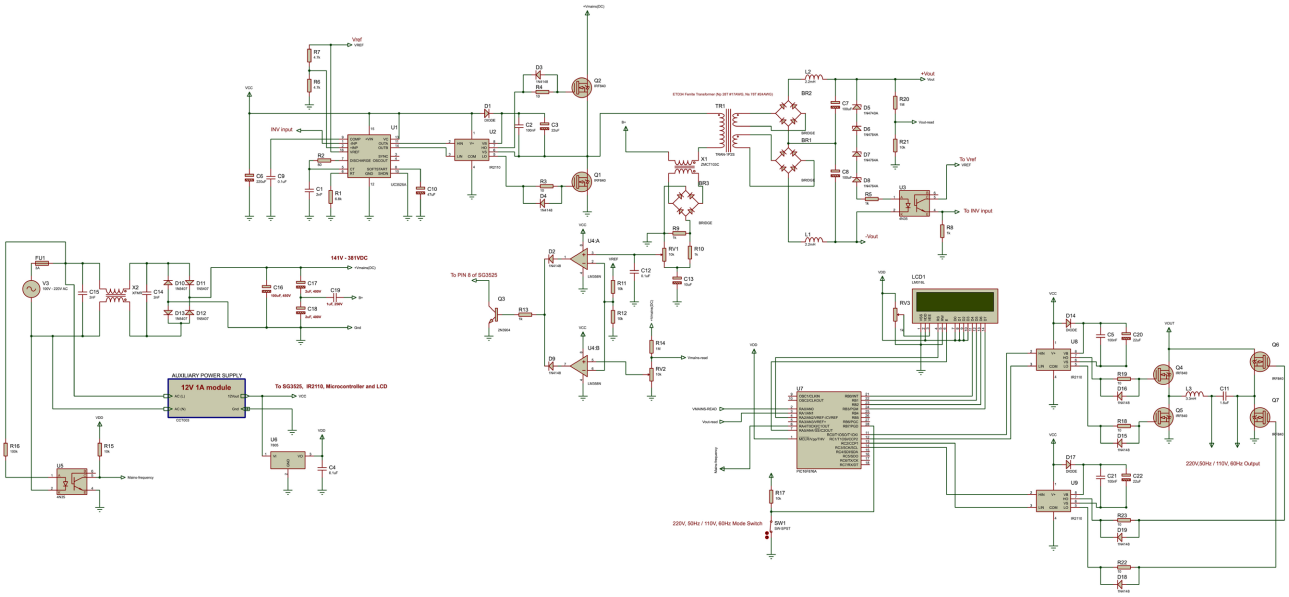

Figure 5. Schematic diagram of the design criteria circuits.

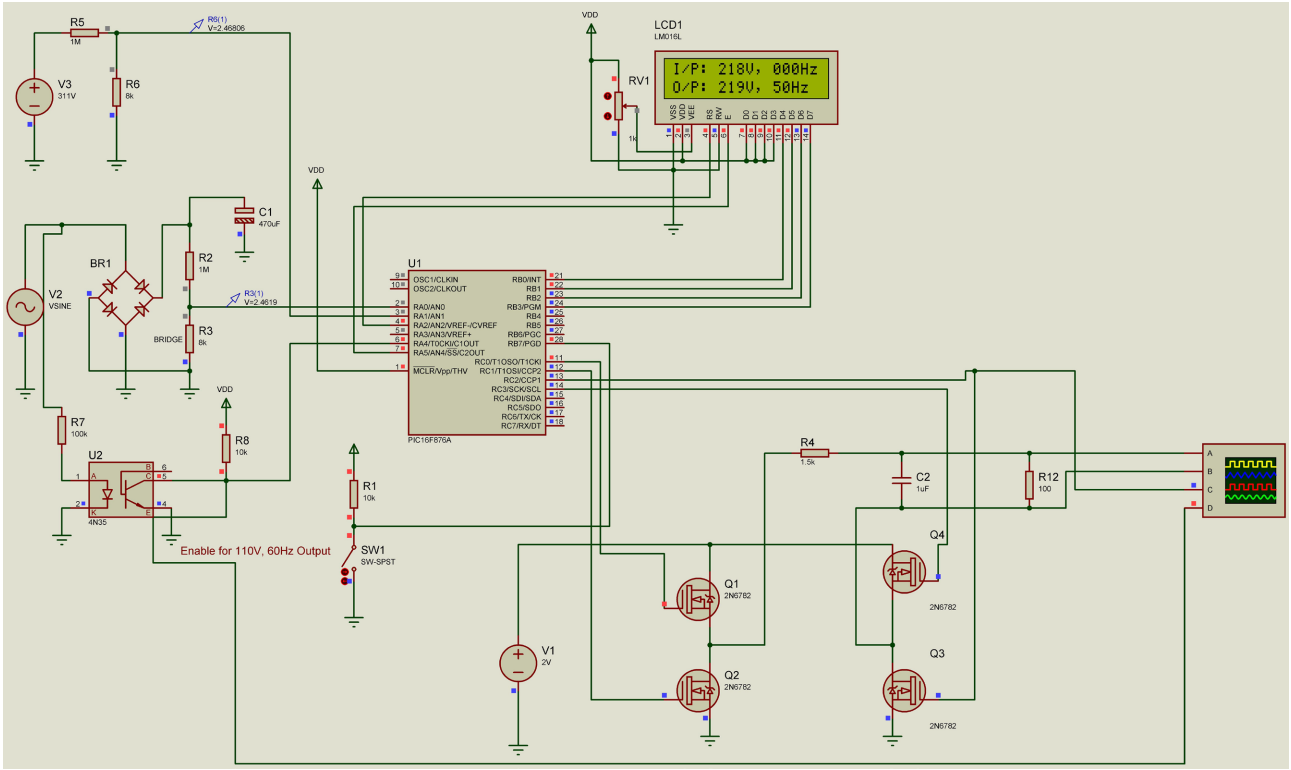

Figure 6. Circuit simulation of 220 V/50 Hz AC input.

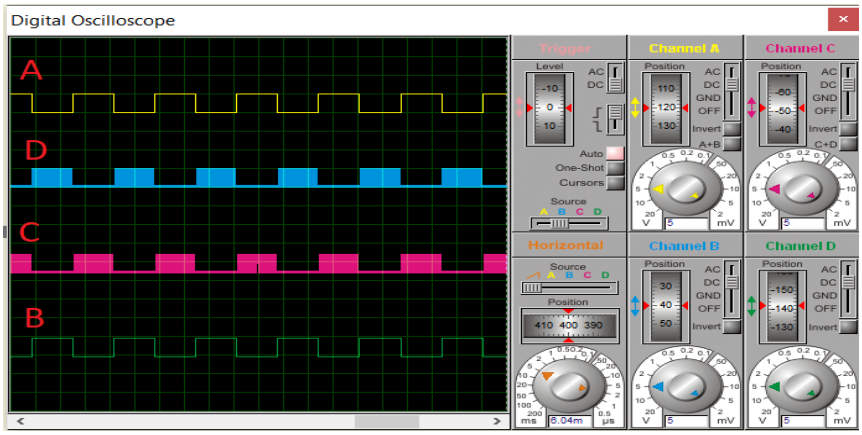

Figure 7. Drive signals output waveform for 220 V/50Hz.

lower MOSFETs, Q2 and Q4. Signals A and B alternate the SPWM through the upper MOSFETS Q1, Q3 at 50 Hz.

The images in Figure 7 and Figure 8 are waveforms captured on the real circuit using an oscilloscope. Since the Siglent SDS1102CNL is a dual-channel scope, only two waveforms can be viewed at a time.

Figure 8 shows the real circuit SPWM signals C and D from the microcontroller used to drive the lower MOSFETs through an IR2110 MOSFET driver.

Figure 9 shows the real circuit square wave signals A and B from the microcontroller used to drive the upper MOSFETS through an IR2110 MOSFET driver. The output of the H-bridge is still a square wave albeit an alternating one. To get a clean sine wave, an LC filter is used. Due to simulation constraints, an RC lowpass filter was used for the simulation. Figure 10 shows the resulting output waveform.

4.2. 110 V/60 Hz Simulation

The image in Figure 11 shows the circuit running under simulation in Proteus ISIS. From the simulation results, it was realised that when SW1 was closed, the LCD displayed the visual output and input mains voltage and frequency respectively as instructed for 110 V, 60 Hz. The drive signals fed to the gates of the MOSFETs in the H-bridge is shown in Figure 12.

Figure 12 Drive Signal and Filtered Output Waveform of 60 Hz when a square wave signal from the microcontroller was used to drive the MOSFETs through an IR2110 MOSFET driver, the output of the H-bridge still remained a square wave albeit an alternating one. To get a clean sine wave, an LC filter was employed. Due to simulation constraints, an RC lowpass filter was used for the simulation. Figure 12 shows the resulting output waveform.

4.3. Hardware Implementation

When all the various subsystems were built and put together, the smart power voltage and frequency synchronizer in power distribution system was built. Figure 13 shows the internal components of the prototype.

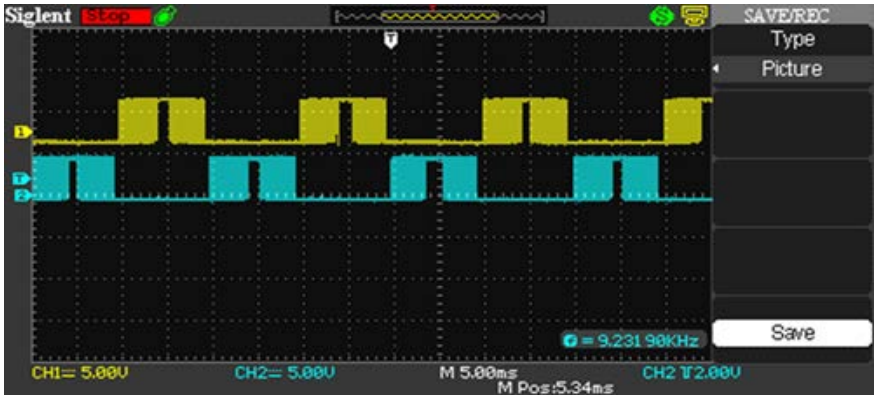

Figure 8. Real circuit drives signal waveform.

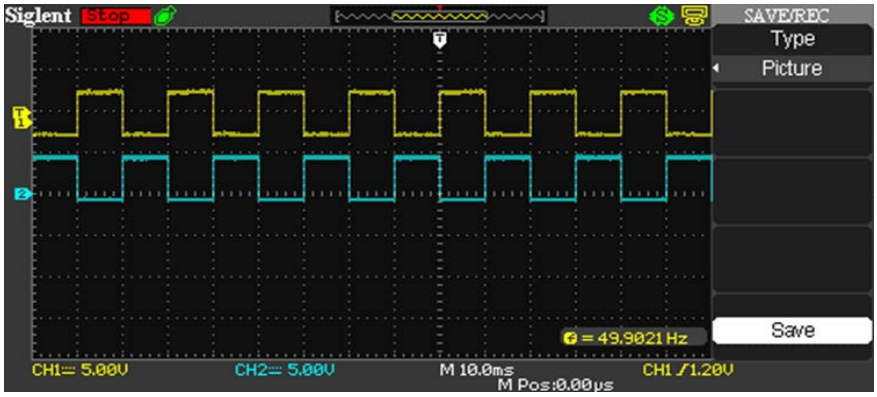

Figure 9. Real circuit H-bridge output waveform.

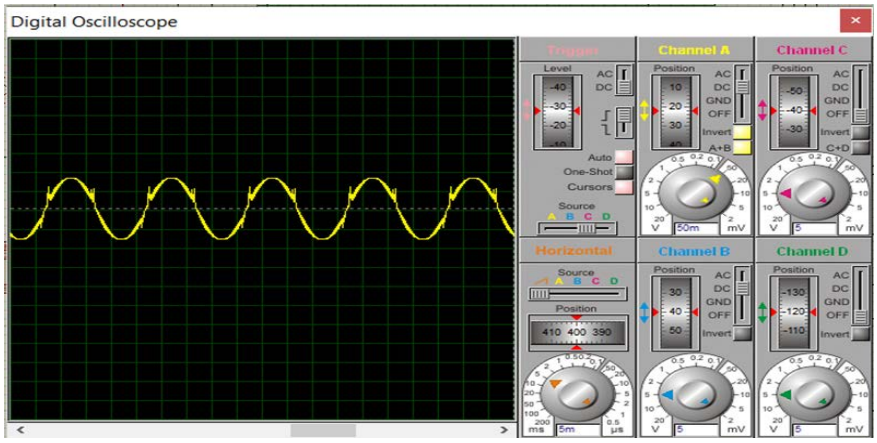

Figure 10. Filtered sine wave for 220 V/50Hz.

The hardware test was carried on at Sekondi 5 cell site of American Towers Company at Fijai Senior High School and was subjected to a series of tests. Several tests were conducted at various stages of the design implementation. However, the most recent tests and results are presented here. There are two steps involved in setting up. These include 220 VAC/50 Hz and 110 VAC and 60 Hz

Figure 14 shows the setup for the implementation of the 220 V/50 Hz test.

Figure 15 shows the setup for the implementation of the 110 V/60 Hz test.

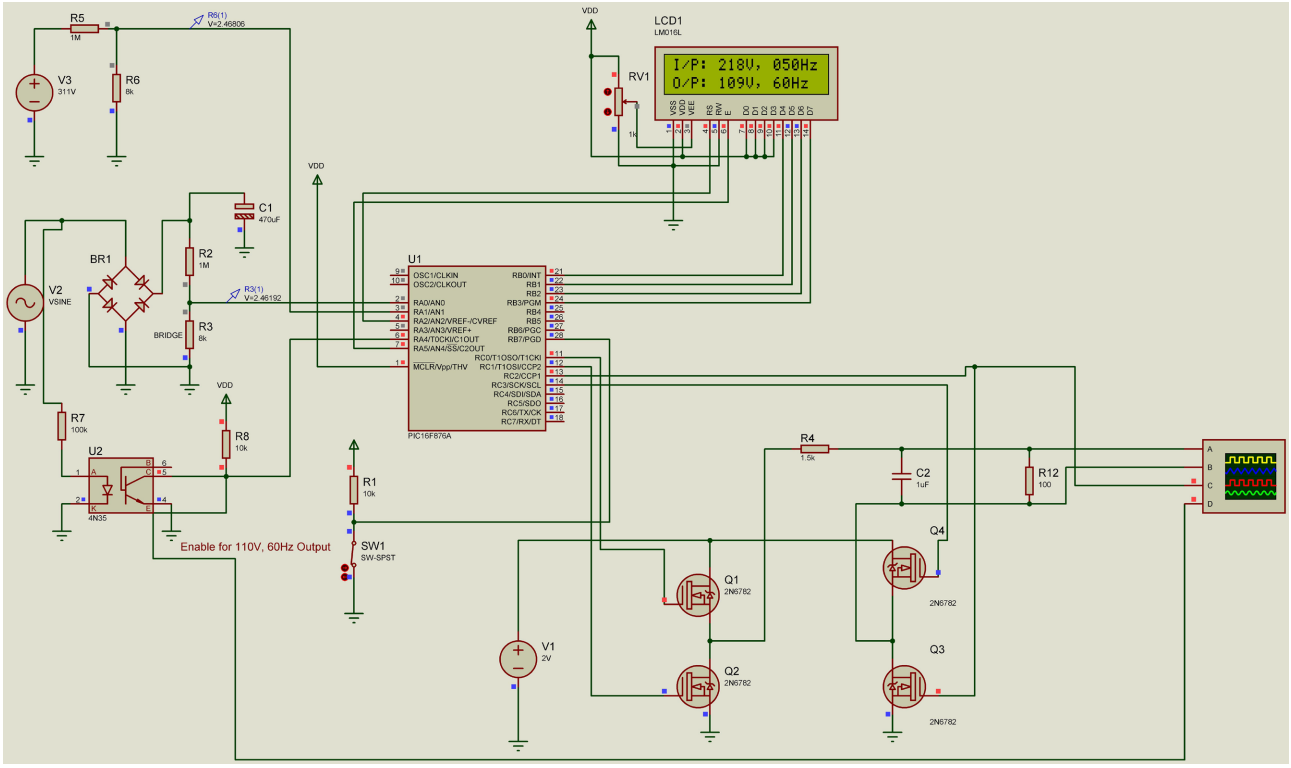

Figure 11. Circuit simulation of 110 V/60 Hz AC input'.

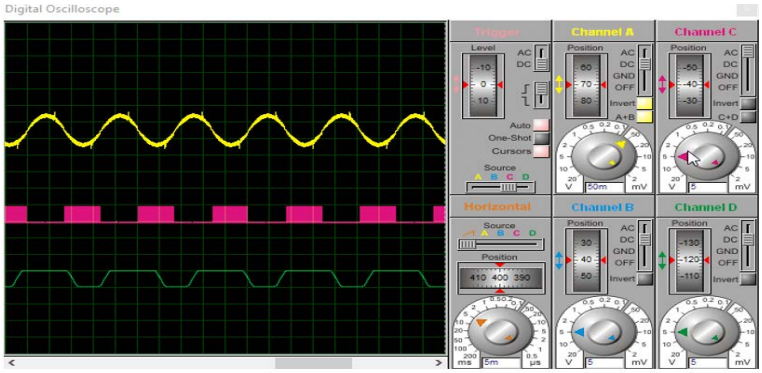

Figure 12. Drive signal and filtered output waveform of 60 Hz.

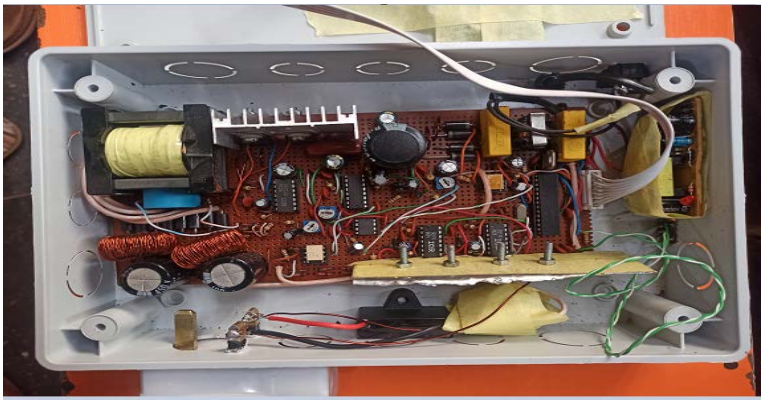

Figure 13. Infernal components of the prototype.

Figure 14. The setup for the implementation of 220 V/50 Hz test.

Figure 15. The setup for the implementation of 110 V/60 Hz test.

The load to the customer load cabinet was set within 100 W in order not to exceed the device operating safe maximum range of 200 W. The device was then subjected to a load by connecting the life and neutral cables coming from the existing consumer energy meter to the device input to monitor the output power consumption for a period of five-to-ten-minute intervals continuously at 240 V/50 Hz and 110 V/60 Hz respectively. The smart power frequency and voltage synchroniser device was monitored periodically to check the display on the LCD of the device. The load monitoring system was also monitored periodically to see if all appropriate fields were updated as designed.

At the end of the test, the following observations were made as shown in Tables 2-5:

1) Test results for a selectable stable output power for 220 V/50 Hz and 110 V/60 Hz proved successful;

2) The proposed smart power voltage and frequency synchroniser in the distribution system gave well-optimised performance outputs as a result of various frequency values taken at the cell site;

Table 2. Voltage readings values for 220 V/50 Hz.

Log	Date	Time	Duration In Minutes	Tigo Load (W)	MTN Load (W)	Battery VDC	Grid VAC Values	System Input VAC Values	System Output VAC Values
1	03/07/2022	5:45	5	30.444	47.269	12.35	242.00	239	222
2	03/07/2022	5:50	5	30.444	47.269	12.15	241.99	239	222
3	03/07/2022	5:55	5	30.444	47.269	12.55	241.90	239	222
4	03/07/2022	6:00	5	30.444	47.269	12.45	237.80	235	222
5	03/07/2022	6:06	5	30.444	47.269	12.25	238.60	235	222
6	03/07/2022	6:10	5	30.444	47.269	12.42	237.80	235	222
7	03/07/2022	6:15	5	30.444	47.269	12.55	238.60	235	222
8	03/07/2022	6:20	5	30.444	47.269	12.56	238.20	235	222
9	03/07/2022	6:25	5	30.444	47.269	12.25	238.30	235	222
10	03/07/2022	6:30	5	30.444	47.269	12.55	237.20	235	222
11	03/07/2022	6:35	5	30.444	47.269	12.15	242.10	239	222
12	03/07/2022	6:40	5	30.444	47.269	12.55	236.70	235	222
13	03/07/2022	6:45	5	30.444	47.269	12.55	236.80	235	222
14	03/07/2022	6:50	5	30.444	47.269	12.5	242.00	239	222
15	03/07/2022	6:55	5	30.444	47.269	12.55	237.80	235	222

Table 3. Frequency readings values for 50 Hz.

Log	Date	Time	Duration in Minutes	Tigo Load (W)	MTN Load (W)	Battery VDC	Grid F Values (Hz)	System Input F Values (Hz)	System Output F Values (Hz)
1	03/07/2022	5:45	5	30.444	47.269	12.35	50.23	50	50
2	03/07/2022	5:50	5	30.444	47.269	12.15	50.25	50	50
3	03/07/2022	5:55	5	30.444	47.269	12.55	50.25	50	50
4	03/07/2022	6:00	5	30.444	47.269	12.45	50.23	50	50
5	03/07/2022	6:06	5	30.444	47.269	12.25	50.23	50	50
6	03/07/2022	6:10	5	30.444	47.269	12.42	50.21	50	50
7	03/07/2022	6:15	5	30.444	47.269	12.55	50.21	50	50
8	03/07/2022	6:20	5	30.444	47.269	12.56	50.10	50	50
9	03/07/2022	6:25	5	30.444	47.269	12.25	50.15	50	50
10	03/07/2022	6:30	5	30.444	47.269	12.55	50.00	50	50
11	03/07/2022	6:35	5	30.444	47.269	12.15	50.23	50	50
12	03/07/2022	6:40	5	30.444	47.269	12.55	50.23	50	50
13	03/07/2022	6:45	5	30.444	47.269	12.55	50.10	50	50
14	03/07/2022	6:50	5	30.444	47.269	12.50	50.10	50	50
15	03/07/2022	6:55	5	30.444	47.269	12.55	50.23	50	50

Table 4. Voltage readings values for 110 V/60Hz.

Log	Date	Time	Duration in Minutes	Tigo Load (W)	MTN Load (W)	Battery VDC	Grid VAC Values	STDTF VAC Values	System Input VAC Value	System Output VAC Value
1	03/07/2022	7:00	10	30.444	47.269	12.55	236.70	110.20	110	112
2	03/07/2022	7:10	10	30.444	47.269	12.50	236.80	111.40	111	112
3	03/07/2022	7:20	10	30.444	47.269	12.45	241.80	117.60	112	112
4	03/07/2022	7:30	10	30.444	47.269	12.21	237.80	111.50	110	112
5	03/07/2022	7:46	10	30.444	47.269	12.35	238.60	113.20	110	112
6	03/07/2022	7:50	10	30.444	47.269	12.45	237.80	109.70	110	112
7	03/07/2022	8:00	10	30.444	47.269	12.50	238.60	113.50	110	112
8	03/07/2022	8:10	10	30.444	47.269	12.55	235.40	106.00	110	112
9	03/07/2022	8:20	10	30.444	47.269	12.55	235.10	106.00	110	112
10	03/07/2022	8:30	10	30.444	47.269	12.50	237.20	122.10	117	112

Table 5. Frequency readings values for 50 Hz.

Log	Date	Time	Duration In Minutes	Tigo Load (W)	MTN Load (W)	Battery VDC	Grid F Values (Hz)	STDTF Values (Hz)	System Input F Value (Hz)	System Output F Value (Hz)
1	03/07/2022	7:00	10	30.444	47.269	12.55	51.10	50.40	50	60
2	03/07/2022	7 10	10	30.444	47.269	12.50	50.20	50.10	50	60
3	03/07/2022	7:20	10	30.444	47.269	12.45	51.20	51.00	50	60
4	03/07/2022	7:30	10	30.444	47.269	12.21	50.20	50.10	50	60
5	03/07/2022	7:46	10	30.444	47.269	12.35	50.80	50.60	50	60
6	03/07/2022	7:50	10	30.444	47.269	12.45	51.20	51.10	50	60
7	03/07/2022	8:00	10	30.444	47.269	12.50	50.20	50.00	50	60
8	03/07/2022	8:10	10	30.444	47.269	12.55	50.70	50.50	50	60
9	03/07/2022	8:20	10	30.444	47.269	12.55	50.10	50.10	50	60
10	03/07/2022	8:30	10	30.444	47.269	12.50	50.50	50.40	50	60

3) In the presence of varied load and input voltage conditions the proposed smart power voltage and frequency synchroniser in the distribution system presented a good performance and more stable output according to the electrical characteristics of the facility;

4) The regulatory mechanism of the proposed smart power voltage and frequency in the distribution system worked very satisfactorily than that of the conventional automatic voltage regulator; and

5) The smart power voltage and frequency in the distribution system device proved efficient in terms of functionalities, reliability, and adaptability to the climate condition.

5. Conclusion

The implementation of a smart power voltage and frequency synchronizer in the

power distribution system is beneficial to the customer and also challenging in stabilizing voltage and frequency instabilities in the power distribution system. The implemented distribution power system study attested that, modern technologies capable of delivering power in more efficient ways and responding to wide-ranging conditions and events are needed. The proposed solution proved that by deploying over current and over voltage protecting and sensing circuit in closed operation with the feedback system and the adoption of the direct digital synthesizer technique, the designed system maintained constant output voltage and frequency under varied load and input voltage fluctuations. This system should be deployed in telecommunication cell sites to reduce the number of passive outages as well as the faults MTTR recorded daily. For further studies, the high noise due to the low voltage switching and logic circuits sharing common ground with the mains circuit should be fixed by isolating the low voltage and high voltage circuits. Rather than using an IR2110 for switching the half-bridge MOSFETs and H-Bridge, a pulse transformer should be used. Future work will focus on the fusion of the proposed techniques into solid-state devices, increasing durability, reducing moving parts to wear out or fail, a high-speed response, and the reduction of heat and power consumption. This model will be more precise if DDS data used for sine wave generation were doubled in order to create a smoother sine wave output voltage requiring lower LC filter values.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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