Scientific Research Publishing

Journal of Power and Energy Engineering, 2023, 11, 1-17
https://www.scirp.org/journal/jpee
ISSN Online: 2327-5901
ISSN Print: 2327-588X

New Approach of Multi-Cell Stacked Cell Inverter for Solar Photovoltaic System

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How to cite this paper: Yonga, F., Welba, C., Dadjé, A. and Djongyang, N. (2023) New Approach of Multi-Cell Stacked Cell Inverter for Solar Photovoltaic System. *Journal of Power and Energy Engineering*, **11**, 1-17.
https://doi.org/10.4236/jpee.2023.111001

Received: January 27, 2022
Accepted: January 28, 2023
Published: January 31, 2023

Abstract

In this paper, a new inverter topology dedicated to isolated or grid-connected PV systems is proposed. This inverter is based on the structures of a stacked multi-cell converter (SMC) and an H-bridge. This new topology has allowed the voltage stresses of the converter to be distributed among several switching cells. Secondly, divide the input voltage into several fractions to reduce the number of power semiconductors to be switched. In this contribution, the general topology of this micro-inverter has been described and the simulation tests developed to validate its operation have been presented. Finally, we discussed the simulation results, the efficiency of this topology and the feasibility of its use in a grid-connected photovoltaic production system.

Keywords

Photovoltaic System, Micro-Inverter, Stacked Multi-Cell Converter (SMC), H-Bridge, Pulse Width Modulation (PWM)

1. Introduction

The topology of power converters, system stability and control of grid-connected photovoltaic power plants has attracted considerable interest in recent years [1] [2]. Since existing technologies are not yet suitable for large-scale photovoltaic power plants. The performance and in particular the profitability of inverters used to connect renewable energy production systems to the electricity distribution network are key elements that strongly influence the quality of the energy produced and the efficiency of the entire installation. During the last two dec-

ades, extensive research has been carried out to propose new topologies of inverters [1] [3] [4]. The structure of multilevel, three-level and more inverters makes it possible to overcome this problem. The use of this type of architecture helps to limit the voltage stresses on the switches by splitting the DC voltage at the inverter input. The association of a multilevel type architecture with judicious control of the power switches also makes it possible to eliminate certain families of harmonic lines and consequently to improve the spectral content of the output signals (voltage and current) [1] [2]. Multilevel inverters (PWM) are highly valued in the field of power electronics research because of their advantages over conventional power inverters [5] [6]. Some of these advantages include reduced voltage and $\mathrm{d}v/\mathrm{d}t$ stress, improved harmonic reduction performance, and less electromagnetic interference such as reduced switching losses [7]. Therefore, these factors along with the growing demand for clean, renewable energy have made multi-level inverters extremely popular in industry and academia. Most renewable sources behave like continuous sources, making inverters an indispensable tool for integrating these sources into existing electricity grids [6]. A multilevel inverter is a power electronic system that synthesizes a desired output voltage from multiple DC voltage levels as inputs [8]. We can see that the more number of levels increases, the better the waveform (close to a sinusoid) [3] [4] [9] [10] [11]. Recently, multi-level power conversion technology has been developing in the field of power electronics very rapidly with good potential for further development. The most attractive applications of this technology are in the medium to high voltage ranges [8]. Moreover, this type of inverter can generate a high number of voltage levels, which leads to the reduced harmonic distortion and better power quality. From the topological perspective, the multilevel inverters are divided into three main categories: neutral point clamped (NPC) multilevel inverters, flying capacitor-based multilevel inverters, and cascaded multilevel inverters [12]. Three-level neutral-point-clamped (NPC) converter has been widely used in high-power motor drives and renewable energy conversions. However, as the number of voltage level increases, the clamping diodes and unbalanced loss distribution will be fast increased [13]. In recent years, hybrid multilevel converters have been proposed and compared to popular multilevel topologies, they require fewer switches and FCs [14] [15]. Active neutral-point-clamped (ANPC) converter is a newly introduced hybrid multilevel converter (HMC), which combines the advantages of the NPC and FC converters. Three-level ANPC and several five-level ANPC topologies have been put forward in [13]. In this configuration, to generate a high number of voltage levels, the number of diodes is increased slightly, which limits applications of this topology. The other problem of the NPC topologies is balancing the voltages of DC links, especially the high number of voltage levels [13]. The multicell topology is a good alternative for NPC topologies. Despite their need for a high number of DC voltage sources, they are considered tremendously in high-power applications [12] [16]. Also, there are different derived topologies, such as flying capacitor multicell (FCM) and stacked multicell (SM) topologies, which show

the great importance of the multicell topologies [13]. The stacked multicell converter (SMC) is another HMC [12], and it draws much attention due to the overwhelming merits, such as modularity, and inherent natural balancing of FCs. Three-level T-type converter (T^2C) can be recognized as the SMC with one cell [13] [17]. In low-voltage applications, a three-level T^2C is a better choice than a three-level NPC converter due to low conduction losses. Several HMC topologies have been proposed based on the T^2C cell [13] [15]. To further increase the voltage levels with reduced devices (including dc voltage source, switches and FCs), several new hybrid stacked multicell converters (HSMCs) have been proposed based on the SMC [13]. These topologies are mainly obtained by adding a low frequency (LF) switches to the original SMC. In [13], the number of dc voltage sources was reduced to half. FCM topology and its derived topology, SM, have some attractive features, such as fixing the flying capacitors' voltages in a predetermined value, which leads to the high usage in applications. This feature, which is named as "self voltage-balancing property," makes these topologies to be able to generate all of the voltage levels without a further voltage-balancing technique [12]. Due to these advantages, many kinds of research improve the FCM-based topologies from the topological or the control method point of view [12] [18] [30]. In this paper, the proposed new multi-cell topology is developed and analysed to solve the problems of voltage balancing and loss distribution inherent in floating capacitor multilevel converters (FCM), neutral point clamped (NPC) topology and stacked multicell (SMC) topology. It is essential to note that the self-balancing capability of the developed topology does not require that the average value of the currents flowing through the floating capacitors is equal to zero, and that the capacitors and clamping diodes are existing there. Moreover, the proposed topology effectively ensures the self-balancing function of the voltages in the absence of a transformer and the equality of the voltages between the switches. The control scheme of the proposed topology, which is based on sinusoidal pulse width modulation (SPWM), is presented. Finally, simulations are performed to record the output voltage waveforms and validate this new approach. Following the Introduction section, this paper is organised as follows: Section 2 concerns the description of the proposed topology. Section 3 is devoted to the modelling of the proposed topology. Section 4 presents the simulation results and the discussion. Finally, Section 5 is devoted to the conclusion.

2. Description of the Proposed Topology

Figure 1(a) shows an SMC converter. This converter structure is an evolution of the serial multicellular converter [19]. It was patented in 2000 in France [20] [21] and 2001 in the world [22]. In **Figure 1(b)**, a modification of the basic NPC (Neutral Point Clamped) topology is presented. This variant of the NPC topology (three-level ANPC) makes it possible to push back certain limitations of the basic structure, such as the inequality of the reverse voltages supported by the diodes [11] [30].

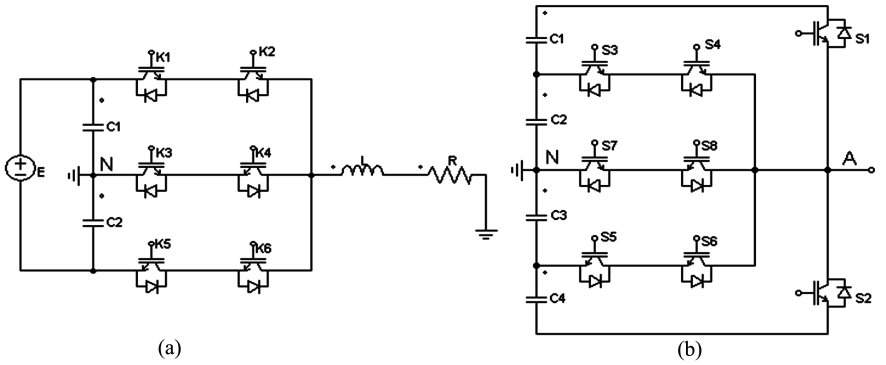


Figure 1. (a) Single phase multicellular model with three-levels [19] and (b) existing ANPC inverter [23].

The basic cell of a multicellular converter can be made up of 4, 6 or 8 switches (**Figure 1**). The outer branches are made up of two 3-segment switches: the switches must be connected in series for voltage withstand. The voltage withstand of all the different switches is E/2. The middle branch is made up of two switches placed in opposition. For these switches, the maximum voltage withstand is equal to E/2; they don't need to be passed [19]. **Figure 2** shows a new five-level three-phase multicell inverter (5L-SMC H-bridge) topology based on stacked semiconductors and implemented using the PSIM software environment.

This inverter topology is based on the single-phase model of a three-level inverter (3L-SMC H-bridge), two variants of which are given in **Figure 3**.

In the structure of **Figure 4**, we have a stacked multicell converter and a half H-bridge. The multicell converter consists of two branches of stacked semiconductors (Cell+ and Cell−) connected to the T-Type bridge. However, by using an appropriate control, our converter provides a DC signal, a three-level AC signal (3L) which can be filtered and fed into the public distribution network [24] [25]. The switches K3, K4, K7 and K8 make it possible to raise the voltage level and prevent the direct voltage source from being short-circuited (directly connected to ground) [26]. Switches K1 and K2 (Cell H), constituting the H-bridge, balance the voltage level at the output of the inverter.

The superimposed cells (Cell+ and Cell−) are the opposition of two semiconductors of the same control so as to form a bidirectional switch on blocking. Putting two switches in opposition does not increase switching losses, because only one of the two switches at the switching frequency, the other switching only twice per modulation period. Unlike the case of multicellular converters with floating capacitors (FC), the Cell+ and Cell− cells are not connected to each other by floating capacitors. The distribution of the voltage stress is linked to the state of the switches (on or off) [27]. As for the 2 × 2 SMC, it is possible to double these switches to obtain a structure with switches whose voltage resistance is identical. These will switch at a lower switching frequency (on the order of the modulation frequency). But this increases the number of switches even

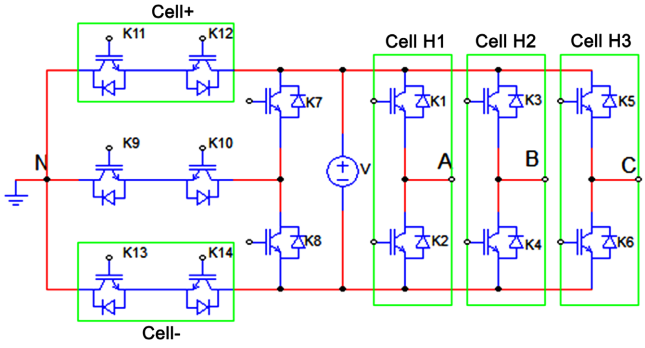
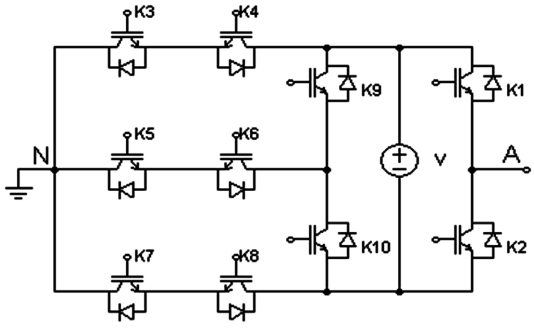
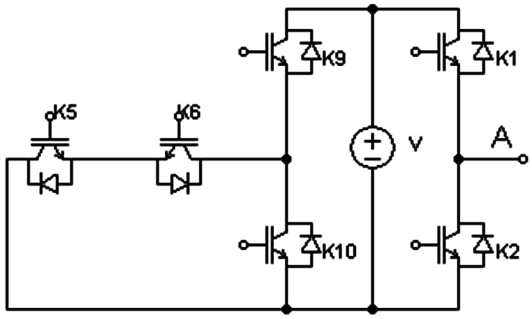


Figure 2. Three-phase, five-level multicellular model (5L-SMC H-bridge) proposed.



(a)



(b)

Figure 3. Variants of the three-level inverter (3L-SMC H-bridge): (a) With three stacked cells and (b) With one stacked cell.

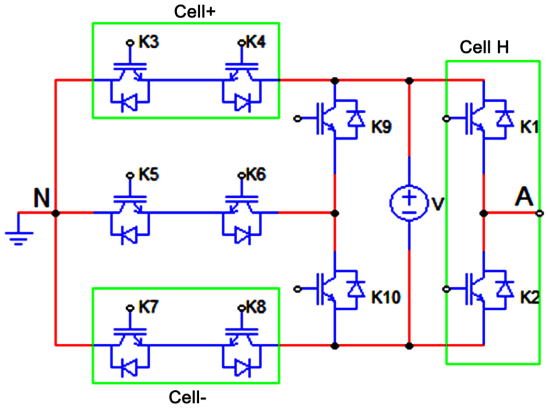


Figure 4. 3L-SMC H-bridge inverter with three stacked cells.

further: the total number of switches per phase is then 8 semiconductor components. The interest of this study is above all to balance the DC bus. So for more simplicity in the control, each switch having to hold a tension of V/2 is considered as unique [19]. The mathematical model of the five-level three-phase multi-cell inverter topology (5L-SMC H-bridge) in the next section will later help explain its operation.

3. Modelling the Converter

To develop a mathematical model of our multicellular converter, we consider that:

- Semiconductors are perfect;
- The switches of the same switching cell operate in a complementary manner;
- The supply voltage is continuous.

In practice, the upper and lower branches of the structure can contain one or two semiconductors in series. The voltage applied to each switching cell in the off state is constant and is equal to [3] [27]:

$$v_{Cell_j} = \frac{V}{p} \quad \text{with} \quad j \in \{1, \cdots, p\} \tag{1}$$

In the presence of a single switch, it must withstand a voltage stress twice as high as those of the middle branch. In order to standardize the distribution of the voltage stress, two identical semiconductors can be connected in series or in opposition; their commands being similar [3] [4] [27]. In this assumption, the stress in tension of all the switches of the structure is worth:

$$v_{Int_j} = \frac{V}{n \times p} \quad \text{with} \quad j \in \{1, \cdots, p\} \tag{2}$$

where: n and p represent respectively number of stages and number of cells associated with the converter.

In **Figure 4**, the upper (Cell+) and lower (Cell−) branches of the structure contain two opposing semiconductors. The voltage applied to each switching cell in the off state is:

$$v_{Cell_j} = \frac{V}{2} \quad \text{with} \quad j \in \{1, 2\} \tag{3}$$

The multicellular converter is made up of 4 or 8 switches (**Figure 3**). The opposition of switches of the outer branches is necessary for voltage withstand. The voltage withstand of all the different switches is $V/2$. Indeed, levels $-V/2$ and $V/2$ can be achieved in 2 different ways and level 0 in 3 different ways, as presented in **Table 1**.

One of the main drawbacks of this structure is the number of components that compose it. The structure of our inverter model can include 8 to 14 switches with different voltage resistance. Indeed, on each basic structure, the switches of the outer branches must hold a voltage V while those of the inner branch must hold a voltage of $V/2$. Doubling the switches increases switching losses, because the two switches switch simultaneously at the switching frequency. The middle

Table 1. Possible states of the switches and the output voltage of the inverter.

Case	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	Output voltage
1	1	0	0	0	0	0	0	0	1	0	1	1	0	0	0
2	1	0	0	0	0	0	0	0	1	1	0	0	0	0	+V/2
3	1	0	0	0	0	0	1	1	0	0	0	0	0	0	+V
4	0	0	1	0	0	0	0	0	1	1	0	0	1	1	+V/2
5	0	1	0	0	0	0	0	0	1	0	1	1	0	0	0
6	0	1	0	0	0	0	1	1	1	1	0	0	0	0	−V/2
7	0	1	0	0	0	0	0	0	0	0	0	0	1	1	−V
8	0	0	0	1	0	0	1	1	1	1	0	0	0	0	−V/2
9	0	0	1	0	0	0	0	0	1	0	1	1	0	0	0

branch is made up of two switches placed in opposition. For these switches, the maximum voltage withstand is equal to $V/2$, they do not need to be doubled. This converter is used to generate (Pxn) + 1 output voltage levels. This new topology makes it possible to distribute the voltage constraints of the converter between several switching cells. It also makes it possible to divide the input voltage into several fractions so as to lower the number of switching power semiconductors. Compared to competing topologies in this field of application, the SMC converter has excellent dynamic performance thanks to the multiplication of the chopped voltage frequency and the increase in the number of levels [9] [28] [29]. The stacked multicellular structure can be adapted to all configurations: chopper or inverter mounting.

Figure 5 shows some possible combinations of the three-phase five-level multicell inverter (5L-SMC H-bridge).

The number of output levels is equal to 5 $[-V, -V/2, 0, +V/2, +V]$. In comparison with the 5-level NPC structure, the advantage of this structure is that it has redundancies for certain levels. Table 2 shows a comparison between the different types of existing inverters with the new 5L-SMC H-bridge three-phase multicell inverter.

From the above, it appears that the new 5L-SMC H-bridge structure gives more advantages (absence of looping diodes and capacitors) over its competitors NPC, SMC and H-bridge. The major drawback to note is the high number of switches used. Multicellular topologies, on the other hand, use the series connection of switches, thus ensuring the distribution of the voltage stress of the converter over several switching cells. The interlacing or shifting of the controls allows these converters to reveal voltage levels En and to multiply the apparent frequency at the output. These improvements induce a harmonically better quality output voltage spectrum and significantly reduce filtering requirements (volume, stored energy, cost) [27] [30]. Simulations carried out under suitable conditions produce results that highlight the performance and flexibility of this new proposed topology.

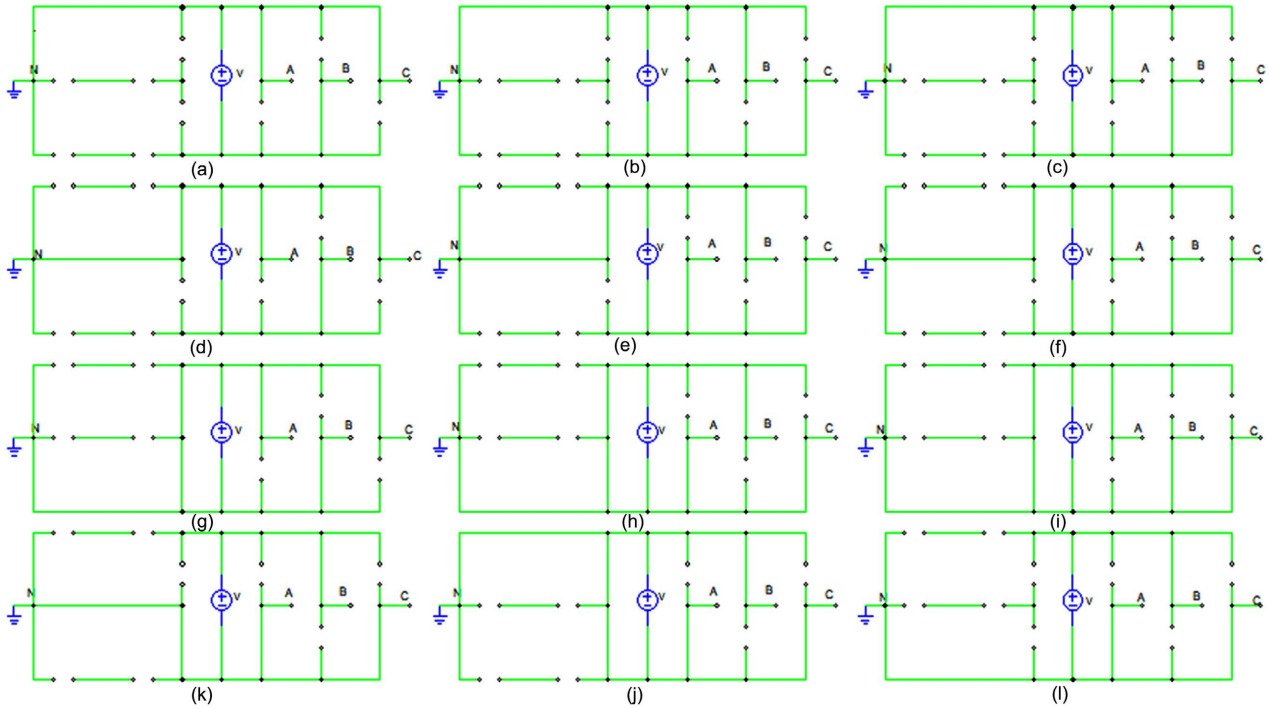


Figure 5. Some combinations that can be made by the inverter.

Table 2. Comparison between the five multilevel inverter structures.

	NPC	MPC	MNP	SMC	H-bridge	5L-SMC H-bridge
Number of DC voltage sources	2	1	1	2	$(n-1)/2$	1
Number of capacitors	$(n-1)(n-2)$	$n-1$	$n-1$	$n-1$	$n-1$	0
Number of switches	$2(n-1)$	$2(n-1)$	$2(n-1)$	$2(n-1)$	$2(n-1)$	$2(2n+3)$
Number of looping diodes	$2(n-1)$	$2(n-1)$	0	0	0	0

4. Results and Discussion

The simulation studies are carried out using Matlab/Simulink software (R2014a). The command method is SPWM. THD% values are measured using Powergui's FFT block. Simulation results are presented to illustrate and validate the performance and ruggedness of the 5L-SMC H-bridge three-phase multicell inverter. The electrical simulation parameters are given in Table 3.

The simulation of the system thus established in Figure 6, allows us to obtain the characteristics of the voltage and the current; as well as their harmonic spectra in Figures 7-10.

Figure 8 and Figure 10, it emerges that the harmonics of the voltage are higher (69.93%) and those of the current lower (2.78%). Likewise, the simulation of the three-phase inverter model proposed in Figure 11 gives the results of Figures 11-21.

Figure 12 and Figure 13 show respectively the waveform and the harmonic spectrum of the voltage between phase a and phase b (V_{ab}) obtained at the output of the proposed 5L-SMC H-bridge three-phase multicell inverter.

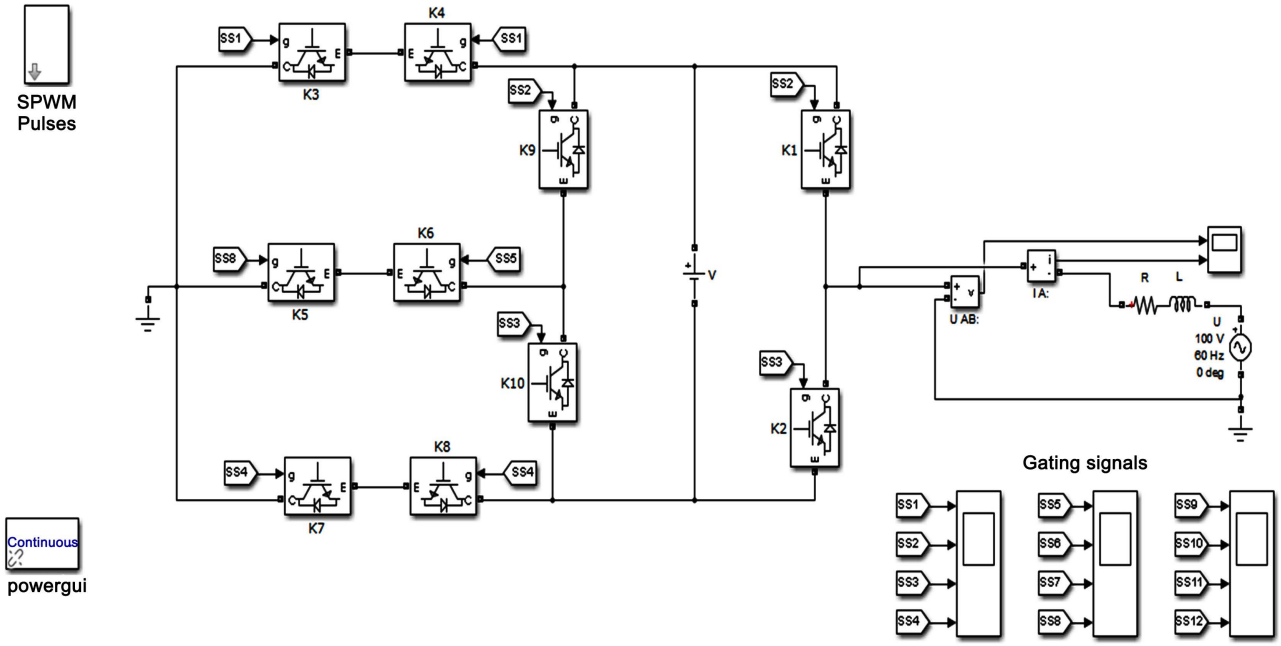


Figure 6. Single-phase model of the inverter 3L–SMC H-bridge inverter offered.

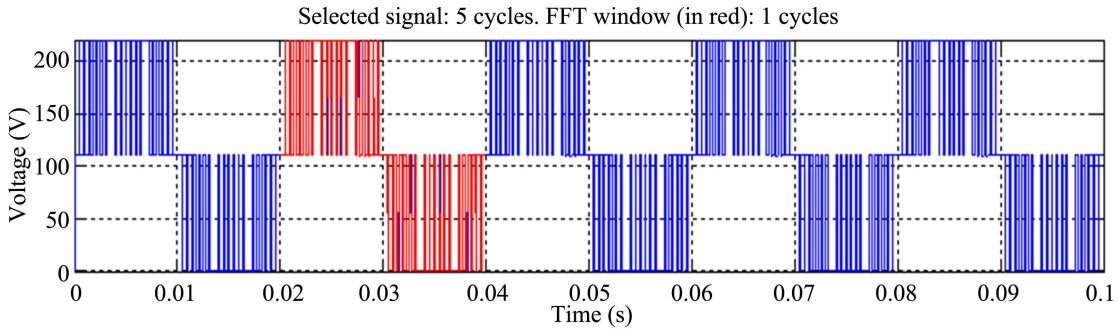


Figure 7. Output voltage.

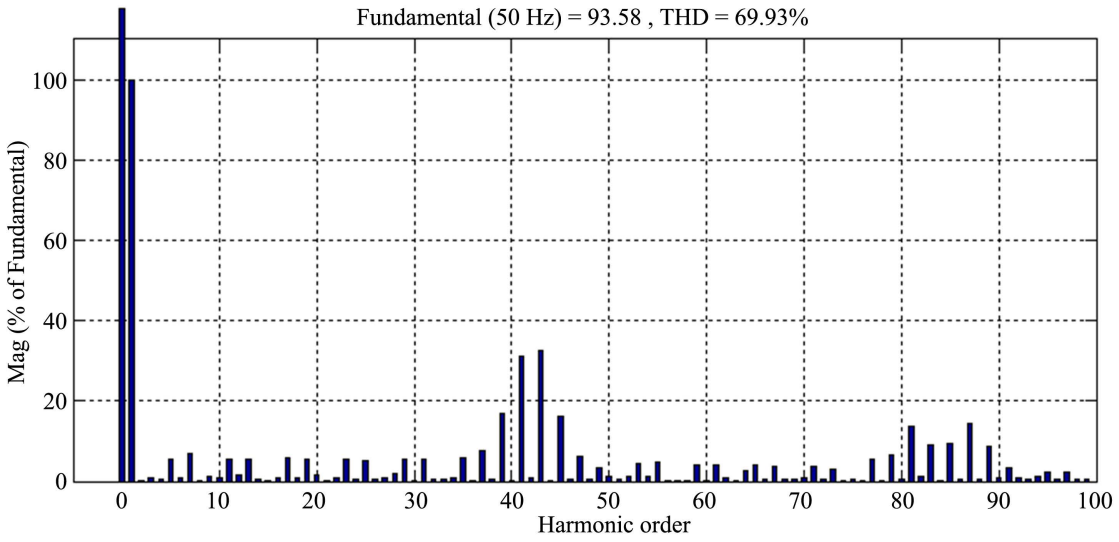


Figure 8. Harmonic spectrum of the output voltage.

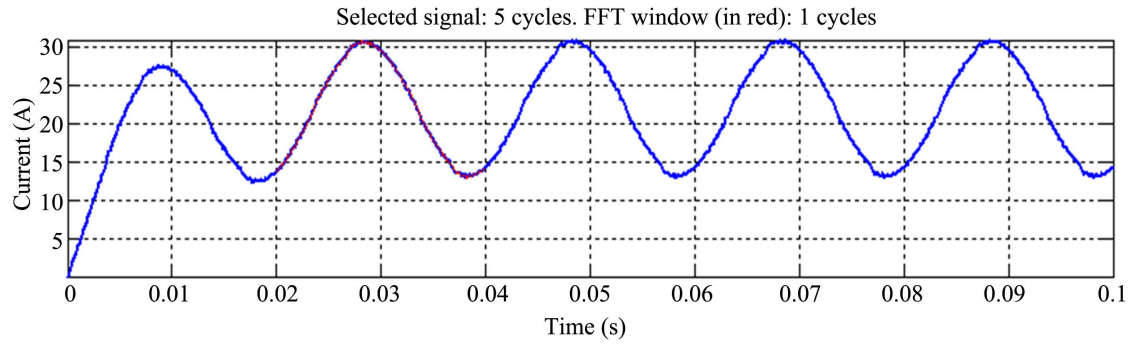


Figure 9. Output current.

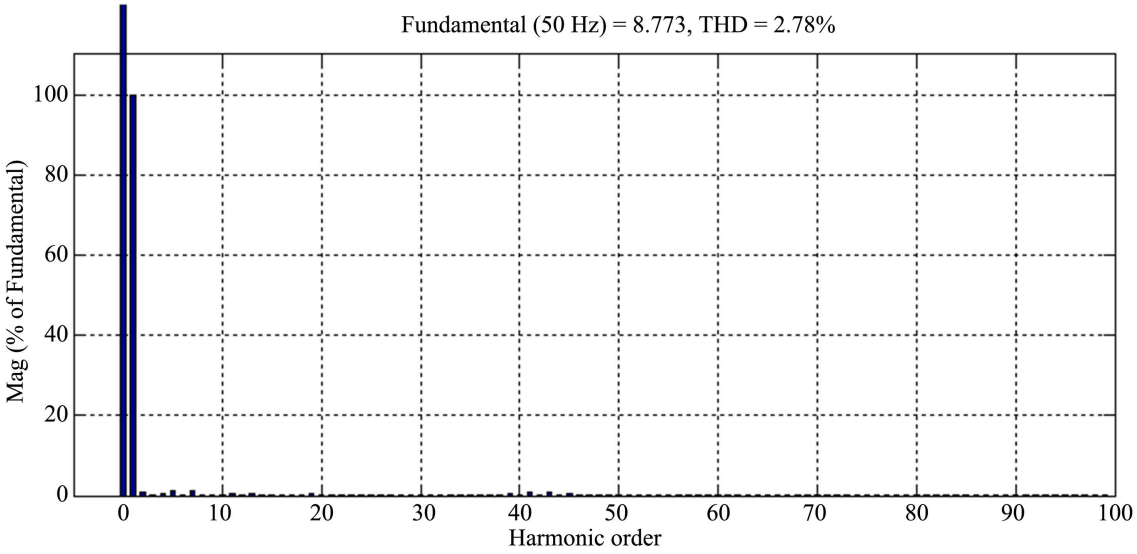


Figure 10. Output current spectrum.

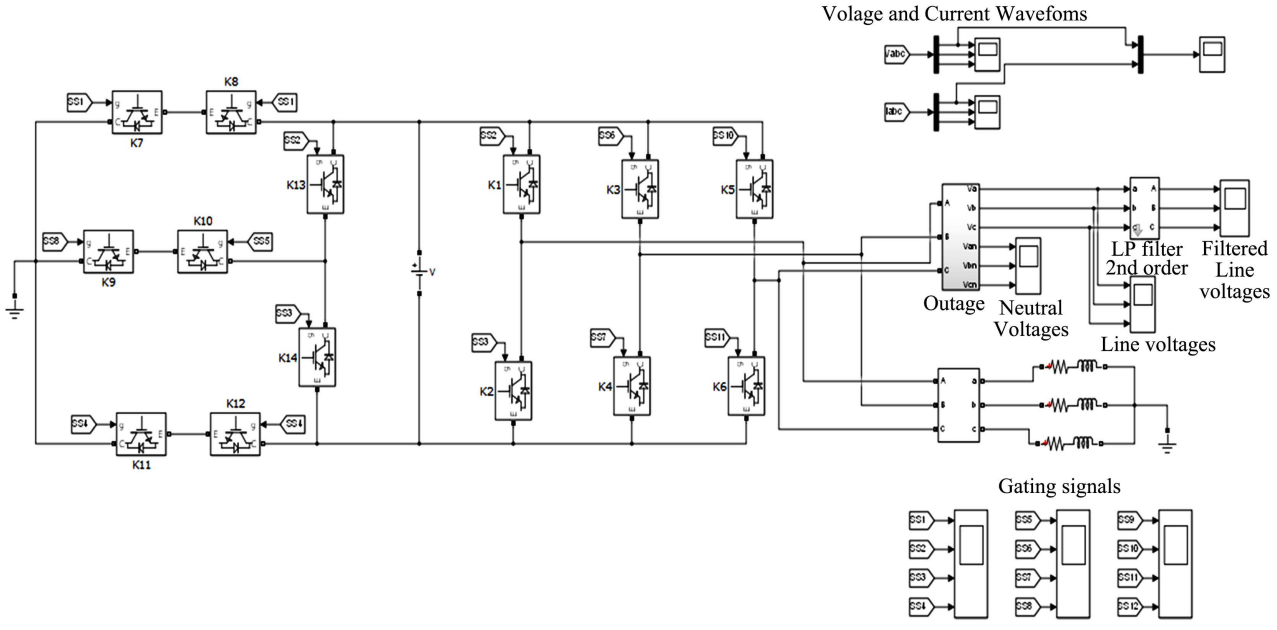


Figure 11. Three-phase model of the three-phase 5L-SMC H-bridge multistage inverter offered.

Table 3. Electrical simulation parameters in Matlab/Simulink.

Simulation parameters	Value
Continuous bus	V = 220 V
Load inductance	L_{ch} = 3 mH
Load resistance	R_{ch} = 5 Ω
Modulation frequency	M_f = 21 Hz
Modulation index	M = 0.8
Reference frequency	f = 50 Hz

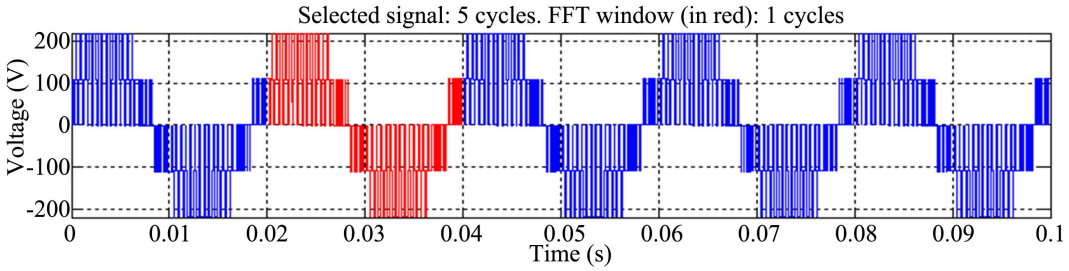


Figure 12. Phase-to-phase voltage seen with the "outage".

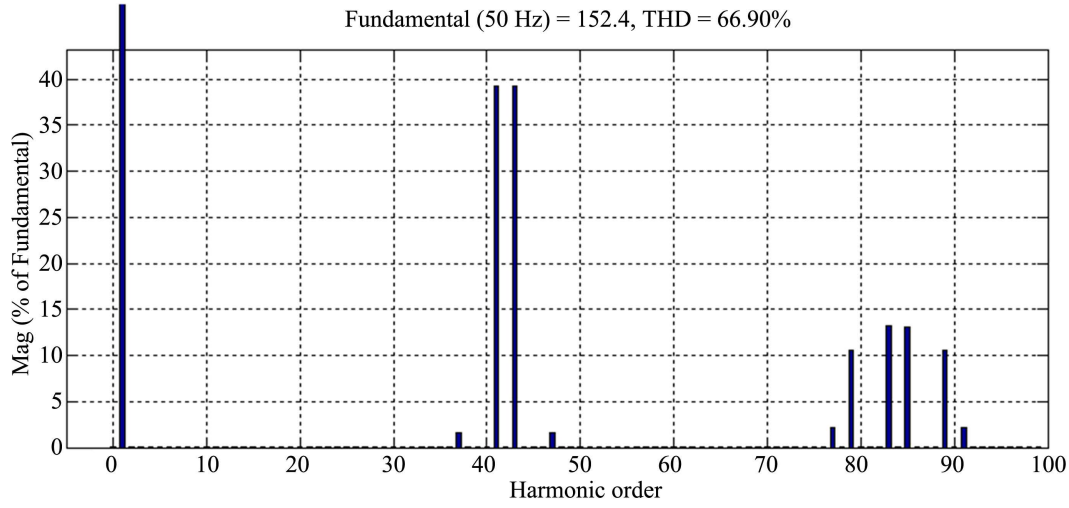


Figure 13. Spectrum of phase-to-phase voltage seen with the "outage".

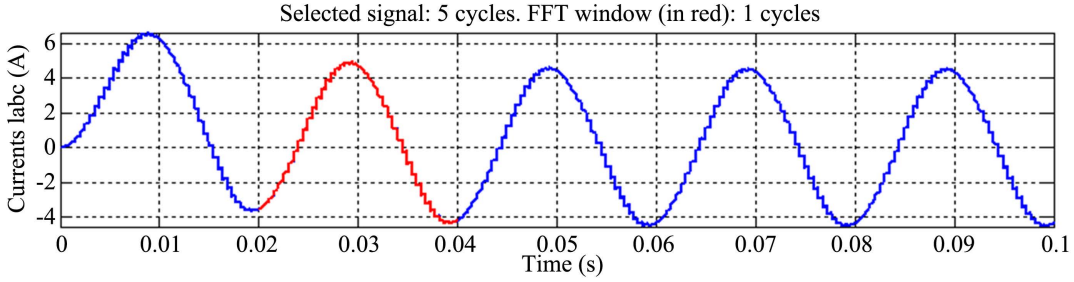


Figure 14. Output current seen with the "outage".

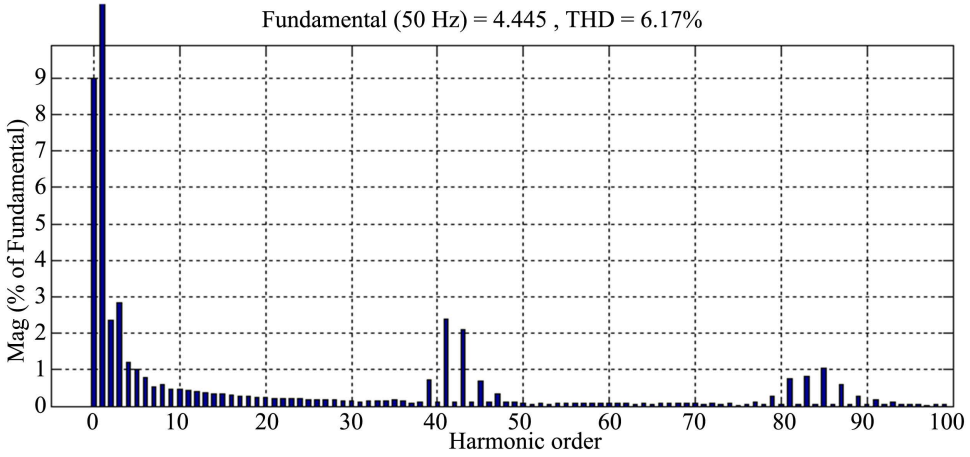


Figure 15. Spectrum of the output current seen with the "outage".

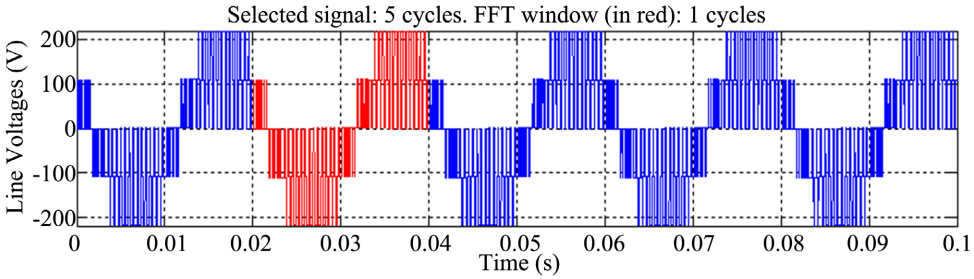


Figure 16. Line voltage.

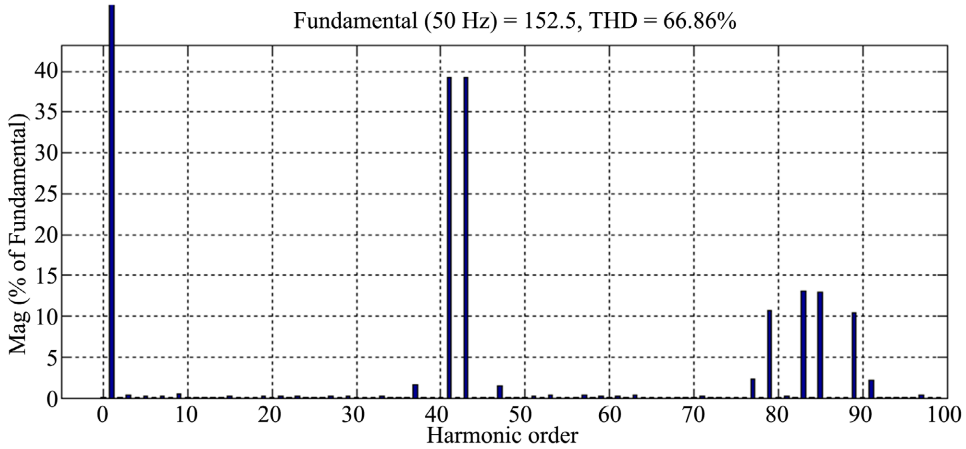


Figure 17. Line voltage spectrum.

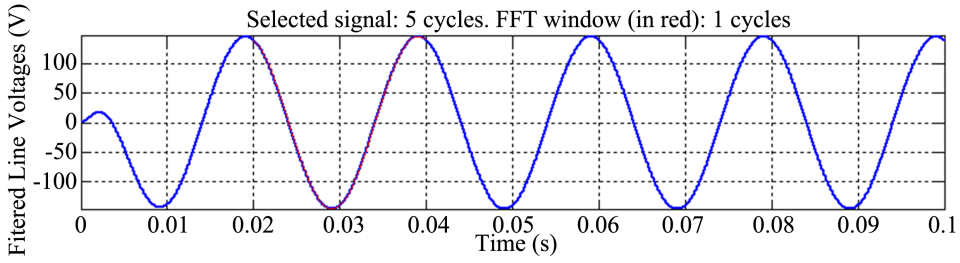


Figure 18. Filtered line voltage.

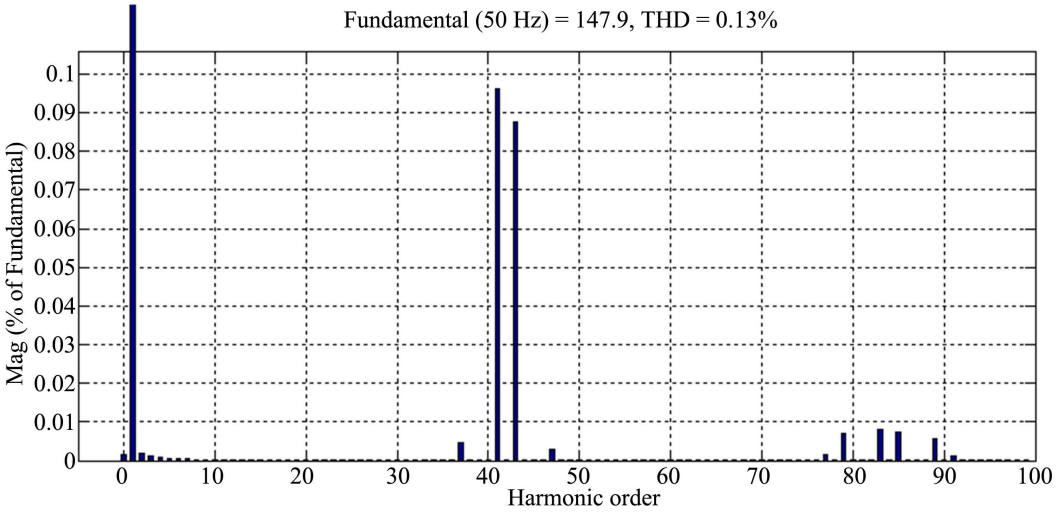


Figure 19. Spectrum of filtered line voltage.

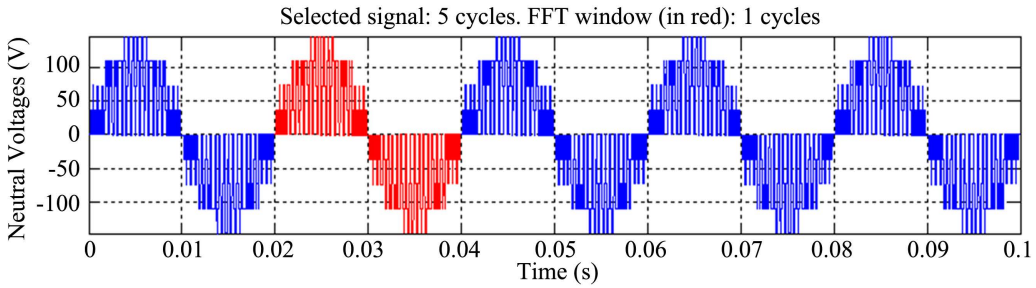


Figure 20. Output voltage between phase and neutral.

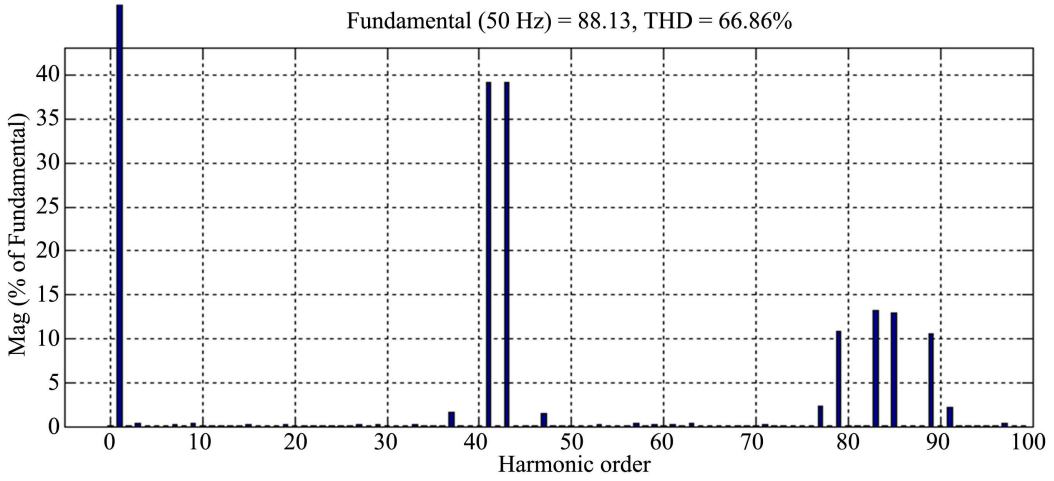


Figure 21. Spectrum of the output voltage between phase and neutral.

The harmonic spectrum of the output voltage V_{ab} for the SPWM command obtained (**Figure 13**) shows that the harmonics are repelled at high frequencies which will allow easy filtering. **Figure 14** and **Figure 15** show respectively the waveform and the current harmonic spectrum of phases a, b and c obtained at the output of the 5L-SMC H-bridge three-phase multicellular inverter.

The harmonic spectrum of the output currents I_{abc} for the SPWM control obtained (**Figure 15**) shows that the output currents include harmonics, with a low THD.

Figure 16 and **Figure 17** show the waveform and harmonic spectrum of the line voltage between phase a and phase b (V_{ab}), respectively.

The harmonic spectrum of the line voltage (**Figure 17**) shows that harmonics are repelled at high frequencies which will also allow easy filtering.

Figure 18 and **Figure 19** show respectively the waveform and the harmonic spectrum of the line voltage filtered between phase a and phase b obtained at the output of the second order filter.

We note the second order filter allows the line voltage signal to be refined and pushes higher order harmonics towards higher frequencies. **Figure 20** and **Figure 21** respectively show the waveform and the harmonic spectrum of the output voltage between phase and neutral obtained at the output of the inverter.

The harmonic spectrum of the output voltage (**Figure 21**) shows that harmonics are repelled at high frequencies which will allow easy filtering. The simulation results of the proposed 5L-SMC H-bridge three-phase multicell inverter (**Figures 12-21**) compared from the point of view of THD with those of the NPC, SMC and H-bridge inverter carried out under the same conditions and for the same simulation parameters, are presented in **Table 4** below.

We observe that the output voltages (between phase, line, between phase and neutral) of the proposed 5L-SMC H-bridge multicell inverter give very high voltage harmonic spectra (of the order of 66%) as the classic H-bridge topology. On the other hand, the output current gives a THD spectrum equal to 6.17%. The harmonic spectrum of the current is higher than that of the NPC converter (1.72%) and lower than those of the SMC and H-bridge topologies (8.32%), while remaining within the admissible THD margins of the current defined by standard IEC 61000. By applying a second order filter to the line voltages; we obtain smoothed voltages with a spectrum of the order of 0.13% for the 5L-SMC H-bridge and NPC inverters compared to that of the SMC and H-bridge converters respectively of 4.86% and 0.29%. This converter makes it possible to obtain an AC voltage of 220 V at the output from a DC voltage of 220 V, which means that no voltage drop is observed in this converter. From the above, the proposed 5L-SMC H-bridge multicell inverter gives better performance from the THD point of view of the output voltage. This converter appears as an interesting structure when the number of output voltage levels increases [19] [24] [27]. It also makes it possible to push back certain limitations of the basic structures (SMC and H-bridge), such as the inequality of the reverse voltages supported by the diodes, removed all looping diodes and used bidirectional switches [2] [9] [24]. The proposed converter makes it possible to eliminate the problem of blocking diodes in the NPC topology and its variants, to impose a blocking voltage equal to V/2 on all switches, to eliminate the problem of their voltage imbalance with the absence of capacitors between different levels [27] [29] [30].

Table 4. Comparison of simulation results under Matlab/Simulink from the THD point of view.

		NPC [11] [20]	SMC [8] [20]	H-bridge [8] [17] et [20]	Proposed 5L-SMC H-bridge
THDV (%)	Output voltage between phase	67.23	77.41	66.66	66.90
	Line voltage	67.15	77.46	66.86	66.86
	Output voltage between phase and neutral	67.15	77.46	66.87	66.86
	Filtered line voltage	0.13	4.86	0.29	0.13
THDI (%)	Output current	1.72	8.32	8.32	6.17

5. Conclusion

In this paper, a new three-phase inverter structure is presented. This new topology makes it possible to distribute the voltage constraints of the converter between several switching cells. It also makes it possible to divide the input voltage into several fractions so as to lower the number of switching power semiconductors. Simulations are performed to record the waveforms of the output voltages and validate this new approach. Finally, it appears that the new 5L-SMC H-bridge structure gives more advantages over its competitors NPC, SMC and H-bridge. The major drawback to note is the high number of switches used. However, many studies can still be carried out; we suggest for this purpose the experimental verification of the proposed approach and the development of harmonic elimination strategies.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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