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Emitter Quality Optimization Using Lightly Doped Phosphorus Diffusion and Thermal Oxide Anneal for Cell Efficiency Improvement in Multi-Crystalline Black Silicon Solar Cells

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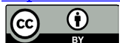
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Abstract

Improving solar cell performance by increasing solar cell efficiency by various process optimization had always been a simple straight-forward methodology followed in a R&D or in a solar cell manufacturing company. This is also the most cost-effective practice to improve a product performance using the same technology without the need to procure alternative or expensive raw materials or by adopting advanced solar cell processing techniques. Aluminium Back Surface Field (Al-BSF) technology using multi-crystalline wafers (mc-Si) had been a well-established and a dominant product in the solar industry for more than two decades. However, as the industry progresses, the demand for high efficiency solar cells and modules started going up and full area Aluminium BSF based cells suffers from a lot of inherent limitations on cell efficiency. This is primarily due to the intrinsic high density of crystal lattice defects or otherwise called as grain boundary defects present dominantly only in mc-Si wafers. These grain boundaries tends to accumulate several defects and become trap centres which cause high recombination for minority carriers thereby exhibiting lower conversion efficiency and higher dispersion in electrical parameters in batches of tested cells. Years of research using this material have helped to derive the maximum benefits using this mc-Si wafer in producing industrial full area BSF cells and we can say with certainty that the efficiency potential has reached the saturation point with this technology. An interesting development that happened in the area of improving the final product performance using mc-Si wafers at both cell and module level, is by replacing the conventional acid texturing process with an introduction of a nano-texturing process called Metal Catalysed Chemical Etching (MCCE) using specialized chemicals which improves the light trapping capabilities by creation of inverted pyramid texture on the silicon wafer surface and thereby enabling the wafers to absorb sunlight over a broader range of wavelength

and incident angle. With this development done in mc-Si wafers in recent past, it is still a daunting task to surpass cell efficiencies beyond 19.0% using this wafer source. Hence for cell manufacturing lines which use mc-Si wafers, there is always a constant need to improve the cell manufacturing processes to reduce the impact of poor intrinsic quality of mc-Si wafers and improve the final product performance without adding any significant cost factor.

Keywords

Lightly Doped Emitter, Oxidation, Annealing, Metal Catalyst Chemical Etching, Phosphorus Silicate Glass, Diffusion

1. Introduction

Black silicon wafers had been a material of interest for photovoltaic devices for more than two decades now due to its unique surface morphology, enhanced optical and electronic properties [1] [2]. The micro structured surface made possible by silicon processing techniques like Reactive Ion Etching (RIE), Metal Catalyst Chemical Etching (MCCE), laser irradiation etc., enables improved light absorptance in visible and infrared wavelengths of light spectrum [2]. The absorptance of light is also influenced by the energy levels of dopants, which can be tailored to achieve a uniformly low surface dopant concentration, sufficient to make a good ohmic contact with the screen printed metal pattern and yet achieve a reduced Auger and metal recombination in solar cells [3].

The aim of this work is to optimize a solar cell emitter quality by developing a lightly doped tube diffusion process using phosphorus dopants and by introducing a thermal oxide anneal to improve solar cell efficiency using 158.75 mm full square multi-crystalline black silicon wafers. A lightly doped emitter was achieved using Phosphorus Oxy Chloride ($POCl_3$) as a diffusion pre-cursor in an industry standard phosphorus tube diffusion furnace. Thermal oxide anneal was achieved using dry oxidation process with Oxygen (O_2) ambient in an industry standard horizontal tube furnace. An absolute cell efficiency improvement of 0.22% was realized by selecting the best optimized recipe conditions for phosphorus diffusion and oxidation anneal process respectively. In a high volume solar cells manufacturing company, a 0.22% cell efficiency gain could translate to an additional revenue of over US$ 200 k per year, with a simple recipe optimization of existing processes. The novelty approach used in this work is to use the best processes available to achieve improved cell performance using an efficiency limiting material like multi-crystalline wafers and without a need to add any additional cost adding process to cell manufacturing.

2. Experimental Work

There are multiple methods to achieve a Lightly Doped Emitter (LDE) with reduced phosphorus dopant concentration in order to reduce the surface recom-

bination velocity and Auger recombination in silicon solar cells [4] [5] [6]. The most commonly used approach in tube based diffusion process will be to enhance the growth of Phosphorus Silicate Glass (PSG) layer which is formed during the deposition step. This helps to improve the Phosphorus gettering process thereby reducing the electron-hole recombination mechanism at grain boundary defect sites typically found in multi-crystalline wafers [7] [8]. In this work, diffusion process parameters which directly contribute for PSG layer thickness and quality were optimized by recipe optimization at deposition, drive-in and cool down steps. Low pressure (LP) diffusion process used in this work was split into six recipe groups, two being baseline (B1 and B2) and four other as trial recipe groups (T1, T2, T3 and T4) aimed at optimizing the PSG layer thickness and subsequent phosphorus dopant concentration.

The low pressure diffusion process consists of a three step deposition in which the thickness of PSG layer is increased by an additional deposition step as compared to the two step deposition process used in the baseline recipe (group B1). All three deposition steps are done at an incremental deposition temperature of 765˚C, 780˚C and 800˚C with a decremental N_2-$POCl_3$ flow of 110 sccm, 90 sccm and 80 sccm in each deposition step respectively (group T1). O_2 flow was varied in trial group T2 as compared to baseline group B2. The impact of these two gas flows were directly studied from the electrical results of each trial group and direct comparison to baseline groups. All other process parameters were maintained the same in order to achieve a sheet resistance target of 115 ± 5 Ω/sq.

Trial groups T3 and T4 were processed using a combination technique of combining gas flow conditions used in trial groups T1 and B2 and in addition, subjecting T3 and T4 group wafers for an oxidation anneal at 780˚C and 750˚C respectively after diffusion and chemical edge isolation processes. Remaining processes from wafer cleaning to screen printing process were kept the same to realize the cell efficiency gain by process optimization of LP diffusion and oxidation anneal process. In this work, oxidation anneal was carried out in a de-commissioned $POCl_3$ diffusion furnace after replacing the used process tube with a new tube. Hence, technically speaking, though it is an additional process step, it must be noted that there was no additional equipment cost involved.

Figure 1 shows the process flow schematic followed for the processing of baseline and trial group of wafers as explained in **Table 1** and **Table 2** indicates the diffusion process conditions used for trial group of wafers.

While trial groups T1 and T2 underwent three step deposition in diffusion process with baseline (3 slm) and reduced O_2 flow (1.5 slm) respectively, T3 and T4 were combination trial of T1 + B2, using three step deposition + higher O_2 flow (3 slm) in baseline diffusion process. The oxide anneal process groups consists of a thermal oxidation step using oxygen at 500 sccm for 20 minutes at 750˚C and 780˚C which were used for trial groups T3 and T4 respectively. The resulting Silicon Oxide (SiO_2) is a very thin layer in the range of 5 to 10 nm which acts as an effective underlying field effect passivation layer along with

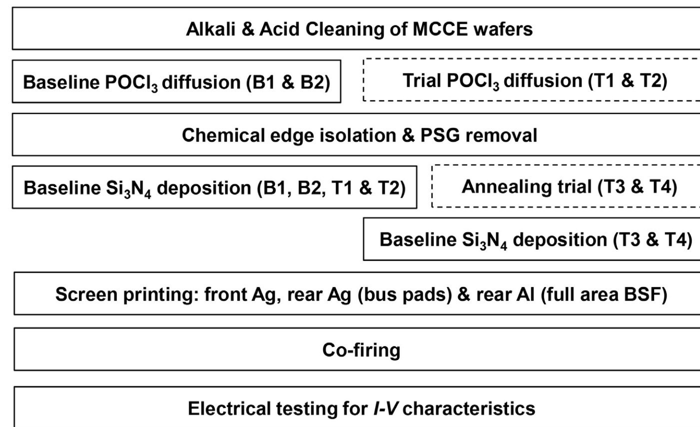

Figure 1. Process flow schematic of cell processing for baseline and trial groups of wafers.

Table 1. Indicates the baseline and trial group Design of Experiment (DOE) for diffusion and oxidation anneal processes along with optimized process parameters.

Groups	Process step	Parameters	Values	Remarks
B1	Deposition	N_2-$POCl_3$ flow rate	90 + 90 sccm	Baseline
B2	Drive-in	O_2 flow rate	3 slm	Baseline
T1	Deposition	N_2-$POCl_3$ flow rate	110 + 90 + 80 sccm	Trial
T2	Drive-in	O_2 flow rate	1.5 slm	Trial
T3	Annealing	Anneal temperature	780˚C	Combination trial
T4	Annealing	Anneal temperature	750˚C	Combination trial

Table 2. Shows the summary of process conditions used for the three deposition step deposition process. The temperature and gas flow conditions used in this trial recipe are indicated in bold.

LP $POCl_3$							
Step #	Time	Temp	N_2	$POCl_3$	O_2	Pressure	Remarks
UOM	Min	˚C	sccm	sccm	sccm	mbar	
1	10	790	15,000				Boat In
2	8	765					Heat-up + Pump Down
3	1	765	1000			50	Stabilize + Purge + Pre-Ox
4	5	**765**	430	**110**	350	50	Deposition1
5	3	780	430		350	50	Ramp up
6	5	**780**	430	**90**	350	50	Deposition 2
7	3	800	430		350	50	Ramp Up
8	5	**800**	430	**80**	350	50	Deposition 3
9	10	820	5000		**3000**	200	Drive-In
10	5	815	3000		0		Cool-Down
11	10	790	15,000				Boat-Out

capping silicon nitride (Si_3N_4) layer to minimize surface reflection and charge carrier recombination losses [9] [10]. It must be noted that for the oxidation anneal trial groups, the Ozone deposition process condition was turned off during edge isolation and PSG removal in chemical edge isolation process. This was done due to the fact that an Ozone deposition process at the end of chemical edge isolation process will form a thin layer of SiO_2, which instead is thermally grown in oxidation anneal process. This formed oxide layer substitutes for chemically grown SiO_2 from chemical edge isolation process. There had been quite a number of research articles which state that the quality of thermally grown SiO_2 over chemical oxide layers is superior for intrinsic surface passivation quality [11] [12]. **Table 3** indicates the process conditions used for oxidation anneal process for the trial group of wafers.

The diffusion and annealing process recipe steps are schematically represented as shown in **Figure 2**.

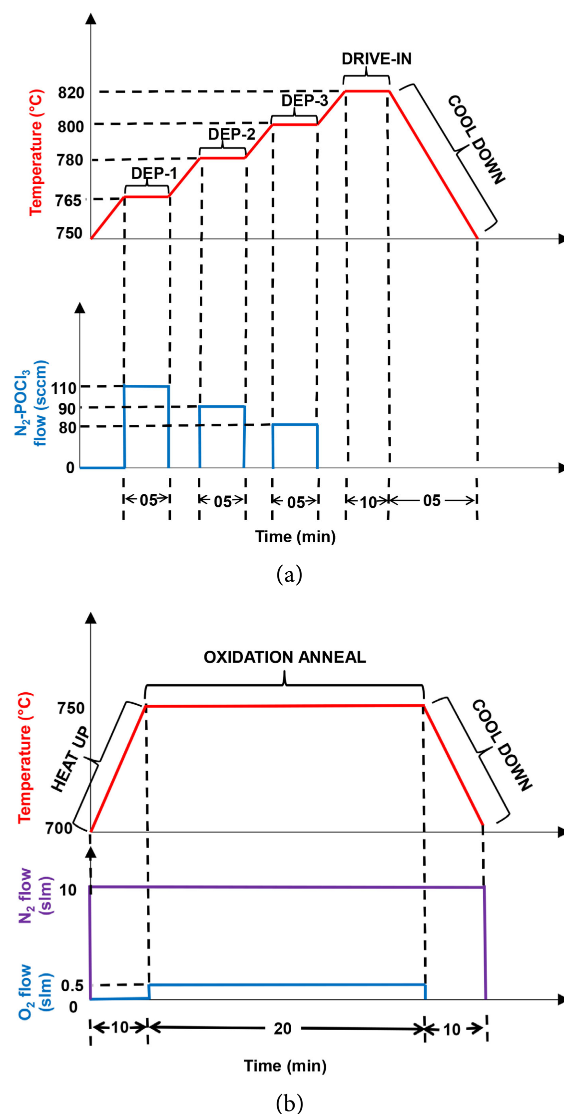

Figure 2. Process schematic of low pressure diffusion (a) and oxidation anneal conditions (b).

Table 3. Shows the summary of process conditions used for the oxidation anneal process. Only the process temperature was varied between the trial groups T3 and T4 which are indicated in bold.

Step #	Time	Temp	O_2	Pressure	Remarks
UOM	Min	˚C	sccm	mbar	
1	10	700	0	1060	Boat-In
2	10	750	0	200	Heat-Up + Pump Down
3	20	**780 and 750**	**500**	200	Oxidation Anneal
4	10	700	0	200	Cool-Down
5	10	700	0	1060	Boat-Out

3. Results

I-V measurements:

The two baseline and four trial groups were processed using the same process conditions except for diffusion and annealing process. As explained in **Table 1**, while the N_2-$POCl_3$ and O_2 gas flows were varied in the LP diffusion process for trial groups B1, B2, T1 and T2, trial groups T3 and T4 were subjected to a combination of T1 and B2 process conditions from diffusion process and an oxidation anneal process was tried at two different temperature conditions (780˚C and 750˚C) respectively.

Figure 3 shows the average cell efficiency trial group wise. From the results, it is evident that the cell efficiency improves from baseline 2-step diffused groups B1 and B2 to 3-step diffusion process groups T1 and T2 and further increases when subjected to an oxidation anneal process for groups T3 and T4.

Table 4 summarizes the overall average efficiency of baseline groups (B1 and B2) using a 2-step diffusion process was 18.80% which increases to an average efficiency of 18.86% after changing to a 3-step diffusion process (T1 and T2). This further increases to an efficiency of 18.94% after being subjected to an oxidation anneal process at 780˚C (T3), and final group efficiency to 19.02% after being subjected to an oxidation anneal process at 750˚C (T4), thereby achieving an overall efficiency gain of 0.22% when compared to baseline group. The efficiency gain achieved in this work was realised with an improvement of 4 mV in open circuit voltage (V_{oc}), 40 mA in short circuit current (I_{sc}) and 0.12% in fill factor (FF).

Post anneal treatment in silicon solar cell always been demonstrated to improve the electrical performance of the device due to its ability to reduce and repair the structural defect damage induced during high temperature process like diffusion in cell processing stages [13] [14]. Annealing also helps to improve the carrier mobility without affecting the surface morphology on silicon wafer surface [15]. Annealing process is also a proven process technique followed in solar cell processing for Passivated Emitter Rear Contact (PERC) solar cells, which helps to boost solar cell efficiency substantially [16]. Both the techniques of

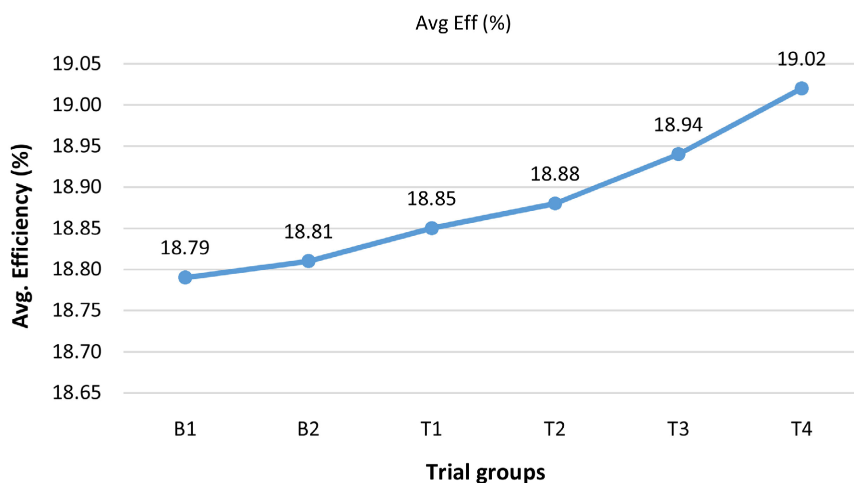

Figure 3. Average cell efficiency of baseline and trial groups processed using various conditions.

Table 4. Summary of average cell efficiency of baseline and trial groups.

Groups	Eff	Voc (mv)	Isc (A)	FF (%)	Rsh (Ω)	Rs (mΩ)	IRev1 (A)	IRev2 (A)
B1	18.79%	634.1	9.266	80.57	196.0	2.355	0.325	0.466
B2	18.81%	634.4	9.261	80.68	261.5	2.277	0.309	0.456
T1	18.85%	639.2	9.199	80.79	422.1	2.302	0.238	0.359
T2	18.88%	638.4	9.228	80.76	289.0	2.268	0.319	0.489
T3	18.94%	637.0	9.266	80.87	142.6	2.237	0.319	0.439
T4	**19.02%**	638.0	9.305	80.75	611.4	2.209	0.183	0.297

diffusion and anneal process optimization were carried out in this work using a highly absorbent textured silicon surface like black silicon had helped to gain a significant improvement in photo current generation, reduced recombination losses and lower threshold voltage. It must be also be mentioned that from the electrical results summarized in **Table 4**, the shunt resistance (Rsh) has greatly improvement resulting in reduced reverse current (I_{rev}) values for T4 group as compared to other test groups.

4. Analysis

Quasi steady state photoconductance (*QSSPC*) *measurements*:

In order to analyse the cell efficiency gain observed from oxidation anneal trial group, QSSPC measurements were carried out using passivated samples prepared by dividing the wafer samples into three groups as shown in **Table 5**. All these group of wafers were deposited with a double-sided anti-reflective coating (ARC) of 80 nanometres (nm) silicon nitride (Si_3N_4) using an industry standard Plasma Enhanced Chemical Vapour Deposition (PECVD) reactor. Samples were subsequently co-fired in a standard industrial co-firing furnace at

Table 5. Shows the trial groups prepared from regular solar cell processing for QSSPC measurement.

S. No	Process	Measurements	Remarks
1	Texture and Clean + PECVD Si_3N_4 (double side) + Co-fire	QSSPC	Textured wafers + Si_3N_4 passivation
2	Texture and Clean + Diffusion + Edge isolation + PECVD Si_3N_4 (double side) + Co-fire	QSSPC	Baseline wafers + Si_3N_4 passivation
3	Texture and Clean + Diffusion + Edge isolation + Anneal + PECVD Si_3N_4 (double side) + Co-fire	QSSPC	Trial wafers + Si_3N_4 passivation

a peak temperature of 850˚C for hydrogen passivation using the elemental hydrogen generated from the deposition process of a-SiN:H to form a Si_3N_4 dielectric layer. QSSPC measurements were carried out at a high-injection minority carrier density (MCD) of $3e^{15}$ cm^{-3} in order to estimate the effective minority carrier lifetime (τ_{eff}), saturation current density (Jo) and implied voltage (i_{Voc}) for the baseline and trial group of wafers.

From the QSSPC results in **Figure 4**, it is evident that there is an improvement in the measured values of τ_{eff}, i_{Voc} and J0e which can be observed to show a linear trend with best optimum results achieved for the anneal oxidation group of wafers (group 3). From this measurement, the best results were 90 µsec for $\tau_{eff,}$ (**Figure 4(a)**) 88 fA/cm^2 for J0e (**Figure 4(b)**) and 690 mV for i_{Voc} (**Figure 4(c)**) were achieved using multi-crystalline double side Si_3N_4 passivated wafers. These results are further convincing on the fact that an anneal oxidation process helps with better surface and bulk passivation, leading to improved results from QSSPC measurements and subsequently from *I*-*V* measurements.

It must be noted that for the QSSPC measurements, samples were taken from the same batch of wafers which were used in the cell fabrication process for baseline and all trial groups to avoid any lot-to-lot variation coming from incoming wafer quality. A linear trend is observed for all the parameters (τ_{eff}, i_{Voc} and J0e) with improved results observed for the oxidation anneal samples (Group 3) and these results further correlates and supports the improved cell efficiency gain observed for oxidation anneal group (T4) as summarized in **Table 4**.

Spectral Response measurements:

Spectral response was measured on selected solar cell samples from trial groups B2, T2 and T4 representing the various types of process groups as mentioned in **Table 1** using Bentham PVE300 photovoltaic Quantum Efficiency equipment. After measuring the reflectance (R) of each trial sample, the detector spectral response was measured using cells of 18.80%, 18.90% and 19.00% cell efficiency for the measurement of External Quantum Efficiency (EQE) and Internal Quantum Efficiency (IQE). **Figure 5(a)** and **Figure 5(b)** shows the EQE, reflectance and IQE measurements data in which, the oxidation anneal trial

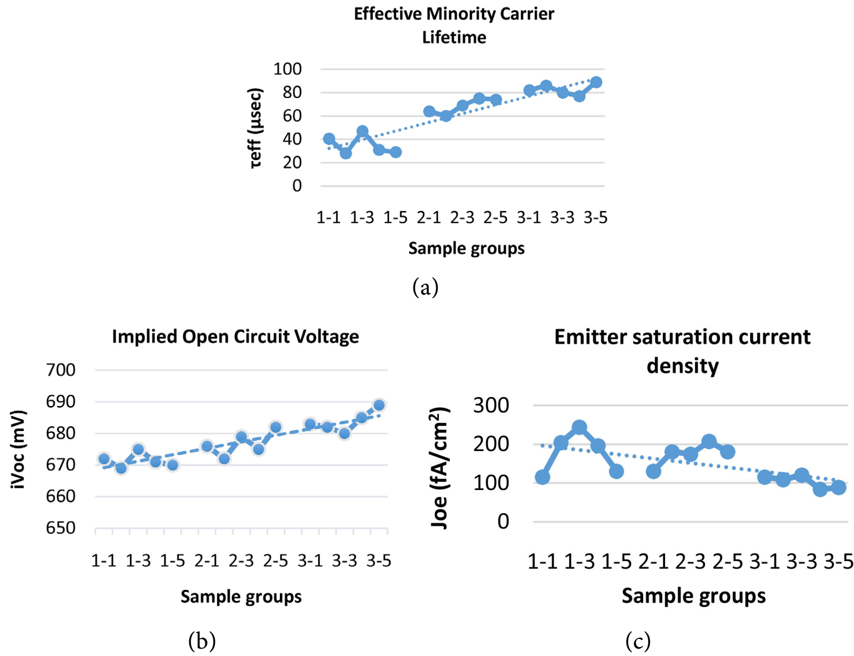

Figure 4. QSSPC measurements on double side Si_3N_4 passivated baseline and trial group samples. (a) τ_{eff} of samples from trial groups; (b) i_{Voc} of samples from trial groups; (c) J_{oe} of samples from trial groups.

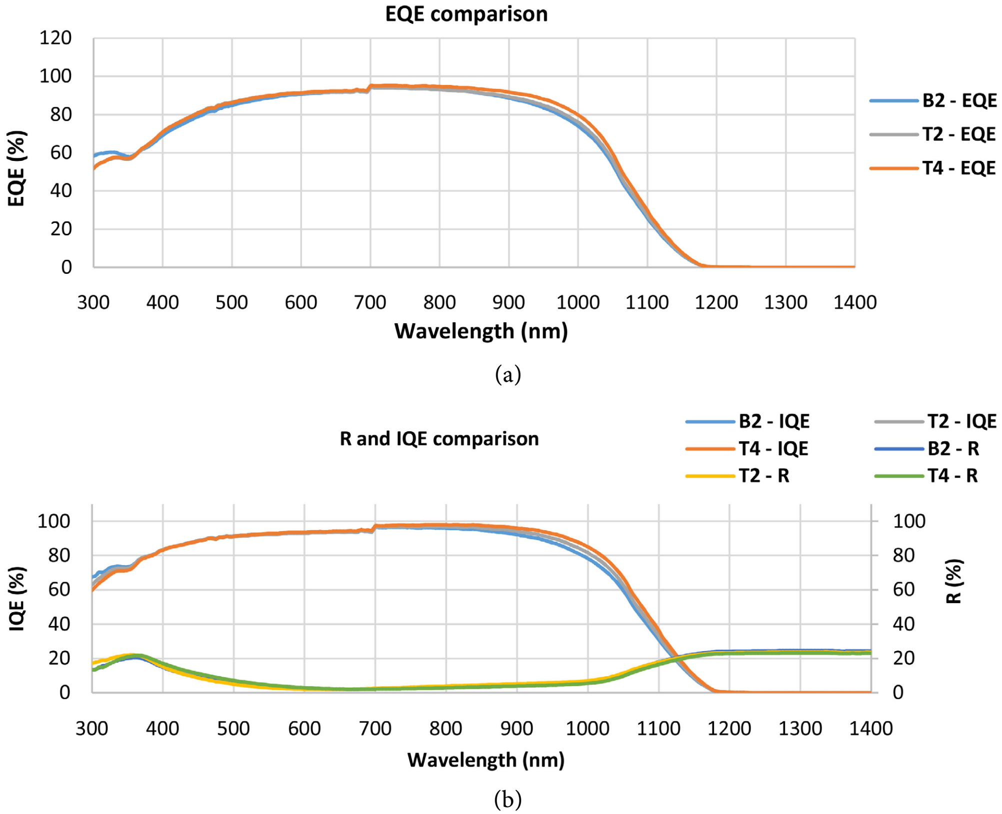

Figure 5. EQE, R and IQE measurements of selective cells taken from B2, T2 and T4 groups. (a) EQE comparison between baseline and trial group of cells; (b) IQE comparison between baseline and trial group of cells.

group (T4) shows a better performance as compared to baseline group, resulting in higher efficiency surpassing 19.0% mark as compared to other two groups.

From the spectral response measurements, an improved performance of EQE and IQE are observed on cells from the oxidation anneal (T4) especially in near Infrared region (700 - 1100 nm), confirming the positive influence of oxidation anneal process on to the improvement of solar cell efficiency. Although the blue response is comparable between baseline and trial groups, resulting in marginal gains of I_{sc} (40 mA) as observed in **Table 4** for groups B1 & B2 versus T4, the main efficiency contribution comes from the significant improvement of V_{oc} (4 mV) between these groups, which is also reflecting with a better red response for trial group T4 as compared to baseline groups.

A lot of extensive research had been done in the past on Selective Emitter (SE) and Lightly Doped Emitter (LDE) using different techniques to achieve a diffused emitter with low doping concentration, as it is key to reduce the minority carrier or Auger recombination in the emitter. As discussed in work carried out by K.D Shetty, *et al.* [4] and Feng Ye, *et al.* [5]. In these works, although the methods used to achieve a low doping concentration were different, like emitter etch-back, pre and post oxidation drive-in techniques at *in-situ* and *ex-situ* diffusion processes, the ultimate intention of those works had been to reduce the Auger recombination and emitter saturation current densities (J_{oe}) in produced solar cells. Similar to these works, in this paper also, the tube diffusion process was optimized to result in low doping concentration by influencing the PSG thickness to achieve better phosphorus gettering process. This technique when combined with a post-diffusion oxidation anneal process helps to improve the effective minority carrier lifetime (τ_{eff}), implied (i_{Voc}) and actual open circuit voltage (V_{oc}) on lifetime samples and solar cell results, as observed in **Table 4** and **Figure 4** respectively.

For cell manufacturers, processing MCCE black silicon wafers had been quite beneficial in terms of improved cell efficiency, less variation in silicon nitride color resulting in better aesthetics and by employing correct set of materials for both cell and module manufacturing, the cell to module (CTM) loss can also be minimized and made comparable to modules made using cells produced using DWS wafers. In the reported work by Kishan Shetty, *et al.* [17], the challenges in processing DWS and MCCE black silicon wafers had been well explained and an average cell efficiency improvement of 0.37% was reported in that work using MCCE black silicon wafers versus DWS wafers. However the average cell efficiency reported was below 19.0% in that work, which was surpassed in this work, by further optimization of diffusion process and by employing an additional oxidation anneal process, which did not add any additional cost to cell manufacturing, as the oxidation anneal process was carried out using replacing a used process tube with a new process tube in a de-commissioned diffusion furnace. The overall cell manufacturing time with oxidation anneal process increased by 60 minutes, but the cost of it is negligible when compared to overall cell efficiency gain achieved in this work.

5. Conclusions

Improving the cell efficiency using mc-Si wafers has reached a saturation limit after several years of extensive research carried out for different process optimizations to improve overall device performance using this wafer source. While DWS mc-Si wafers technology resulted in better yield than SWC mc-Si wafers for wafer manufacturers, change-over from DWS to MCCE wafer source yielded in a cell efficiency gain of 0.3% for most of the cell manufacturers who have done this migration. This efficiency gain of 0.3% is not attributed to only change in wafer type, but inclusive of cumulative gains achieved in MCCE nano-texturing and other process improvements done best suited for this wafer type in a high volume manufacturing environment. In order to reduce manufacturing costs and remain competitive in the industry, it is very important to constantly improve the device performance by usage of high performance raw materials and by re-optimization of cell manufacturing processes.

In this work, a cell process re-optimization involving low pressure diffusion and oxidation anneal processes were carried out in this work leading to a cell absolute efficiency improvement of 0.22% using multi-crystalline black silicon solar wafers. A three-step deposition technique with gradient decremental flow of Phosphorus Oxy Chloride ($POCl_3$) was adopted in the diffusion process, to create a denser PSG layer and increased phosphorus gettering process. This process when combined with an oxidation anneal process helps to achieve a good field effect passivation thereby resulting in a lightly doped emitter with reduced Auger recombination loss and emitter saturation current densities, thereby resulting in an improved device performance for cells processed with trial conditions as compared to baseline conditions. Although the oxidation anneal was an additional process in the cell manufacturing process flow to produce standard full area Al-BSF cells, the cost incurred for this additional process step was indemnified by the cell efficiency gain of 0.22%, which gives an additional revenue of US$ 200 k per year to the company.

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Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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