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Physical Parameter Variation Analysis on the Performance Characteristics of Nano DG-MOSFETs

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Abstract

DG-MOSFETs are the most widely explored device architectures for nano-scale CMOS circuit design in sub-50 nm due to the improved subthreshold slope and the reduced leakage power compared to bulk MOSFETs. In thin-film (t_{si} < 10 nm) DG-MOS structures, charge carriers are affected by t_{si}-induced quantum confinement along with the confinement caused by a very high electric field at the interface. Therefore, quantum confinement effects on the device characteristics are also quite important and it needs to be incorporated along with short channel effects for nano-scale circuit design. In this paper, we analyzed a DG-MOSFET structure at the 20 nm technology node incorporating quantum confinement effects and various short channel effects. The effect of physical parameter variations on performance characteristics of the device such as threshold voltage, subthreshold slope, I_{ON} - I_{OFF} ratio, *DIBL*, etc. has been investigated and plotted through extensive TCAD simulations. The physical parameters considered in this paper are operating temperature (T_{op}), channel doping concentration (N_c), gate oxide thickness (t_{ox}) and Silicon film thickness (t_{si}). It was observed that quantum confinement of charge carriers significantly affected the performance characteristics (mostly the subthreshold characteristics) of the device and therefore, it cannot be ignored in the subthreshold region-based circuit design like in many previous research works. The ATLAS™ device simulator has been used in this paper to perform simulation and parameter extraction. The TCAD analysis presented in the manuscript can be incorporated for device modeling and device matching. It can be used to illustrate exact device behavior and for proper device control.

Keywords

Nano DG-MOSFET, Quantum Confinement Effects, Thin Film Structures, Short Channel Effects, Performance Characteristics

1. Introduction

The conventional bulk MOSFETs pose scaling limitations beyond 50 nm technology node because of increased Short Channel Effects (SCEs), increased gate-oxide tunneling currents [1] [2] and remarkable mobility degradation [3] [4] [5]. These scaling limits can be overcome by the use of DG-MOSFET structures. Unlike bulk MOSFETs, DG-MOS architectures have two gates which provide an enhanced gate-to-channel coupling capacitance, and therefore, they suffer less from SCEs. The enhanced electrostatic coupling between the gate and the channel allows DG-MOSFETs to be designed with intrinsic channels and hence the problem of mobility degradation and random dopant fluctuations are eliminated in these devices. DG-MOSFETs with ultra-thin (Si) bodies are now being seriously explored for nano-scale CMOS circuit design. In such architectures (with $t_{si} < 10$ nm and $t_{ox} < 3$ nm), quantum effects become prominent and they must be taken care of in the analysis and modeling of such devices [6] [7]. As shown in this paper, quantum effects significantly affect device characteristics such as threshold voltage (V_t), transconductance (g_m), subthreshold slope (SS), etc. The TCAD analysis can be incorporated for device modeling and device matching. It can be used to illustrate exact device behavior and for proper device control. It can also be used for checking technological parameter fluctuations, reliability evaluation factors, etc.

The results are demonstrated by extensive 2-D TCAD simulation and confirmed analytically at various technology nodes to validate the robustness of the model. Hence, the proffered physical models and the proposed device may be utilized in the progression of reliable and trustworthy TCAD simulation tools for nanodevices. The proposed Nano-DG-MOSFET is the confirmed upcoming device of ultra-low-power VLSI and high-frequency applications. This nano-device can definitely replace the conventional bulk MOSFETs in the future for low power circuits.

2. Methodology

2.1. General Structure

The double gate structure as shown in **Figure 1** consists of two gate electrodes: front gate and back gate controlling a conducting channel in between.

2.2. Advantages of DG MOSFET

DG-MOSFETs can easily be scaled down beyond 50 nm technology node due to better immunity to short channel effects. This is because of the enhanced gate to channel coupling capacitance provided by the two gates on either side of the channel. The DG-MOS architectures can be designed with low doped channels which give better carrier mobility and hence, better switching time. The leakage power dissipation caused by off-state currents are minimized in DG-MOSFETs as compared to bulk MOSFETs. The DG-MOSFETs have better current driving

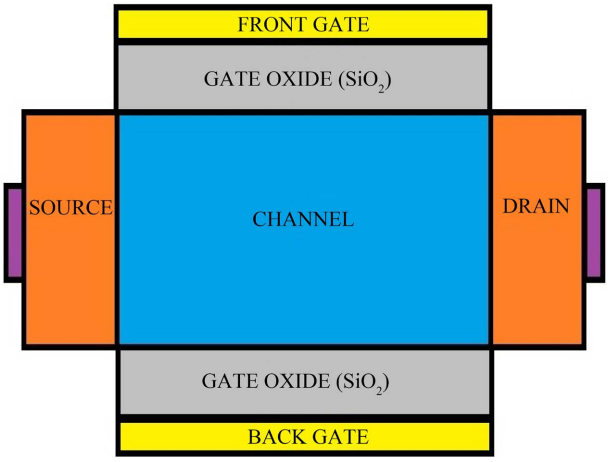

Figure 1. Schematic of a double gate MOSFET.

capability and hence they can be used at much lower threshold and input voltages and consequently power consumption is reduced in DG-MOSFETs. Since no part of the channel is too far away from the two gates, channel current is better controlled by the gate electrodes that gives ideal sub-threshold slope required for sub-threshold region based circuit design [6] [7] [8].

2.3. Quantum Confinement Effect

In order to minimize the drastic increase of short channel effects in highly scaled DG-MOSFETs, very thin oxides and highly doped channels are required which results in very high electric field at the interface. This high electric field leads to the formation of potential well sufficiently steep for inducing quantization of carrier energy levels. The charge carriers then follow the physics of tightly confined particles and they require quantum mechanical treatment. In DG-MOSFETs, carriers are confined due to two main phenomenon: first one is the confinement caused by very high electric field at the interface when oxide thickness is very less ($t_{ox} < 3$ nm) (known as electric field induced quantum confinement and second one is due to the confinement caused by ultra-thin Si film thickness ($t_{si} < 10$ nm) (known as t_{si} induced structural quantum confinement). The effect of these confinements on the device characteristics such as threshold voltage and drain current are quite important. For DG-MOSFETs with Si-film thickness less than 10nm, quantum effects must be incorporated in the analysis and modeling of such device architectures [9] [10] [11].

2.4. Simulation Methodology

The device structure is designed as per the ITRS guidelines and simulated using Silvaco ATLAS Deckbuild editor. Bohm Quantum Potential (*BQP*) model has been used for incorporating quantum effects; incomplete ionization has been activated in order to account for impurity freeze-out at low temperature. Mobility degradation due to surface roughness scattering and acoustic phonon scattering and concentration dependent mobility is taken care by Lombardi CVT Mobility Model.

Shockley-Read-Hall (*SRH*) model has been used to take recombination effects into account. The impact ionization of carrier under high lateral electric field along with Fermi carrier statistics has also been activated in simulation. The Constant Current Method (*CCM*) has been used for the threshold voltage extraction and calculation of *DIBL* [12] [13] [14]. V_t is extracted from transfer characteristics by measuring the gate voltage at drain current value $I_D = \frac{W}{L} * 10^{-7} A$, where W is channel width and L is channel length. The $\frac{W}{L}$ ratio used in the work is 50 [15] [16]. The device parameters selected for simulation are as per the guidelines of International technology roadmap for semiconductors [17] (see Table 1).

3. Simulation Results and Discussion

3.1. Effect of Operating Temperature Variation

Figure 2 represents threshold voltage (V_t) and leakage current (I_{off}) variation as a function of channel length for different values of operating temperature (T_{op}). It is evident from the figure that the threshold voltage decreases and leakage current increases with increase in operating temperature at a fixed channel length.

Table 1. Device parameters used for simulation.

Parameter	Value
Channel Doping Concentration, N_c	10^{15} cm^{-3}
Source/Drain Doping Concentration, N_s/N_d	10^{20} cm^{-3}
Source/Drain Region Width, L_S/L_D	5 nm
Silicon Film Thickness, t_{si}	5 nm
Gate Oxide Thickness, t_{ox}	2 nm
Gate Work Function, ϕ_G	4.9 eV

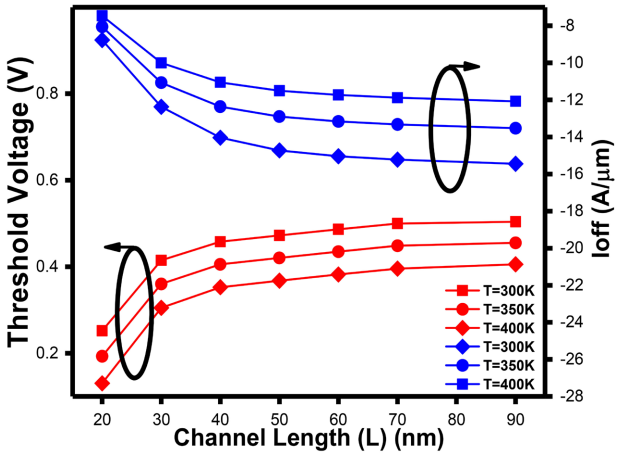

Figure 2. Variation of I_{off} current (in log scale) and threshold voltage with channel length for different values of operating temperature (N_c = 10^{15} cm^{-3}, N_s = 10^{18} cm^{-3}, t_{ox} = 2 nm, t_{si} = 5 nm, ϕ_G = 4.9 eV).

The threshold voltage (V_t) dependence on temperature is modeled as [18]:

$$\frac{\partial V_t}{\partial T} = \frac{\varphi_{ms}}{\partial T} + 2\frac{\partial \varphi_f}{\partial T} + \frac{\gamma}{\sqrt[2]{2\varphi_f}} + \frac{\partial \varphi_f}{\partial T} \tag{1}$$

where φ_{ms} is metal-substrate contact potential, T is operating temperature, φ_f is substrate Fermi potential, γ is body effect coefficient.

As the temperature increases, the first and third term in the equation decreases and second term increases resulting in a net decrease in threshold voltage.

As the threshold voltage decreases with increase in temperature, the leakage current (I_{off}) increases as per the following equation [19]:

$$I_{off} = I_o e^{\frac{V_{GS}-V_t}{nV_T}} \left[1 - e^{\frac{-V_{DS}}{V_T}}\right] \tag{2}$$

where $I_o = \frac{W\mu_o C_{ox} V_T^2 e^{1.8}}{L}$ and thermal voltage $V_T = \frac{KT}{q}$ C_{ox} is gate oxide capacitance, μ_o is the carrier mobility and n is the subthreshold swing coefficient.

In **Figure 3**, variation of I_{on} current and transconductance with channel length for different values of operating temperature is plotted. It can be observed that both the quantities decrease with increasing temperature at a fixed channel length. This is because I_{on} is proportional to $\mu(T)$ and $(V_{GS}\text{-}V_t(T))^2$ term and g_m is proportional to $\mu(T)$ and $(V_{GS}\text{-}V_t(T))$ term. As the temperature increases, $(V_{GS}\text{-}V_t(T))$ term increases because threshold voltage $(V_t(T))$ decreases as discussed earlier and $\mu(T)$ term decreases due to phonon scattering at higher temperature ($T > 300$ K). The decrease in mobility dominates the term $(V_{GS}\text{-}V_t(T))$ which causes I_{on} current and transconductance to decrease at higher temperature [20].

Figure 4 shows the variation of subthreshold slope (SS) and I_{on}-I_{off} ratio with channel length for different values of operating temperature. It is clear from the plot that the subthreshold slope and I_{on}-I_{off} ratio degrades with increasing temperature at a fixed channel length. This may be due to the fact that as the temperature increases, I_{on} current decreases due to mobility reduction caused by phonon scattering and I_{off} current increases because of increase in junction leakage current which approximately doubles for every 10˚C rise in temperature.

Figure 5 shows the variation of $DIBL$ with channel length for different values of operating temperature. $DIBL$ increases with increasing temperature at a fixed channel length. This is due to the fact that the threshold voltage degrades when temperature increases.

3.2. Effect of Channel Doping Variation

From **Figure 6**, the threshold voltage can be found decreasing with increasing channel doping concentration due to the degradation in mobility caused by surface roughness scattering and acoustic phonon scattering. Since, threshold voltage increases with increasing channel doping concentration, the leakage current must reduce according to Equation (2) [21].

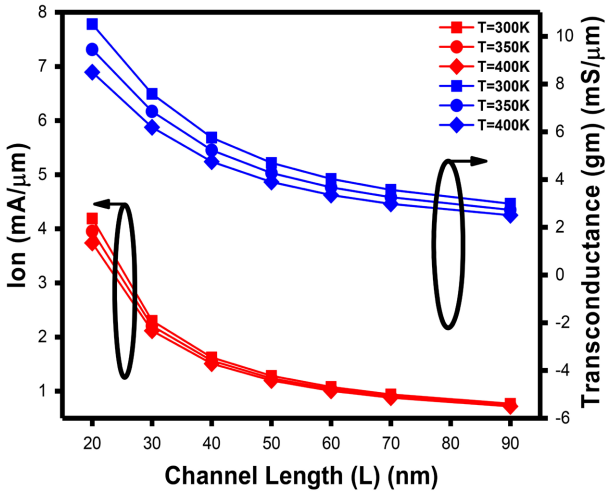

Figure 3. Variation of subthreshold slope and I_{on} - I_{off} ratio (in log scale) with channel length for different values of operating temperature (N_c = 10^{15} cm^{-3}, N_s = 10^{18} cm^{-3}, t_{ox} = 2 nm, t_{si} = 5 nm, ϕ_G = 4.9 eV).

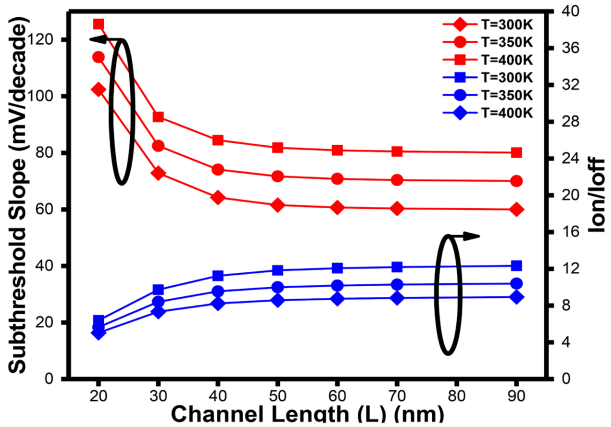

Figure 4. Variation of I_{on} current and transconductance (g_m) with channel length for different values of operating temperature (N_c = 10^{15} cm^{-3}, N_s = 10^{18} cm^{-3}, t_{ox} = 2 nm, t_{si} = 5 nm, ϕ_G = 4.9 eV).

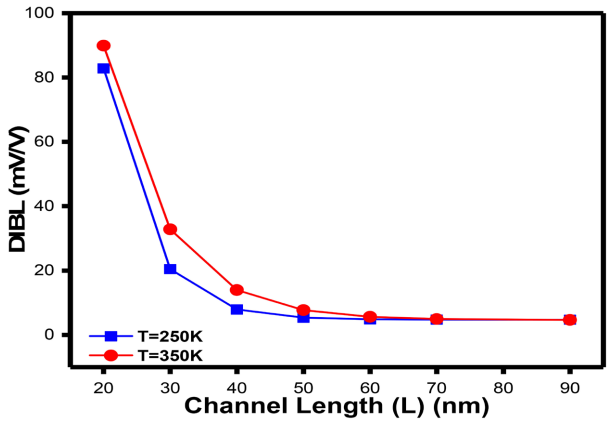

Figure 5. Variation of DIBL with channel length for different values of operating temperature (N_c = 10^{15} cm^{-3}, N_s = 10^{18} cm^{-3}, t_{ox} = 2 nm, t_{si} = 5 nm, ϕ_G = 4.9 eV).

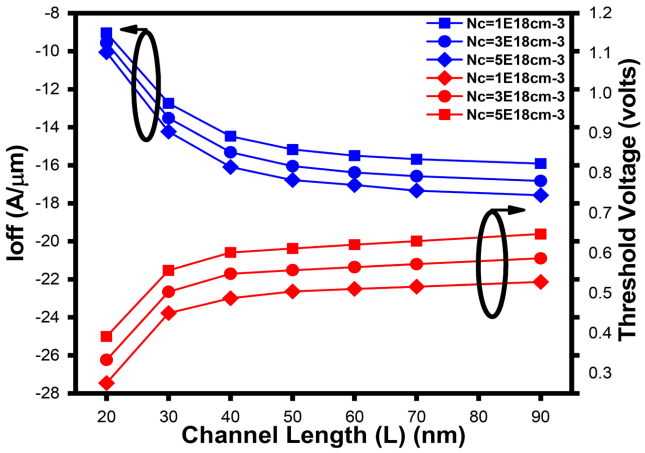

Figure 6. Variation of I_{off} current (in log scale) and threshold voltage with channel length for different values of channel doping concentration ($N_s = 10^{18}$ cm^{-3}, $t_{ox} = 2$ nm, $t_{si} = 5$ nm, $\phi_G = 4.9$ eV).

In **Figure 7**, it is observed that I_{on} current and transconductance decreases with increasing channel doping concentration. This is because of mobility degradation due to columbic scattering and increase in threshold voltage due to increase in Fermi potential of the bulk at high channel doping concentration [22].

Figure 8 represents the variation of I_{on}-I_{off} ratio and subthreshold slope (SS) as a function of channel length for different values of channel doping concentration. It is observed that I_{on}-I_{off} ratio and SS improves at higher channel doping concentration as leakage current (I_{off}) is reduced to a great extent [23] [24].

Figure 9 shows that variation of $DIBL$ with channel length for different values of channel doping concentration. It is found that $DIBL$ is lower for higher channel doping concentration at a fixed channel length due to threshold voltage degradation at high doping concentration.

3.3. Effect of Gate Oxide Thickness Variation

In **Figure 10**, the variation of threshold voltage (V_t) and leakage current (I_{off}) at different channel length for different values of oxide thickness is plotted. It is clear from the plot that the threshold voltage increases with decreasing oxide thickness for a fixed channel length. This can be attributed to quantum mechanical effects due to which peak of the inversion layer is found at a finite distance, d_m away from the interface resulting in increased effective oxide thickness [25]. The effective increase in oxide thickness is given by Equation (3):

$$\Delta T_{OX,QM} = \frac{\varepsilon_{OX}}{\varepsilon_{Si}} d_m \tag{3}$$

Also, due to splitting of allowable energy levels into discrete sub-bands with energy levels above that of the classical conduction band edge, energy band gap increases which results in increased effective Fermi potential. This leads to increase in surface potential and thus in increased value for threshold voltage.

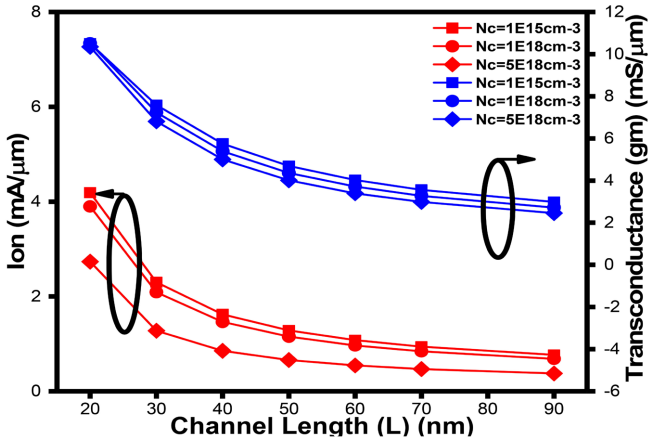

Figure 7. Variation of I_{on} current and transconductance with channel length for different values of channel doping concentration ($N_s = 10^{18}$ cm^{-3}, $t_{ox} = 2$ nm, $t_{si} = 5$ nm, $\phi_G = 4.9$ eV).

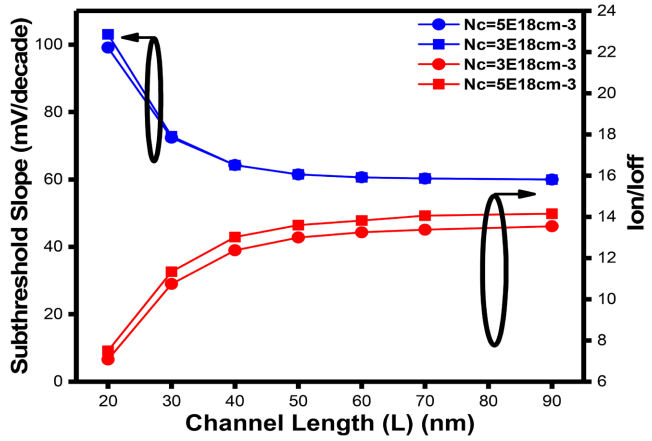

Figure 8. Variation of subthreshold slope and Ion/Ioff ratio (in log scale) with channel length for different values of channel doping concentration ($N_s = 10^{18}$ cm^{-3}, $t_{ox} = 2$ nm, $t_{si} = 5$ nm, $\phi_G = 4.9$ eV).

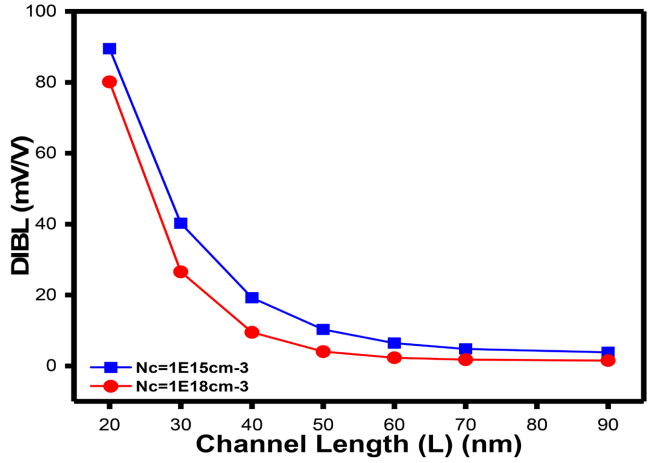

Figure 9. Variation of *DIBL* with channel length for different values of channel doping concentration ($N_s = 10^{18}$ cm^{-3}, $t_{ox} = 2$ nm, $t_{si} = 5$ nm, $\phi_G = 4.9$ eV).

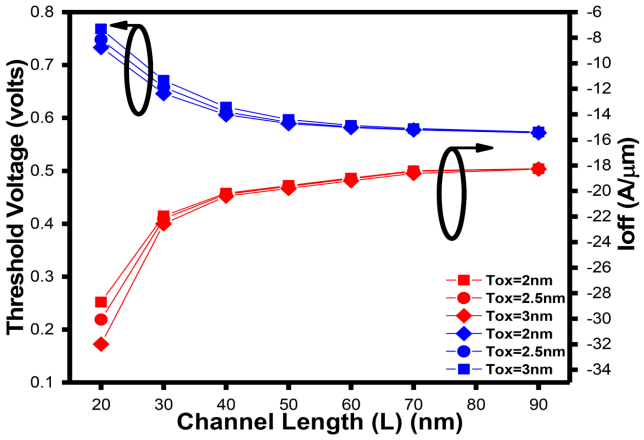

Figure 10. Variation of I_{off} current (in log scale) and threshold voltage with channel length for different values of gate oxide thickness (N_c = 10^{15} cm^{-3}, $N_s = 10^{18}$ cm^{-3}, $t_{si} = 5$ nm, $\phi_G = 4.9$ eV).

From Figure 11, the leakage current can be observed increasing with increase in oxide thickness as the threshold voltage decreases with increased oxide thickness.

Figure 11 shows the variation of I_{on} and transconductance with channel length for different values of oxide thickness. It is evident from the plot that both the quantities decrease with increase in oxide thickness at a fixed channel length. This is because of reduced gate to channel coupling capacitance with increase in oxide thickness.

Figure 12 represents the variation of I_{on}-I_{off} ratio and *SS* with channel length for different values of oxide thickness. As I_{on} current decreases and I_{off} current increases with increase in oxide thickness, I_{on}-I_{off} ratio and *SS* degrades with increase in oxide thickness.

Figure 13 shows the variation of *DIBL* with channel length for different values of oxide thickness. It is observed that device with thicker oxide suffers more from *DIBL* effects. This is due to reduced gate to channel coupling which allows drain to control the channel charges.

3.4. Effect of Silicon Film Thickness Variation

Figure 14 represents the variation of threshold voltage and leakage current with channel length for different Si film thickness values. It is observed from the figure that with decreasing Si film thickness at a fixed channel length, threshold voltage increases. This is because of the fact that the energy quantization increases in channel region with decreasing Si film thickness, $t_{si.}$

The leakage current is observed to increase with increase in Si film thickness at a given channel length due to reduced gate to channel coupling capacitance at higher values of Si film thickness.

Figure 15 shows the variation of I_{on} current and transconductance with channel length for different values of Si film thickness. I_{on} current decreases with decrease in Si film thickness due to increase in energy quantization in channel region

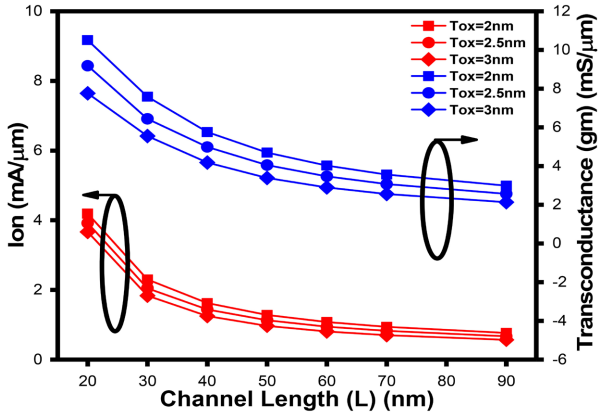

Figure 11. Variation of I_{on} current and transconductance with channel length for different values of gate oxide thickness ($N_c = 10^{15}$ cm^{-3}, $N_s = 10^{18}$ cm^{-3}, $t_{si} = 5$ nm, $\phi_G = 4.9$ eV).

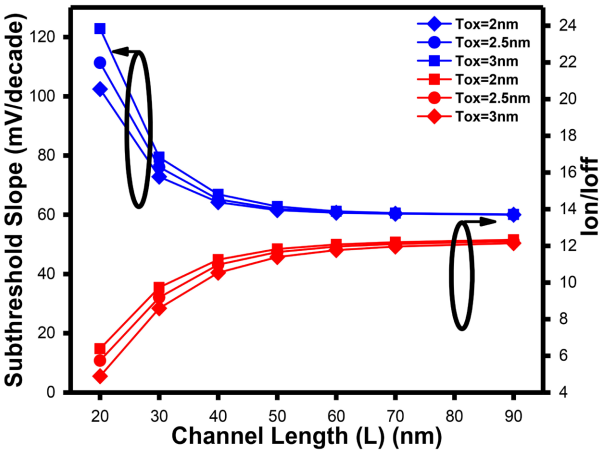

Figure 12. Variation of subthreshold slope and I_{on} - I_{off} ratio (in log scale) with channel length for different values of gate oxide thickness ($N_c = 10^{15}$ cm^{-3}, $N_s = 10^{18}$ cm^{-3}, $t_{si} = 5$ nm, $\phi_G = 4.9$ eV).

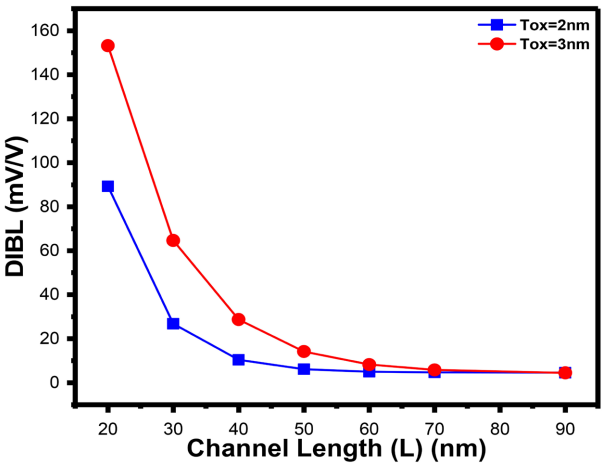

Figure 13. Variation of DIBL with channel length for different values of gate oxide thickness ($N_c = 10^{15}$ cm^{-3}, $N_s = 10^{18}$ cm^{-3}, $t_{si} = 5$ nm, $\phi_G = 4.9$ eV).

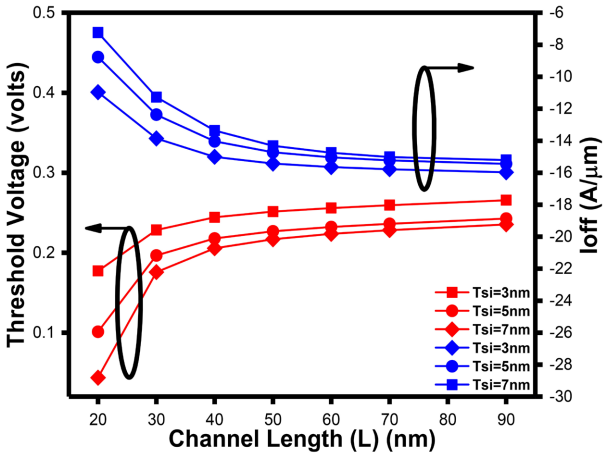

Figure 14. Variation of I_{off} current (in log scale) and threshold voltage with channel length for different values of Si film thickness ($N_c = 10^{15}$ cm^{-3}, $N_s = 10^{18}$ cm^{-3}, $t_{ox} = 2$ nm, $\phi_G = 4.9$ eV).

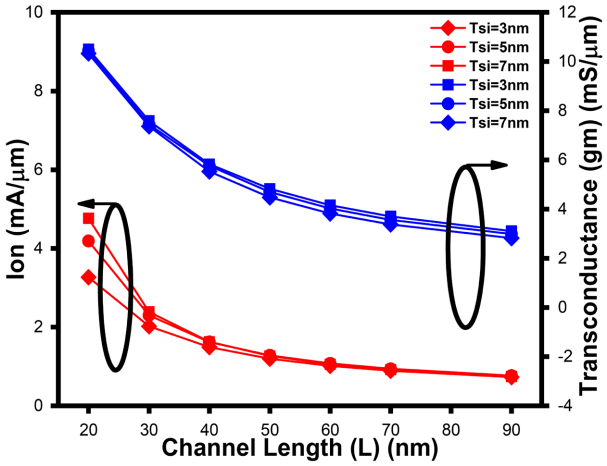

Figure 15. Variation of I_{on} current and transconductance with channel length for different values of Si film thickness ($N_c = 10^{15}$ cm^{-3}, $N_s = 10^{18}$ cm^{-3}, $t_{ox} = 2$ nm, $\phi_G = 4.9$ eV).

that leads to enhanced threshold voltage values. The transconductance value is found to decrease with increase in Si film thickness due to reduced gate to channel coupling.

In Figure 16, variation of *SS* and I_{on}-I_{off} ratio with channel length for different Si film thickness values is shown. The I_{on}-I_{off} ratio is found to decrease with increasing Si film thickness. This is because both I_{on} and I_{off} current increase with increasing Si film thickness but increase in I_{off} is more as compared to I_{on}. Therefore, the ratio I_{on}-I_{off} decreases with increase in Si film thickness. The *SS* is observed to improve with decreasing Si film thickness as I_{on}-I_{off} ratio is enhanced when Si film thickness is reduced.

Figure 17 shows the variation of *DIBL* as function of channel length for different values of Si film thickness. It can be observed that the *DIBL* effect is negligible for longer channel length devices. The *DIBL* effects are more prominent

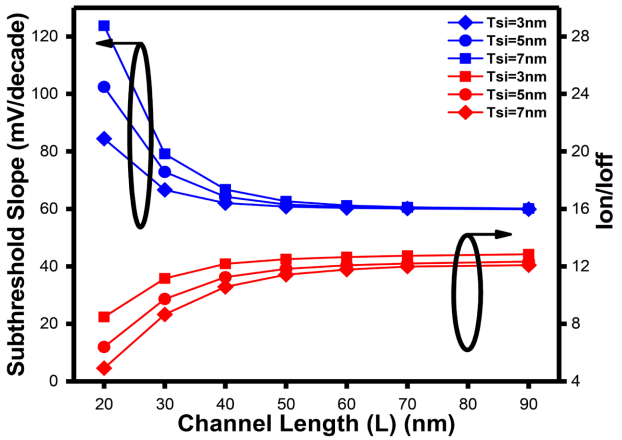

Figure 16. Variation of subthreshold slope and I_{on} - I_{off} ratio (in log scale) with channel length for different values of Si film thickness ($N_c = 10^{15}$ cm^{-3}, $N_s = 10^{18}$ cm^{-3}, $t_{ox} = 2$ nm, $\phi_G = 4.9$ eV).

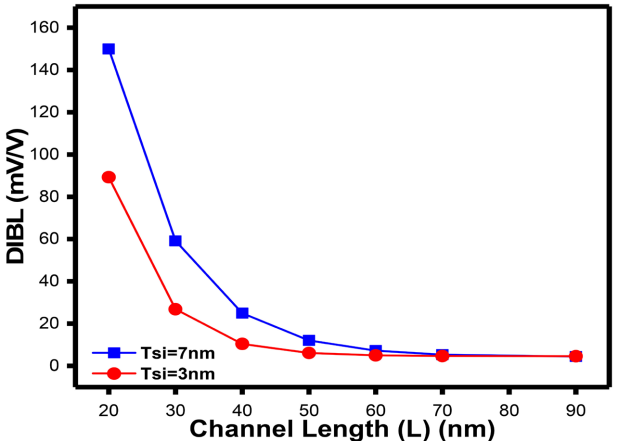

Figure 17. Variation of *DIBL* with channel length for different values of Si film thickness ($N_c = 10^{15}$ cm^{-3}, $N_s = 10^{18}$ cm^{-3}, $t_{si} = 5$ nm, $\phi_G = 4.9$ eV).

in devices with thicker channel. This is due to weak gate to channel coupling which allow drain to enhance the control over channel charges.

4. Conclusion

The effect of physical parameters variation on performance characteristics of the device such as V_t, *SS*, I_{ON}/I_{OFF} ratio, *DIBL*, etc. has been studied incorporating quantum confinement effects along with short channel effects. The V_t and I_{off} are found to increase and decrease respectively with the increasing channel length, increasing channel doping concentration, decreasing operating temperature, decreasing oxide thickness, decreasing Si film thickness whereas I_{on} and g_m can be seen decreasing with the increasing channel length, increasing temperature, increasing channel doping concentration and increasing gate oxide thickness. I_{on} and g_m increase and decrease respectively with the increase in Si film thickness. The I_{on}/I_{off} ratio and *SS* can be observed to enhance with the increasing channel

length, decreasing operating temperature, and increasing concentration of the channel region, decreasing gate oxide thickness and decreasing Si film thickness. The *DIBL* effect is more at higher operating temperature, lower channel doping concentration, higher gate oxide thickness and higher Si film thickness. It can be concluded that quantum effects and short channel effects significantly affect the performance characteristics of the device, and therefore, these must be incorporated for nano-scale circuit design. The TCAD analysis can also be used for device modeling and device matching. It can be used to illustrate exact device behavior and for proper device control. It can also be used for checking technological parameter fluctuations, reliability evaluation factors, etc. The results are demonstrated by extensive 2-D TCAD simulation and confirmed analytically at various technology nodes to validate the robustness of the model. Hence, the proffered physical models and the proposed device may be utilized in the progression of reliable and trustworthy TCAD simulation tools for nanodevices. The proposed Nano-DG-MOSFET is the confirmed upcoming device of ultra-low-power VLSI and high-frequency applications. This nano-device can definitely replace the conventional bulk MOSFETs in the future for low power circuits.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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