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Nullors, and Nullor Circuits; There Applications in Symbolic Circuit Analysis and Design

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Abstract

The objective in this presentation is to introduce some of the unique properties and applications of nullors in active circuit analysis and designs. The emphasis is to discuss the role nullors can play in symbolic representation of transfer functions. To show this we adopt the topological platform for the circuit analysis and use a recently developed Admittance Method (AM) to achieve the Sum of Tree Products (STP), replacing the determinant and cofactors of the Nodal Admittance Matrix (NAM) of the circuit. To construct a transfer function, we start with a given active circuit and convert all its controlled sources and I/O-ports to nullors. Now, with a solid nullor circuit (passive elements and nullors) we first eliminate the passive elements through AM operations. This produces the STPs. Second, the all-nullor circuit is then used to find the signs or the STPs. Finally, the transfer function (in symbolic, if chosen) is obtained from the ratio between the STPs.

Keywords

Admittance Method, Analog Circuits, Nullors, Nullor Circuits, Sum of Tree Products, Transfer Functions

1. Introduction

Although virtual nullors play a constructive role in the analysis and design of active circuits. They can basically replace controlled sources as well as I/O-ports in circuits and greatly simplify the circuit analysis and synthesis. Nullors are quite essential in behavioral modeling of active devices [1]-[7]. Just like any active circuit component a nullor can take orientation and get a magnitude, called coefficient multiplier. Their major use is in replacement of both active devices and I/O-ports. So, in doing that we substantially simplify an active circuit to contain only passive elements and nullors.

Due to their simplicity and being versatile, nullors are ideal for symbolic representation of circuit transfer functions [8]. In this presentation we are going to use nullors exactly for this purpose, and the platform adopted for it is going to be the topological platform using the tree enumeration method. We particularly put emphasis on the *Sum of Tree Products* (STP) here. Given a circuit N, any circuit transfer function of N can be expressed as a ratio of two rational symbolic expressions, the numerator, and the denominator. For N represented by its *Nodal Admittance Matrix* (NAM) this ratio is the ratio of the NAM determinant and a cofactor, or the ratio of two cofactors. However, in the topological platform there is no need to go after any cofactor. The ratio is the ratio of two STPs extracted from two circuits: 1) the main circuit, and 2) one augmented by a nullor.

Another major property of nullors in circuit analysis is that, with the help of the *Admittance Method* (AM) procedure [9] [10] the computation of the STP will be gradually stepwise, and there is no need to form the well-known 2-graph representation, typically used for active circuits. In addition, the use of 2-trees to find the transfer functions is also eliminated.

The paper is organized as follows. Section II is on nullors and nullor circuits. It briefly explains different types of nullors and their applications in replacing controlled sources and I/O-ports. It describes how an active circuit, as well as its augmented circuit, are totally turned into a nullor circuit. In Section III a newly developed AM methodology is provided and is being used in nullor circuits. Through the AM operations the determinant of the NAM of the circuit and its augmented version are generated, which are the same as the STPs of the circuits. Finally, the desired transfer function of the circuit is found in symbolic format, if needed. Section IV gives the conclusion.

2. Nullors and Nullor Circuit Modeling

Nullors are well established, and their properties are vastly investigated [1] [2] [3] [4]. Here we briefly introduce nullors and talk about their properties and applications that we need in this presentation.

2.1. Nullors

A *nullor* is a two port, with four terminals or three terminals component, shown in **Figure 1**. It consists of two elements, a nullator (left) and a norator (right). Nullors carry signs depending on the direction assigned to its elements, as shown in **Figure 1(a)**. In a three-terminal the nullor sign is positive if the two arrows merge at the common node or depart, **Figure 1(b)**. Otherwise, the sign is negative, **Figure 1(c)**. Presently, for four-terminal nullors we can only decide on the sign if the nullor becomes three-terminal in the circuit processing. Nullors always come with magnitude 1. When a controlled source with a magnitude p (e, f, g, or h) is replaced with a nullor the magnitude p is kept as a *coefficient* multiplier for a later use.

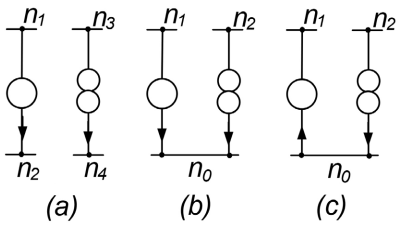


Figure 1. Nullors; (a) three nodes, STP = 0; (b) two nodes and positive, STP = 1; (c) two nodes and negative, STP = −1.

Nullors are of four types, *e*, *f*, *g*, and *h*. The distinction between them appears when the nullor is removed from the hosting circuit. As shown in Figure 2 (the two last columns), it works as follows:

1) Removing an *e* nullor (n_e) leaves the nullator nodes, n_1 and n_2, open circuited and the norator nodes, n_3 and n_4, short circuited.

2) Removing an *f* nullor (n_f) leaves the nullator nodes, n_1 and n_2, short circuited and the norator nodes, n_3 and n_4, open circuited.

3) Removing a *g* nullor (n_g) leaves the nullator and the norator nodes, n_1, n_2, n_3 and n_4, open circuited.

4) Removing an *h* nullor (n_h) leaves the nullator nodes, n_1 and n_2, short circuited and the norator nodes, n_3 and n_4, short circuited.

2.2. Nullor Modeling of Dependent Sources

Dependent sources of all kinds can be modeled by nullors. As an example, let us assume that the dependent source is of a VCCS (g) type with the transadmittance gm, as shown in Figure 2(c). The source value gv_1 depends on two parameters g and v_1. To keep the source value within the limits, we can grow g to infinity and at the same time reduce v_1 toward zero to keep gv_1 within the limit. Apparently, the outcome will be a nullor replacing the dependent source, with the nullor value g, as shown in Figure 2(c). For other types of dependent sources, namely, VCVS (e), CCCS (f), and CCVS (h), the procedure is the same, nullors replacing the dependent sources. A complete list of converting dependent sources to their equivalent nullors is shown in Figure 2.

2.3. Nullor Modeling of I/O-Ports

To model I/O-ports with nullors we need to replace them with controlled sources first, and then replace the controlled sources with nullors. We start with a simple case of a 2-port linear circuit N with current input and voltage output, as shown in Figure 3(a). We then write the I/O-ports transadmittance y_{21} of N as $y_{21} = I_1/V_2$, or $I_1 = y_{21} * V_2$. Now, assume that I_1 is removed and replaced with a VCCS with $g_m = y_{21}$, which is controlled by the output voltage V_2. Call this new circuit an *augmented circuit*, as shown in Figure 3(b). Therefore, if we initially apply a voltage V_2 to the output port of the augmented circuit a current is produced at the input port exactly equal to the initial current source I_1. This means a replacement of an I/O-ports by a controlled source g_m does the same job.

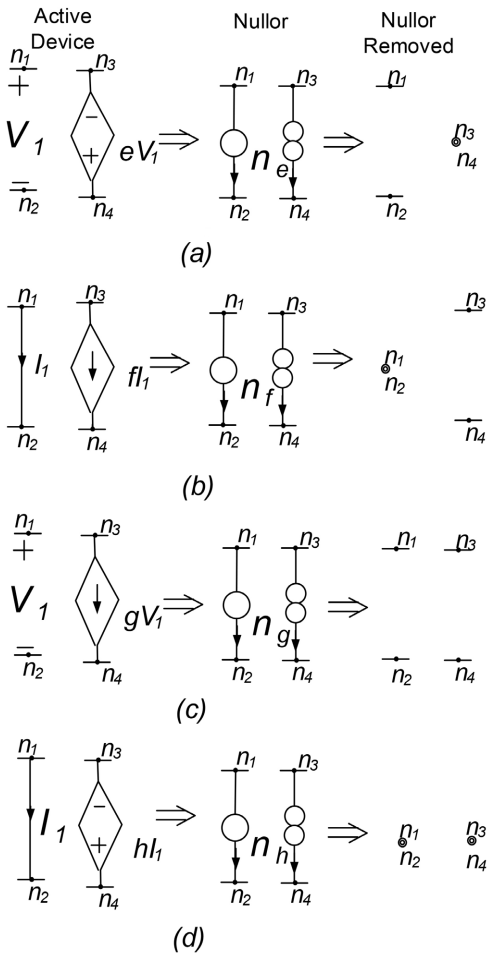


Figure 2. Different stages of four types of controlled sources: dependent sources, nullor equivalent, and when the active device is removed from the circuit, namely VCVS (e); CCCS (f); VCCS (g); CCVS (h).

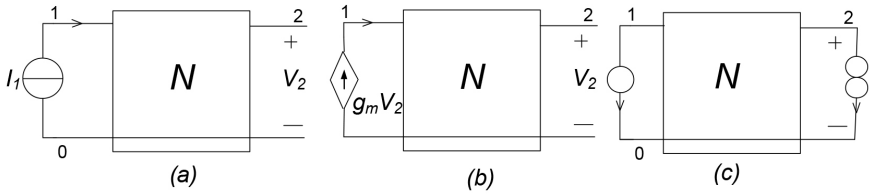


Figure 3. A 2-port circuit to calculate the trans-conductance y_{21}; (a) original 2-port; (b) port replacement with a VCCS; (c) final replacement with a nullor.

Note that replacing the I/O-ports with $g_m = y_{21}$ returns the circuit back to its original N. So, the determinant of the circuit NAM still becomes equal to T_o. But we have already found T_o. Instead, we need T_{21} to get the trans-admittance $y_{21} = T_o/T_{21}$. We can also write $T_{21} = T_o/y_{21} = T_o/g_m$. Hence, to compute T_{21} all we need to do is to assume $g_m = 1$ in the augmented circuit and then compute the NAM determinant of the circuit.

Up to here, we have been able to work on controlled sources replacing I/O-ports. Now, it remains to convert the controlled sources to nullors. In the case of an

augmented circuit, we replace the controlled source with an appropriate nullor with the source multiplier equal to 1. This is shown in Figure 3(c). However, we are still missing the type of the nullor replacing an I/O-ports. What we need to do is to specify the types of I/O port, and it so happens that, just like controlled sources, I/O-ports are also of four types:

1) Voltage input and voltage output, VIVO, or *e* type,

2) Current input and current output, CICO, or *f* type,

3) Current input and voltage output, CIVO, or *g* type,

4) Voltage input and current output, VICO, or *h* type.

Therefore, modeling of an I/O-ports is done by replacing it with the same type of nullor. Figure 4 displays four types of I/O-ports, and the different stages each type goes through to be replaced with the right type of the nullor model, and finally, when the I/O-ports are removed.

So far, we concluded that, to find the transadmittance $y_{21} = T_o / T_{21}$ of a given circuit N we need to take the following steps:

1) Generate an augmented circuit N_a by removing the I/O-ports and replacing it with the same kind of controlled source with the coefficient, e, f, g, or h, equal to 1.

2) Replace all controlled sources in both N and N_a with the right types of nullors and keep the controlled source coefficients.

3) Compute the STPs T_o and T_{21}, respectively, and find the transfer function $y_{21} = T_o / T_{21}$.

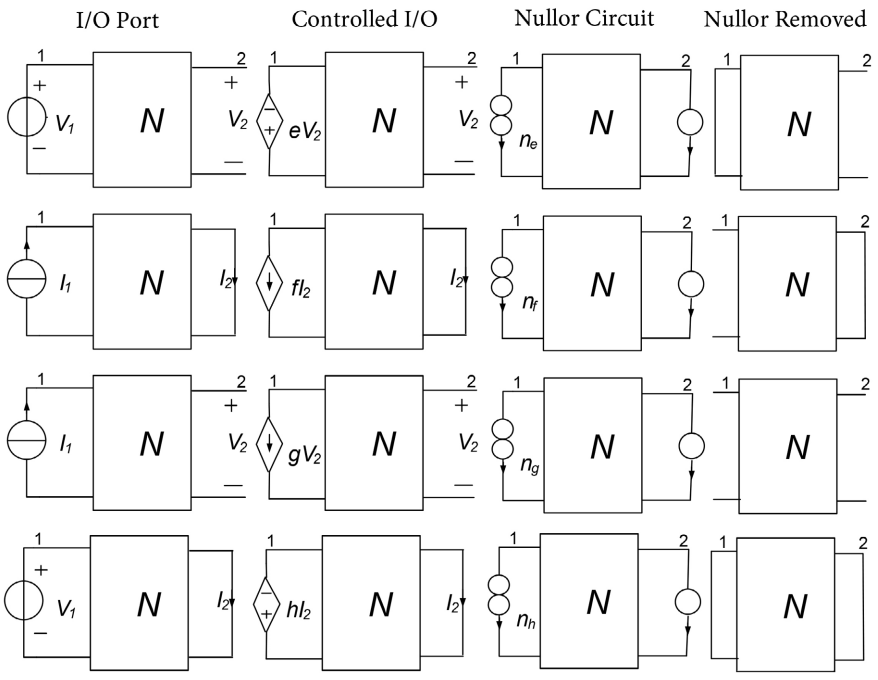


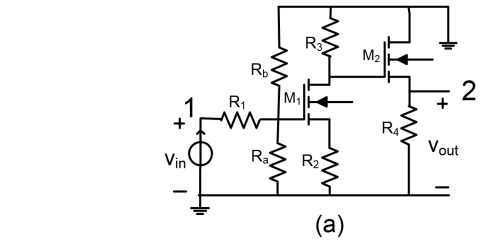
Figure 4. Different stages of four types of I/O-ports: input source applied, i) a controlled source replacement with e, f, g, or h coefficient equal to 1, ii) a nullor model, and iii) when the pair of I/O-ports is removed from the circuit. I/O types: VIVO (e), CICO (f), CIVO (g), VICO (h).

2.4. Nullor Circuit

As discussed before, given an active circuit with any types of controlled sources and I/O-ports, the final circuit becomes a *nullor circuit* when all active devices and I/O-ports are nullor modeled. Such a nullor circuit consists of only passive components and nullors. So, by nullor modeling we can turn the analysis of any active circuit to the analysis of its equivalent nullor circuit, which includes finding the circuit transfer functions. This is a significant achievement; for example, by nullor modeling of active circuits there is no need for two (I and V) graph representation of circuits, nor there is any requirement for 2-tree partitioning of circuit trees, typically used in the computation of cofactors to write the circuit transfer functions [11] [12] [13] [14]. Some examples may clarify the procedure.

Example 1—Consider a two stages nMOS amplifier N with the AC equivalent shown in **Figure 5(a)**. The mall signal circuit model is also shown in **Figure 5(b)** with $R_5 = R_a // R_b$. As seen, the amplifier contains two controlled sources of VCCS type with the trans-admittances g_1 and g_2, and an I/O-ports of VIVO type. To apply the STP operations on N we first construct the graph representations of the circuit in two forms. One for just the amplifier without the I/O-ports, shown in **Figure 5(c)**, and the other one with the I/O-ports included, shown in **Figure 5(d)**. This means we are going to have two STPs, one for the graph in **Figure 5(c)** and one for the graph in **Figure 5(d)**.

There are several points to notice here. First, as discussed in sub-section 3, the STP extracted from **Figure 5(c)**, denoted by T_o, represents the determinant of the NAM of N, whereas, that extracted from **Figure 5(d)**, denoted by T_{21}, which is the cofactor-*21* of the NAM of N. Secondly, the pair of I/O-ports, which is of VIVO type, is modeled by an e nullor with the coefficient value $e_3 = 1$. Also notice that, in contrast to g_1 and g_2 nullors, the removal of e_3 nullor makes the input port short circuited. Finally, the amplifier gain is found as $A_v = V_2 / V_1 = T_{21} / T_o$.



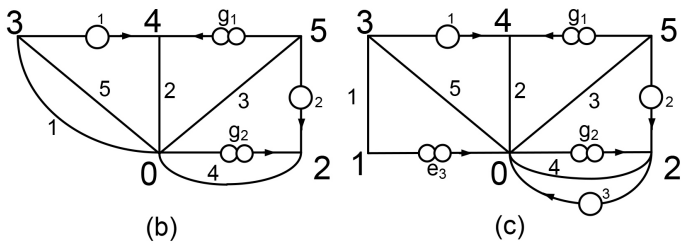


Figure 5. (a) The AC equivalent of a two stage MOS amplifier with the values assigned: $R_1 = 1$ *KOhm*, $R_2 = 1$ *KOhm*, $R_3 = 10$ *KOhms*, $R_4 = 2$ *KOhms*, and $R_5 = 50$ *KOhms*, $R_5 = R_a // R_b$. (b) The graph representation of the amplifier. (c) The graph representation of the amplifier when the I/O-ports is augmented with a nullor e type.

Now that we have turned an active circuit to a nullor circuit equivalence, we need to know how we can apply the STP to nullor graph, both to the main graph, depicted in **Figure 5(c)**, and the augmented graph for T_{21}, depicted in **Figure 5(d)**. This will provide us with the NAM determinant and the specific cofactor of the NAM. The procedure we are applying here is the AM technique [8] [10].

3. Admittance Method for Nullor Circuits

3.1. Sub-Circuit Generations from an Active Circuit

Here we compute the STP of an active (nullor) circuit through *AM* procedure, but before explaining the procedure we need to produce the sub-circuits from the main circuit. These sub-circuits are collectively constructing the STP of the main circuit. To start with, let us assume a circuit transfer function, such as the voltage gain of *Example 1*, $A_v = V_2/V_1 = T_{21}/T_o$. In case we desire to find the gain in symbolic format, with respect to the active devices and the I/O-ports, we need to write each STP, T_o and T_{21}, in symbolic format. For this example, we have two controlled sources g_1, g_2 and the I/O-ports specified by e_3 assigned. So, for example, take the graph in **Figure 5(d)**, and call it N_{21}, with the $STP = T_{21}$ expanded as

$$T_{21} = T^O + g_1T^1 + g_2T^2 + e_3T^3 + g_1g_2T^{12} + g_1e_3T^{13} + g_2e_3T^{23} + g_1g_2e_3T^{123} \quad (1)$$

Apparently, we can assume that $T^{ij\ldots m}$ is the STP of a sub-circuit $N^{ij\ldots m}$, for all i, j, …, and m, constructed from N_{21} when the active devices (and I/O-ports), i, j, …, and m, are present and replace with nullors, and the rest of the active devices (nullors) are removed from N_{21}. Therefore, for a circuit N_{21} with n active devices there are going to be $q = 2\text{^}n$ sub-circuits generated.

For the proof, let us assume that, for *Example 1*, all three nullors g_1, g_2, and e_3, are present in the circuit. We then realize that T_{21} approaches $g_1g_3e_3T^{123}$ as all g_1, g_2, and e_3 grow large. On the other hand, when this happens, we can simply ignore the rest of the controlled sources (nullors) and remove them from the circuit. The result, therefore, is N^{123}, a sub-circuit of N_{21}. Hence, referring to (1) we must then generate q numbers of sub-circuits from the main circuit N_{21}. What it means is the following.

The process of computing the final STP of N_{21} is going to be in two stages. In the first stage we get the q number of sub-circuits $N^{ij\ldots m}$ from the original circuit N_{21}. Notice that $N^{ij\ldots m}$ is a nullor circuit, *i.e.*, all active devices, including the I/O-ports, are replaced with nullors and the coefficient multipliers are kept separately. In the second stage each subcircuit $N^{ij\ldots m}$ is analyzed and its STP, $T^{ij\ldots m}$, is calculated. The final STP for N_{21} is subsequently given by (1). So, basically, our task now is to find the STPs for the sub-circuits $N^{ij\ldots m}$.

Now, we are ready to apply the AM operations on the sub-circuit $N^{ij\ldots m}$. The circuit is a nullor circuit consisting of two types of components, passive and nullors. We first apply the AM operations on the passive components of $N^{ij\ldots m}$ and then complete the process by doing the nullors operations, and then combining the two.

Remark 1—It is important to note that the nullors associated with all the active components, i, j, …, and m, in $N^{ij\cdots m}$ must be present in all the trees in the STP. This is evident from (1). For example, according to (1), both nullors related to the active devices g_1 and e_3 must be present in every tree in computing T^{13}.

3.2. AM Procedure for Passive Portion of a Circuit

In this AM procedure we try to eliminate the passive components of the circuit one by one until the last element is reached. This last element, naturally, has an admittance representing a transfer function of the passive portion of the circuit. More details and an extended description of the procedure is given in [8] [13]. In brief, the AM procedure uses two fundamental operations: 1) *parallel* and *series*, and 2) *partition*. To apply the procedure smoothly, we first need to write admittances in ratios. For instance, the admittance of a 2-terminal component c_i is given by $y_i = n_i/d_i = y_i/1$.

Parallel and Series—Two parallel passive components c_i and c_j with admittances $y_i = n_i/d_i$ and $y_j = n_j/d_j$ produce a component c_p with the admittance given as

$$y_p = \left(n_i d_j + n_j d_i\right) \Big/ d_i d_j \tag{2}$$

Two series passive components c_i and c_j produce a component c_s with the admittance given as

$$y_s = n_i n_j \Big/ \left(n_i d_j + n_j d_i\right) \tag{3}$$

An exhausted sequence of *parallel/series* (*P/S*) operations results in a *P/S free* circuit.

Partition—Consider circuit N, and let c_i be a component of N. In partitioning N with respect to c_i two circuits are generated, one with c_i removed, denoted by $N\{c_i; 0\}$, and one with c_i short-circuited, denoted by $N\{0; c_i\}$. In general, a partitioned circuit $N\{A; B\}$ is obtained from N by removing elements A and short circuiting elements B from N. $T\{A; B\}$ refers to the determinant (STP) of the NAM of $N\{A; B\}$. With T being the STP of N we get

$$T = n_i T\{0 : c_i\} + d_i T\{c_i : 0\} \tag{4}$$

All we have done up to this point has been the operations involving passive-passive components. Our next move is going to operate on the passive-active (nullor) components.

Parallel/Series of passive and nullor elements—This kind of P/S operation is slightly different from those passive-passive cases.

Theorem 1—If a passive element c_i is parallel with a nullator or a norator, c_i is removed and d_i, in $y_i = n_i/d_i$, is preserved as a coefficient-multiplier. Likewise, if a passive element c_i is in series with a nullor element, c_i is short-circuited and n_i, in $y_i = n_i/d_i$, is preserved as a coefficient-multiplier.

Proof—Suppose the determinant of the original circuit is T. Then in the case of a parallel we get $T\{0; c_i\} = 0$, because of a loop in a nullor element. So, from

(4) we get $T = d_i T\{c_i; 0\}$. Similarly, in the case of a series we get $T\{c_i; 0\} = 0$, because of a node with a single nullor element. Hence, $T = n_i T\{0; c_i\}$.

4. Finding the Determinant of a Nullor Circuit through STP

The determinant of the NAM of a circuit N, which uses the STP procedure, can be given as

$$T = p * T_p * T_a \tag{5}$$

where, each of the three components, p, T_p, and T_a, can be separately calculated.

1) *The coefficient-multiplier p*—The coefficient-multiplier p is found through.

$$p = \prod_i b_i \prod_j a_j \tag{6}$$

where, b_i, for all i, denote the dependent sources (e_i, f_i, g_i, and h_i) in N, and a_j, for all j, denote all the individual coefficient-multipliers (n_j, and d_j) resulted in the passive AM operations.

2) T_p is the STP of the passive components obtained through the AM operations.

3) T_a is the STP of the *all-nullor* circuit of N; where, an all-nullor circuit is constructed from the nullor circuit N when all the passive components are eliminated in the AM operations.

The first two components p and T_p have already been computed. So, it remains to find T_a.

4.1. The STP of an All-Nullor Circuit

Consider an all-nullor circuit N_a, which consists of an equal number of nullators and norators, forming a network. We can state the following theorems.

Theorem 2—The STP of an all-nullor circuit T_a is either 0, 1, or −1.

Proof—This is because the magnitude of a nullor is 1, and so, evidently, we get $|T_a| = 1$ or 0.

Theorem 3—The magnitude $|T_a| = 1$ if and only if each nullator and norator networks form a single tree with no loop. Otherwise, $T_a = 0$.

The proof follows from *Remark 1*.

Corollary 1—An all-nullor circuit N_a has a non-zero *STP* only if 1) the total number of its nodes is equal to the total number of nullors plus one, and 2) any node is incident to at least one nullator and one norator.

Remark 2—We now need to find the sign of an all-nullor circuit, T_a. To do this, we first separate the nullator and norator networks from each other in N_a and begin eliminating nullors (corresponding nullators and norators) one by one starting from the 3-terminals[1] nullors. In case the arrows in the paring nullator and norator are toward or away from the common node the sign is positive, otherwise it is negative. Next, short-circuit the nullor elements in the network with the common node removed, and then move to the next nullor and do

[1]In practice, when the passive circuit is removed in a nullor circuit most 4-terminal nullors become 3-terminals. Also removing 3-terminal nullors usually change some 4-terminals to 3-terminals.

the same until all nullors are gone. The final sign obtained is the sign of T_a.

For proof, notice that each time we short circuit a nullor, depending on the direction, either we change the sign of T_a or not. Therefore, the sign of T_a (and $T^{ij\ldots m}$) depends on the number of changes we have made in removing all nullors.

Example 2—In this example we are going to take *Example 1* and expand the circuit graphs to form the sub-circuits (graphs) and then compute the corresponding STPs for each sub-circuit. By combining these STPs we find the circuit determinant and the cofactor in symbolic format, and finally the symbolic gain $A_v = V_2/V_1$.

Figure 6 shows the graphs for all eight sub-circuits, where each graph contains a certain number of active devices (nullors) as explained before. To compute the STPs for the sub-circuits we need to assign values to the passive components. A listing of the sub-circuits, their active components, and the values of the STPs for the sub-circuits are given in Table 1. Finally, based on the data given in Table 1 we produce the symbolic representation of T, T_{21}, and the gain transfer function A_v, as given in (7), (8), and (10).

$$T = 51 + 51g_1 + 102g_2 + 102g_1g_2 \tag{7}$$

$$T_{21} = -1000g_1g_2 \tag{8}$$

$$A_v = \frac{V_2}{V_2} = T_{21}/T \tag{9}$$

$$A_v = -1000g_1g_2/(51 + 51g_1 + 102g_2 + 102g_1g_2) \tag{10}$$

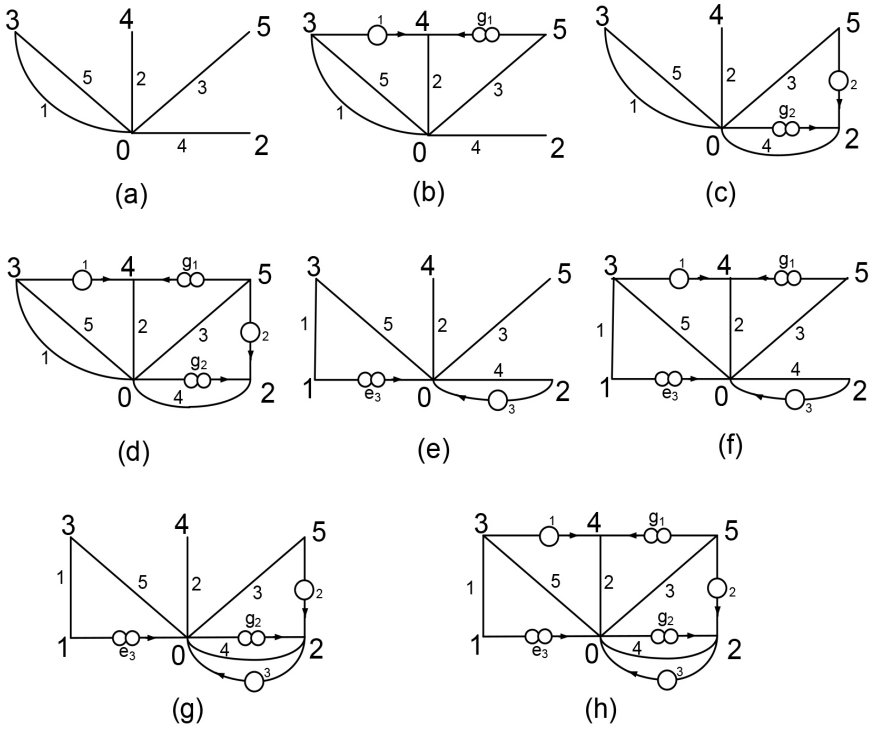


Figure 6. Graphs of the eight sub-circuits corresponding to the amplifier in Example 1.

Table 1. Sub-circuits and their STP values.

Sub-graph	Active Devices included	STP Value
Figure 6(a)	-	51
Figure 6(b)	g_1	51
Figure 6(c)	g_2	102
Figure 6(d)	g_1g_2	102
Figure 6(e)	e_3	0
Figure 6(f)	g_1e_3	0
Figure 6(g)	g_2e_3	0
Figure 6(h)	$g_1g_2e_3$	−1000

For $g_1 = 5\ mA/V$ and $g_2 = 10\ mA/V$ we get the gain $A_v = -7.78\ V/V$.

Notice that the active device (nullor) e_3 is not present in either T or T_{21}. This is because the role of e_3 is just to distinguish between and separate the two sets of sub-circuits; those that construct T and the rest which form T_{21}. This is a major achievement, because there is no need to create 2-tree graphs, as normally required [11].

4.2. The STP Expanded for a Sub-Circuit

To show how AM procedure works for the construction of a STP, we take one of the sub-circuits of this example, say the graph of Figure 6(h), and find its STP, T^{123}, through AM operations.

Take the graph of Figure 6(h) and continue with the following operations.

1) Resistance R_1 is in series with nullor element e_3, and resistance R_4 is in parallel with nullor element e_3. R_1 is short-circuited and R_4 is removed. The coefficient p gets R_4 and becomes $p = 2$.

2) Resistance R_5 is now in parallel with nullor element e_3. R_5 is removed. The coefficient p gets R_5 and becomes $p = 2 * 50 = 100$.

3) There are two resistors left in the circuit, R_2 and R_3. Notice that the graph has five nodes and three nullors. According to corollary 1 it must lose one node. This means of the two one resistance must be short-circuited and one removed. The STP becomes 0 if R_3 is short-circuited, because we get a nullator loop. So, the only choice is R_2 short-circuited and R_3 removed. With the resistance value $R_3 = 10$ the process terminates with the coefficient value $p = 2 * 50 * 10 = 1000$.

4) For the sign we refer to Figure 7(a), which is the graph of Figure 6(h) when all the passive components are processed. Figure 7(b) is the same as Figure 7(a) when the nullator and norator networks are separated. We short-circuit pairs of the nullor elements according to *Remark 2*. The sequence is shown in Figures 7(b)-(d), which finally results in $sign = -1$. Therefore, we get the $STP = -1000$.

This concludes our Example 2.

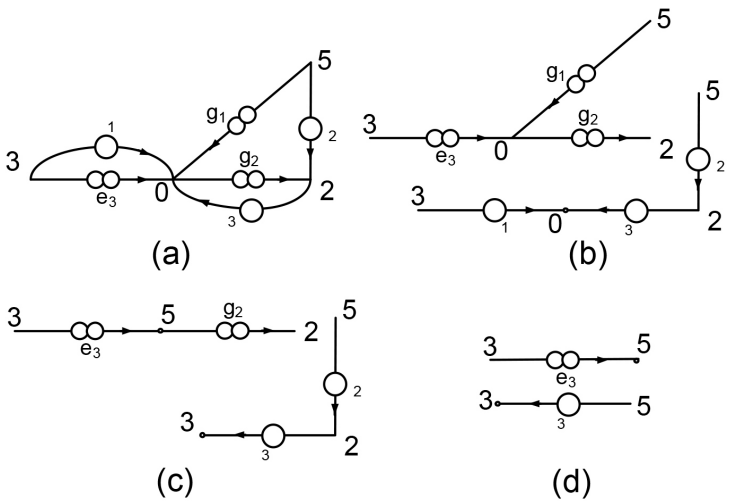


Figure 7. (a) From **Figure 6(h)** when all the passive components are processed. (b) The same as (a) when the nullator and norator networks are separated. (c) and (d) When the corresponding pairs of nullators an norators are short-circuited according to *Remark 2*.

5. Conclusions

A new technique is described for the construction of transfer functions of active circuits in symbolic form. The technique is based on, first converting an active circuit into a nullor circuit and then using the tree enumeration procedure to find the STP of the circuit in symbolic form. The nullor is also used to obtain an augmented nullor circuit from the original circuit by adding a nullor to the I/O-ports. While the STP provides the determinant of the NAM of the main circuit the STP from the augmented circuit gets the cofactor needed to form the circuit transfer function. The technique also skips the normal tree enumeration procedures and instead uses the, newly developed, AM operations to construct the STPs.

The technique can be explained in several steps. First, both the circuit and its augmented circuit produce sub-circuits. Each sub-circuit consists of all passive elements plus several (including zero and all) active components, and the rest of the components are removed. The sub-circuits so created represent all sub-circuits possible. Second, each sub-circuit goes through the AM operations for the passive elements to find the magnitude of STPs. For the sign, the gradual removal of the active components (nullors) is performed. Finally, the desired transfer function appears in the ratio of the two STPs, preferably in symbolic format.

Conflicts of Interest

The author declares no conflicts of interest regarding the publication of this paper.

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