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Design of Low Power Level Shifter Circuit with Sleep Transistor Using MultiSupply Voltage Scheme

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Abstract

New low-power Level Shifter (LS) circuit is designed by using sleep transistor with Multi Threshold CMOS (MTCMOS) technique for robust logic voltage shifting from sub-threshold to above-threshold domain. MultiSupply Voltage Design (MSVD) technique is mainly used for energy and speed in modern system-on-chip. In MSVD, level shifters are required to allow different voltage supply to shift from the lower power supply voltage to the higher power supply voltage. This new low-power level shifter circuit is also used for fast response and low leakage power consumption. This low leakage power consumption can be achieved through insertion of sleep transistor and proper transistors sizing. The proposed design efficiently converts 100 mv input signal into 1 v output signal and achieves the power of 2.56 nW by using 90 nm technology.

Keywords

Level shifter (LS), MultiSupply Voltage Design (MSVD), Subthreshold operation, Ultralow Power

1. Introduction

MultiSupply Voltage Domain (MSVD) technique is an effective method to reduce both dynamic and leakage powers in modern system-on-chips. It consists of partitioning the design into separate voltage domains. Based on timing requirements, each module can be operated at a proper power supply voltage level [1]-[3]. Time critical domains run at higher power supply voltage (VDDH) to maximize performance, while noncritical domains run at lower power supply voltage (VDDL), to reduce static and dynamic power without impacting on the overall circuit performance. In MSVD system, level shifters (LSs) are required on the boundaries between the circuit

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subsections operating at different power supply voltages to convert signals from the VDDL to the VDDH voltage level.

Multithreshold CMOS technique is mainly used to optimize the delay and power of the circuit. It consists of two levels of threshold voltage such as low threshold voltage and high threshold voltage. Low threshold voltage is used to increase the speed and reduce the clock period. High threshold voltage is used to reduce the static power leakage. Sleep transistors are series to the pull-up and/or the pull-down of the logic gates, and turn them off when the circuit is idle, thereby decreasing the leakage component due to sub-threshold currents. When an nMOS sleep transistor is used on the pull-down path, a SLEEP signal controls its active/standby mode (*i.e*., SLEEP during standby and SLEEP during active mode) [4]-[6]. In the standby mode, the sleep transistor is off, thus disconnecting its insertion point, called virtual ground, from the physical ground. In active mode, the gated circuit operates normally, but it incurs delay degradation due to the series resistance of the sleep transistor.

The common LS is the differential cascade voltage switch (DCVS) circuit that is typically used for changing signals between the two different above-threshold voltage domains. Drawback of the DCVS-LS is the conflict between the pull-up and pull-down networks which becomes severe when input signals are in the subthreshold range, thus making the conventional sizing methods impractical to get a properly functioning circuit. To address this problem, in order to improve the performance several conventional DCVS circuits have been proposed. The four-stage cascaded DCVS circuit was designed for robust level up-conversion from the subthreshold region. But it introduced large power penalties to the intermediate power supplies and also limited speed performance [7]-[9].

A two-stage LS was proposed, the first stage exploits a DCVS circuit with an always-on diode-connected nMOS transistor on the top; whereas, the second one is a conventional DCVS stage that achieves rail to rail swing. It avoids intermediate power lines, but again it is not enough to reach high-speed performances. The LS was designed by two pMOS current limiters to reduce the half-latch pull-up strength within the conventional DCVS structure. This circuit is able to convert subthreshold input signals and it requires reasonably sized pull-down transistors. Also this LS is relatively slow and energy-hungry. A circuit based on current mirrors has been designed for better speed performance, but the current mirror output floats when the input voltage signal is high [10]-[12]. This causes a detrimental effect on subthreshold leakage of the output buffer.

Recently, LS was designed, it is suitable for fast and wide range voltage conversion from the subthreshold domain to above-threshold domain, but it has high power consumption. A new low-power LS is designed to improve the speed and reduce the power by using multithreshold CMOS technique and sleep transistor.

This paper is organized as follows. Firstly, the related work is briefly explained in Section 2; next, the proposed methodology is described in Section 3. Then, the results and discussion are described in Section 4. Finally, the content is concluded in Section 5.

2. Related Work

The Level shifter in the system is mainly used for fast and wide range voltage conversion in Multi Supply Voltage Domain [7]. Multi Threshold CMOS (MTCMOS) technique is used in the architecture of level shifter circuit. These circuit which gives robust voltage shifting from the deep sub-threshold to the above-threshold domain, while demonstrating fast response and low energy consumption [13]-[15].

The LS circuit is shown in **Figure 1** is designed by using the multi-threshold CMOS design technique along with novel topological strategies. The circuit consists of an input inverter, a main voltage conversion stage and an output inverting buffer. The input inverter (MP_1/MN_1) is designed using low threshold voltage (lvt) transistors. To have higher strength of the pull-down network, also MN2 and MN3 are lvt transistors. Then, two lvt pMOS devices (MP_2 and MP_3) are added to both the branches of the circuit.

These devices limit the cross-bar current that is the current flowing in the pull-up network and opposing to the discharge of NH (or NL) node at the beginning of their high to low transition. To further facilitate the high to low transition at the nodes NH and NL, MP_4 and MP_5 are high threshold voltage (hvt) transistors. This choice also reduces leakage current flowing through the pull-up networks when MP_4 or MP_5 are turned off. However, using hvt, pMOS transistors has the counter effect of slowing the low to high transition of the nodes NH and NL. Therefore, to reduce the switching delay, a pull-up network able to self-adapt its strength to the actually occurring desirable transition [16]-[18].

This behavior was obtained by introducing the parallel connected hvt devices MP_6-MP_{10} and MP_7-MP_{11},

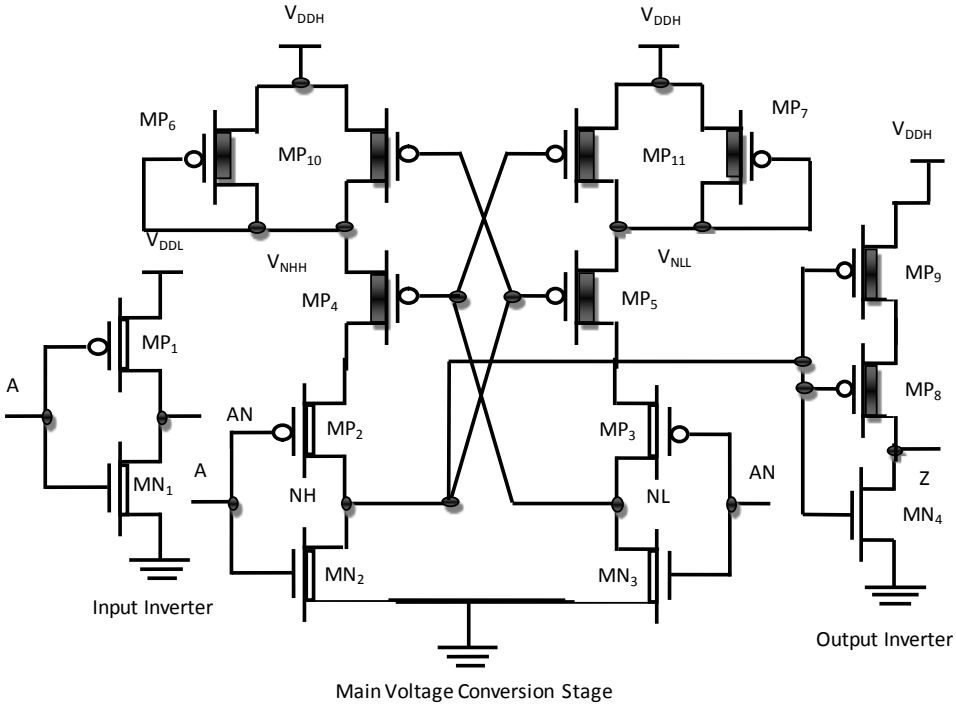

Figure 1. Existing level shifter.

with MP_6 and MP_7 being diode connected transistors. The two variable virtual power supplies on the two branches of the circuits are V_{NHH} and V_{NLL}. Therefore, the strength of pull-up networks is adapted to the next output switching transition. Assuming that the output Z is initially low (high), the pull-up network of the left branch is weakened (strengthened) and that of the right branch is strengthened (weakened), thus speeding-up a low-to-high (high-to-low) output transition.

The introduction of hvt MP_{10} and MP_{11} devices controlled by NH and NL voltages. To assure a rail-to-rail conversion, an output inverting buffer is connected to the node NH. This inverter uses a standard threshold voltage (svt) nMOS (MN_4) device and two stacked hvt pMOS transistors (MP_8 and MP_9). The used pull-up configuration allows static current when NH is high to be significantly reduced. In such a condition, the MP_9 device has the effect of maintaining the source node of MP_8 below V_{DDH}. As the source terminal of MP_8 results to be at lower voltage than its bulk node, the MP_8 threshold voltage increases. The source-gate voltage of MP_8 is also reduced, thus further reducing static current in the above referred condition. These LS is suitable for robust logic voltage shifting from near/sub-threshold to above threshold domain has been presented. This circuit exploits proper design strategies to increase the operating speed while maintaining low energy consumption and large voltage conversion range [19] [20].

Table 1 represents the sizing of transistor in existing system. Proper transistor sizing can be achieved by changing the aspect ratio of the transistors, *i.e*. width and length of the transistors. MN_1 to MN_2 denotes the nMOS transistors and MP_1 to MP_{11} denotes the pMOS transistors.

3. Proposed Work

The proposed low power level shifter is mainly used for power reduction and wide range voltage conversion in MultiSupply Voltage Domain. Novel level shifter architecture is combined with Multi Threshold CMOS (MTCMOS) technique can be achieved by proper sizing of transistors and sleep transistor. This circuit provides robust voltage shifting from the deep sub-threshold to the above-threshold domain with low power consumption.

3.1. Sleep Transistor

Sleep transistor is an effective approach to minimize standby leakage current. Sleep transistor is added to the cir-

Table 1. Transistor sizing of existing system.

Device	W/L (μm)	Device	W/L (μm)	Device	W/L (μm)
MN_1	0.3/0.1	MP_2	1.2/0.2	MP_7	0.18/0.2
MN_2	1.2/0.2	MP_3	0.18/0.2	MP_8	1.2/0.2
MN_3	0.5/0.2	MP_4	0.3/0.2	MP_9	1.2/0.2
MN_4	1.1/0.2	MP_5	0.18/0.2	MP_{10}	0.12/0.2
MP_1	0.45/0.1	MP_6	0.3/0.2	MP_{11}	0.12/0.2

cuit serially. Sleep transistor is used as a switch to shut off power supplies to parts of a design in standby mode. A sleep transistor is referred to either a pMOS or nMOS high threshold transistor that connects the permanent power supply to circuit power supply which is commonly called "virtual power supply". The sleep transistor is controlled by a power management unit to switch ON and OFF power supply to the circuit. The nMOS sleep transistor is used to switch VSS supply and it is called footer switch. The header switch is pMOS has lower drive current than footer switch is NMOS of a same size. Due to this, a header switch implementation usually consumes more area than a footer switch implementation. Because of this problem, footer switch is used in the proposed level shifter. When the state of footer switch is "1" then it is in turn on condition to block the leakage current to the ground.

3.2. Circuit Diagram

The proposed LS circuit is shown in **Figure 2** is designed by using the multi-threshold CMOS design technique along with sleep mode strategies. The circuit diagram consists of an input inverter, a main voltage conversion stage, sleep transistor and an output inverting buffer.

Table 2 represents that the sizing of transistors in proposed level shifter by changing the width and length of the transistors. The circuit has been sized to achieve the minimum energy delay product in the following operating condition: V_{DDH} = 1 V, V_{DDL} = 0.1 V, 25 fF load capacitance on the output node, T = 25˚C, TT process corner.

3.3. Input Inverter

The input inverter MP_1 and MN_1 are designed for low threshold voltages (lvt) transistors. It provides fast differential low voltage input signal to main voltage conversion stage.

3.4. Main Voltage Conversion Stage

The MN_2 and MN_3 are lvt transistors used to achieve high strength in pull down network. Then two lvt pMOS devices MP_2 and MP_3 are added to both the branches of the circuit. MP_4 and MP_5 are high threshold voltage (hvt) transistors. It is used to reduce leakage current from the pull up transistors when MP_4 and MP_5 are turned off. And also this hvt pMOS transistor are used to reduce the switching delay and a pull-up network are able to self adapt its strength for occurring actual transition.

This behavior was obtained by using a parallel connected hvt devices MP_6-MP_{10} and MP_7-MP_{11}, with MP_6 and MP_7 being diode connected transistors. It is used to adapt the strength of the pull up networks into next output switching transition. The hvt is applied to MP_{10} and MP_{11} devices and it is controlled by High Node (NH) and Low Node (NL) voltages. The use of diode-connected pMOS transistors MP_6 and MP_7 limits the output range of the main conversion stage. MN_5 (nMOS) transistor act as a sleep transistor which is used to block the leakage current from the main voltage conversion stage to the ground.

3.5. Output Inverting Buffer

To secure a rail-to-rail conversion, an output inverting buffer is connected to the node NH. The output inverter consists of standard threshold voltage (svt) in MN_4 (nMOS) and to stacked hvt MP_8 and MP_9 (pMOS).

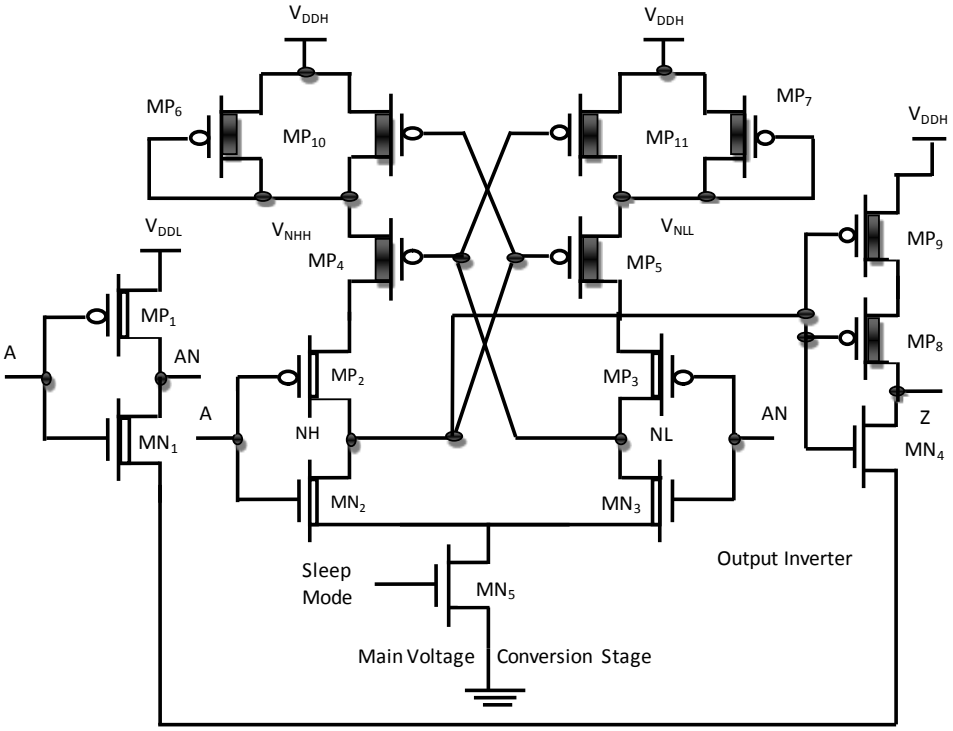

Figure 2. Proposed level shifter.

Table 2. Transistor sizing of proposed system.

Device	W/L (μm)	Device	W/L (μm)	Device	W/L (μm)
MN_1	0.3/0.1	MP_2	0.3/0.2	MP_7	1.2/0.2
MN_2	1.5/0.2	MP_3	1.2/0.2	MP_8	1.2/0.2
MN_3	1.1/0.2	MP_4	1.2/0.2	MP_9	1.2/0.2
MN_4	1.1/0.2	MP_5	1.2/0.2	MP_{10}	1.2/0.2
MP_1	1.2/0.2	MP_6	1.2/0.2	MP_{11}	1.2/0.2

3.6. Operation

As the input signal switches, the transistor MN_2 is turned on and the node NH starts to be discharged. Due to this, the source to gate voltage of MP_4 is reduced and increases its threshold voltage. Owing to this, MP_4 is weakened, thus increasing the discharge of the node NH. In the meantime, the stronger pull-up of the right branch charges the node NL and causing MP_4 to be turned off. This allows the discharging of NH to be further accelerated. As NH approaches the ground voltage, the positive feedback becomes to explode, causing MP_5 to be fully activated. Therefore, NL is fully charged at the low voltage level. Once transitions in the nodes NH and NL are completed, the virtual power supplies $V_{NHH} = V_{DDH}$ and $V_{NLL} = V_{DDH} - V_{dsat}$, MP_7 are established to provide fast switching in the subsequent input transition.

The used pull-up configuration allows static current when NH is high to be significantly reduced. In such a condition, the MP_9 device has maintaining the source node of MP_8 below V_{DDH}. As the source terminal of MP_8 results to be at lower voltage than its bulk node, the MP_8 threshold voltage increases. The source-gate voltage of MP_8 is also reduced, thus further reducing static current in the above condition. As 3 V external power supply is supplied to MN_5 (sleep transistor) and it is always in turn on condition to block the leakage power from the main voltage conversion stage.

4. Implementation

4.1. Simulation Results

Figure 3 represents that simulation diagram of existing level shifter. In this diagram, appropriate nMOS and pMOS transistors are selected and then fix the width and length of the transistor and connected by using wire. High voltage nMOS transistor is used as a sleep transistor. Voltage pins are used to calculate the voltage conversion and wattmeter is used to calculate the power.

Figure 4 shows the waveform of voltage conversion and power analysis of proposed level shifter. PM1 denotes the power of 2.56 nW. VF1 denotes voltage converted to 1 V. VF2 denotes the voltage at NH. VF3 denotes the voltage at NL. VG1 denotes the voltage in sleep transistor.

4.2. Performance Analysis

Table 3 compares the existing system and proposed system. In both the systems, voltage conversion can be achieved from 100 mV to 1 V but low power can be achieved in proposed system than the existing system.

The **Figure 5** shows that comparison chart of power analysis for existing and proposed system. The proposed system consumes 2.56 nW power. The existing system consumes 5.66 nW power. When compared to existing system, the proposed system consumes low power.

5. Conclusions

The proposed level shifter is suitable for robust logic voltage shifting from near/subthreshold to above-threshold domain. The proposed circuit exploits proper design strategies to maintain very low energy consumption and large voltage conversion range. Sleep transistor technique is used which is able to further reduce the total leakage power from the circuit to the ground by breaking the physical connection to the ground. And also low

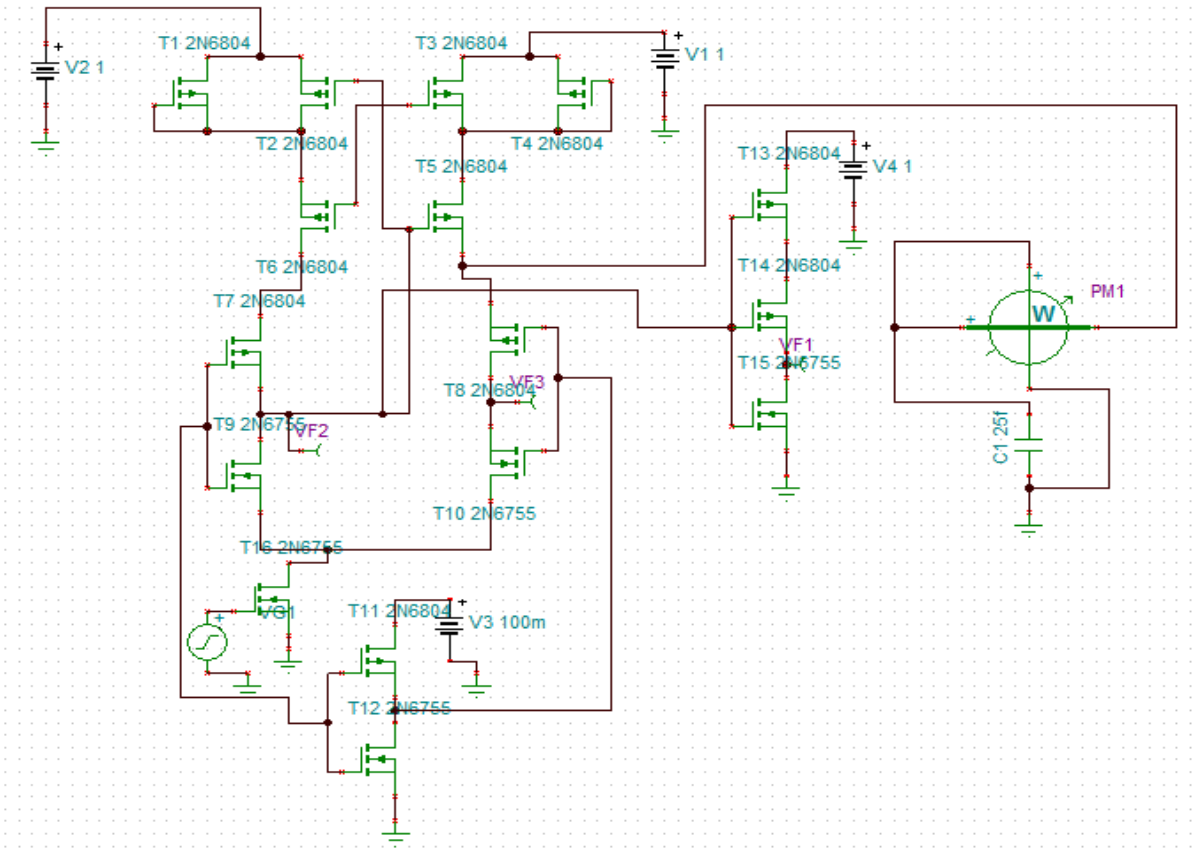

Figure 3. Simulation diagram of proposed level shifter.

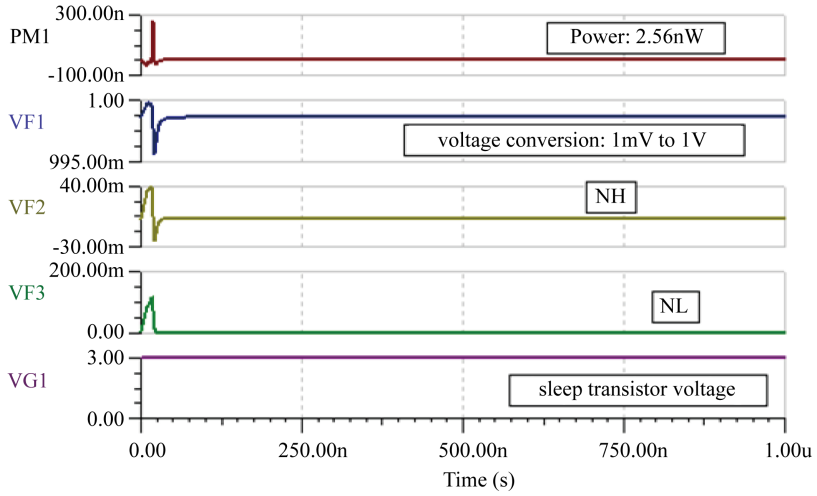

Figure 4. Output waveform of proposed level shifter.

Table 3. Comparison table of power analysis.

Sl. No.	Methodology	V_{DDH} (V)	V_{DDL} (V)	Power (nW)
1	Existing Method	1	0.1	5.66
2	Proposed Method	1	0.1	2.56

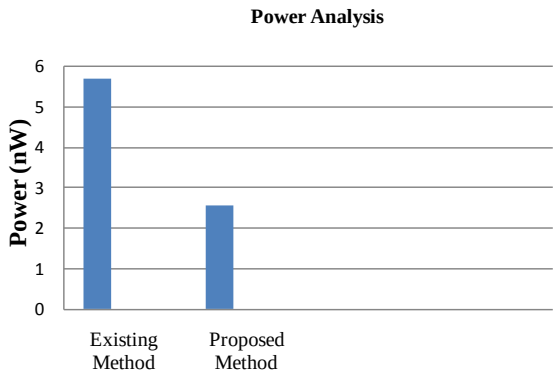

Figure 5. Comparison chart of power analysis.

power consumption can be achieved by proper sizing of transistor. The proposed design reliably converts 100 mV input voltage into 1 V output voltage. The simulation results demonstrate that the new LS shows power of 2.56 nW compared to existing system power of 5.66 nW.

The proposed level shifter is used in many applications. In future, the proposed level shifter is implemented in flip-flop circuit for further reducing the power and achieves the voltage conversion from subthreshold to above-threshold.

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