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Design and Implementation of Efficient Reversible Arithmetic and Logic Unit

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Abstract

In computing architecture, ALU plays a major role. Many promising applications are possible with ATMEGA microcontroller. ALU is a part of these microcontrollers. The performance of these microcontrollers can be improved by applying Reversible Logic and Vedic Mathematics. In this paper, an efficient reversible Arithmetic and Logic Unit with reversible Vedic Multiplier is proposed and the simulation results show its effectiveness in reducing quantum cost, number of gates, and the total number of logical calculations.

Keywords

Reversible Logic Gates, Reversible Logic Circuits, Reversible Multiplier Circuits, Vedic Multiplier, ALU

1. Introduction

Moore's law states that number of transistors in a chip doubles every two years but chip size decreases. This cannot be reduced greatly which will lead to more power consumption. This paves the path to new technologies "Reversible Logic" and "Quantum Dot Cellular Automata" (QCA). As stated by Launder irreversible logic (unequal number of inputs and outputs) consumes more power [1]. To overcome this problem Bennett sets equal number of inputs and outputs, which will dissipate less power as input bits are preserved at the output [2]. This is called Reversible Logic. In this paper, Reversible Logic is chosen for its low power and Vedic concept is used for its faster arithmetic calculations. A quantum computer uses principle of superposition and entanglement for qubit (quantum bit-basic unit of information in quantum computers) computation. Quantum computers are faster than classical computer and will find its application in air craft tester, driverless cars and develop more effective

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drugs, etc. Reversible Logic plays an important role in converting classical computation to quantum computation. The basic properties of Reversible Logic are discussed in [3].

Reversible gates are classified as 2 × 2 gates, 3 × 3 gates and 4 × 4 gates. The classification of Reversible Logic gates is given in **Figure 1**.

The basic reversible gates are Feynman gate, Taffoli gate and Peres gate. The basic reversible gates are shown in **Figure 2** [4].

The 4 × 4 reversible gates such as TSG gate and HNG gate are discussed in [3] given below.

TSG Gate

Thapliyal proposed a 4 × 4 reversible gate called TSG gate [5]. The TSG gate is shown in **Figure 3** and quantum circuit diagram for TSG gate is given in **Figure 4**. The input and output functions are given in Equations (1) and (2) respectively.

$$\mathrm{Iv} = (\mathrm{A}, \mathrm{B}, \mathrm{C}, \mathrm{D}) \tag{1}$$

$$\mathrm{Ov} = \left(\mathrm{P} = \mathrm{A}, \mathrm{Q} = \mathrm{A'C'} \oplus \mathrm{B'}, \mathrm{R} = (\mathrm{A'C'} \oplus \mathrm{B'}) \oplus \mathrm{D}, \mathrm{S} = (\mathrm{A'C'} \oplus \mathrm{B'}) \cdot \mathrm{D} \oplus \mathrm{AB} \oplus \mathrm{C}\right) \tag{2}$$

Full adder, Wallace tree multiplier 4:2 compressor are constructed using TSG gate.

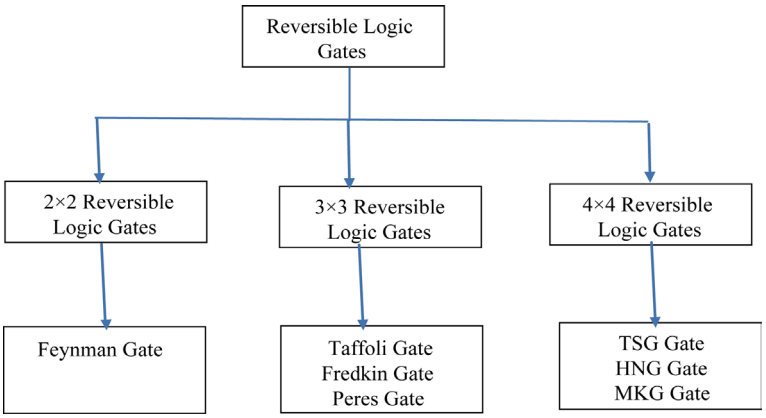

Figure 1. Classification of reversible logic gates.

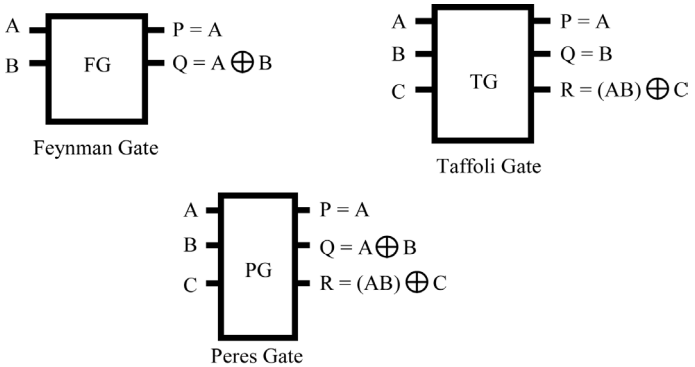

Figure 2. Basic reversible gates.

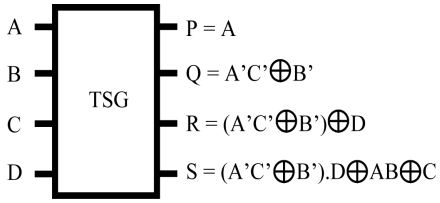

Figure 3. TSG gate.

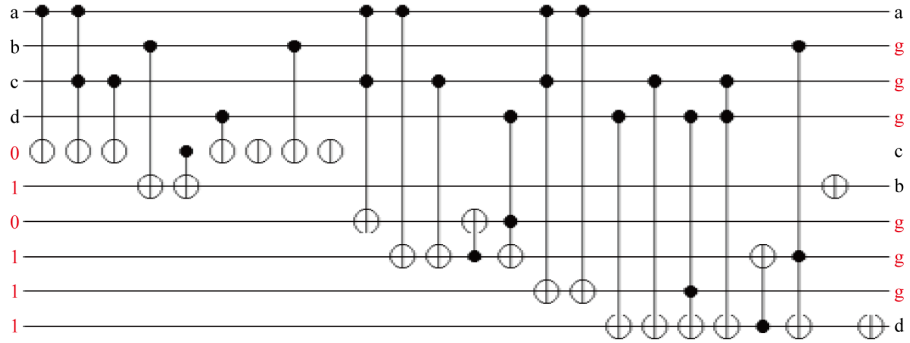

Figure 4. Quantum circuit diagram for TSG gate.

Single TSG gate will act as full adder. Parallel adder or ripple carry adder is implemented using the same. Ripple carry adder is needed in multiplier. When C input is 0, D input is given with carry input, and then TSG gate functions as full adder. The TSG gate as full adder is shown in **Figure 5**.

HNG Gate

It is a 4 × 4 reversible gate [6]. The HNG gate is shown in **Figure 6** and quantum circuit diagram for HNG gate is given in **Figure 7**. The input and output functions are given in Equations (3) and (4) respectively.

$$\mathrm{Iv} = \left(\mathrm{A}, \mathrm{B}, \mathrm{C}, \mathrm{D}\right) \tag{3}$$

$$\mathrm{Ov} = \left(\mathrm{P} = \mathrm{A}, \mathrm{Q} = \mathrm{B}, \mathrm{R} = \mathrm{A} \oplus \mathrm{B} \oplus \mathrm{C}, \mathrm{S} = \left(\mathrm{A} \oplus \mathrm{B}\right)\mathrm{C} \oplus \mathrm{AB} \oplus \mathrm{D}\right) \tag{4}$$

HNG gate is used to construct full adder and multiplier. When D input is 0, A, B and C inputs are given, and then HNG gate functions as full adder. The HNG gate as full adder is shown in **Figure 8**.

The basic benchmark parameters of the reversible logic circuits are quantum cost, garbage output, and total number of logical calculations.

The number of reversible logic gates either 1 × 1, 2 × 2, 3 × 3 or 4 × 4 needed to design a reversible system is called number of gates. Quantum cost (QC) refers to the number of elementary gates 1 × 1 or 2 × 2 reversible logic gates needed to design the reversible logic circuit.

The unused output in a reversible circuit is called garbage output.

Total logic calculation is the number of XOR, AND, and NOT logic functions used in the reversible circuit. α indicates number of XOR logic in the circuit, β indicates number of AND logic in the circuit and d indicates number of NOT logic in the circuit

Research in reversible logic is getting important today. Thapliyal and Srinivasan proposed a new reversible TSG gate [5] and discussed about reversible carry look-ahead adder and other adder architecture which formed a part of ALU. The quantum cost of TSG gate is quiet high when compared to HNG gate. Haghparast proposes two new 4 × 4 bit reversible multiplier designs with less hardware complexity, less garbage bits, less quantum cost, and less constant inputs [6] and the architecture uses Peres gate for partial product generation. But the total logical calculation is more due to extra logics in Peres gate. Research is going on in deriving more applications out of it. Research is moving towards deriving a new application from reversible gates. Ancient Indians followed some sutras or formulae for mathematical computation. These basic mathematical calculations form the base for modern VLSI architecture. Thapliyal discussed about performance of Vedic Multipliers on FPGA [7] and discussed the irreversible architecture based on delay. These architectures when implemented in VLSI will reduce power consumption. Ehsan Pour Ali Akbar *et al*. proposed reversible signed Wallace tree multiplier in [8]. Synthesis of reversible circuits is discussed in [9]-[14] and testing of reversible circuits is discussed in [15].

1.1. Vedic Multiplication

"Vedic Mathematics" was derived from the ancient word "Vedas". Vedic mathematics was rediscovered in early twentieth century. It works on the sixteen mathematical formulae called as "sutras" [16]. Mostly the speed of the DSP processors depends mainly on the speed of its multipliers which in turn depends on number of internal logics used [17]. Multipliers are used to realize many important functions such as Fast Fourier transforms and con-

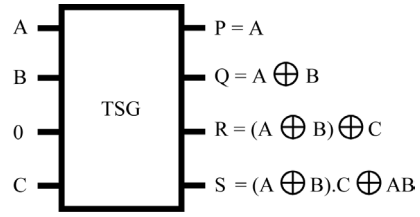

Figure 5. TSG gate as full adder.

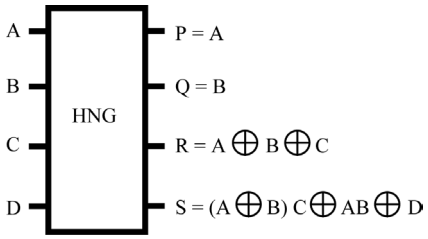

Figure 6. HNG gate.

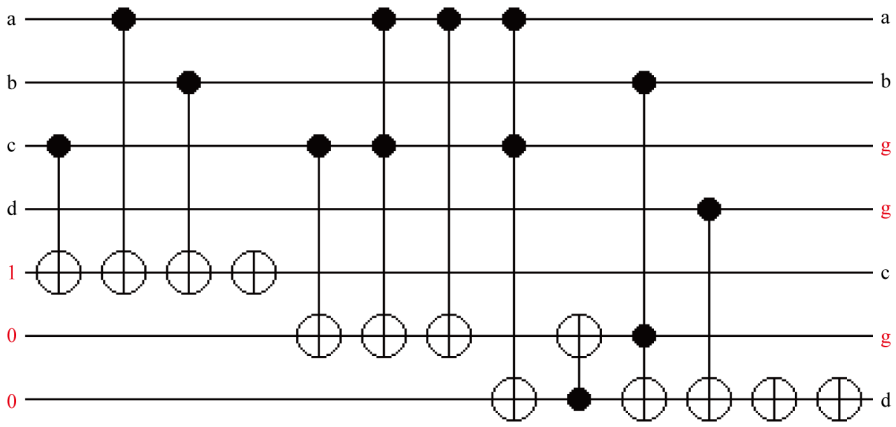

Figure 7. Quantum circuit diagram for HNG gate.

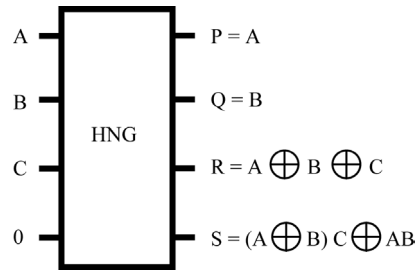

Figure 8. HNG gate as full adder.

volutions. VLSI architectures built using these sutras will improve the performance of the system. Vedic mathematics makes complex conventional calculations to be simpler and easier ones [18]. It does the computations very fast using human mind. Vedic Mathematics is a set of arithmetic rules that allows more efficient and speedy calculations. “Urdhva Tiryagbhyam” and “Nikhilam Navatashcaramam Dashatah” are the two important sutras involved in multiplication. Conventionally these Sutras are used to multiply decimal numbers. In this paper these sutras were applied to binary number system which makes it compatible for digital hardware. The partial products are generated in parallel but there will be some delay due to propagation of carry. It requires less hardware to implement.

1.2. Urdhva Tiryagbhyam Sutra

The Vedic Multiplier is designed using Urdhva Tiryagbhyam Sutra. This sutra has been traditionally used for the multiplication of two numbers. Urdhva Tiryagbhyam Sutra means "Vertically and Crosswise" [19]. The Least significant bits and most significant bits are multiplied vertically. LSB and MSB bits are multiplied crosswise and added as well. The line diagram for Urdhva Tiryagbhyam Sutra (step sequence from step 1 to step 7) is discussed in [3] and shown in **Figure 9**.

Tiwari *et al*. discussed about various Vedic Multipliers [20]. Rong Lin proposed reconfigurable and self-repairable multipliers and discussed about recursive architecture decomposition of partial product matrices [21]. Deodhe *et al*. presented a design of 8 bit Vedic Multiplier using CMOS logic [22]. Kumar *et al*. demonstrated 8 bit Vedic Multiplier using barrel shifter [23]. Haghparast's parity preserving reversible Vedic Multiplier has advantage of concurrent testing but its quantum cost is high [24]. Saravanan *et al*. discussed about reversible Vedic Multiplier design using nikhilam sutra [25].

2. Proposed Reversible ALU

ALU forms the major part of any processor. In this paper a reversible ALU is designed. All components of ALU are reversible in nature (equal inputs and outputs). Furthermore Vedic concept is adopted to enhance the speed of the processor by reducing critical path delay. The reversible ALU consists of 8 bit Multiplier, Logical unit and Binary to gray code converter. The sub modules are discussed below.

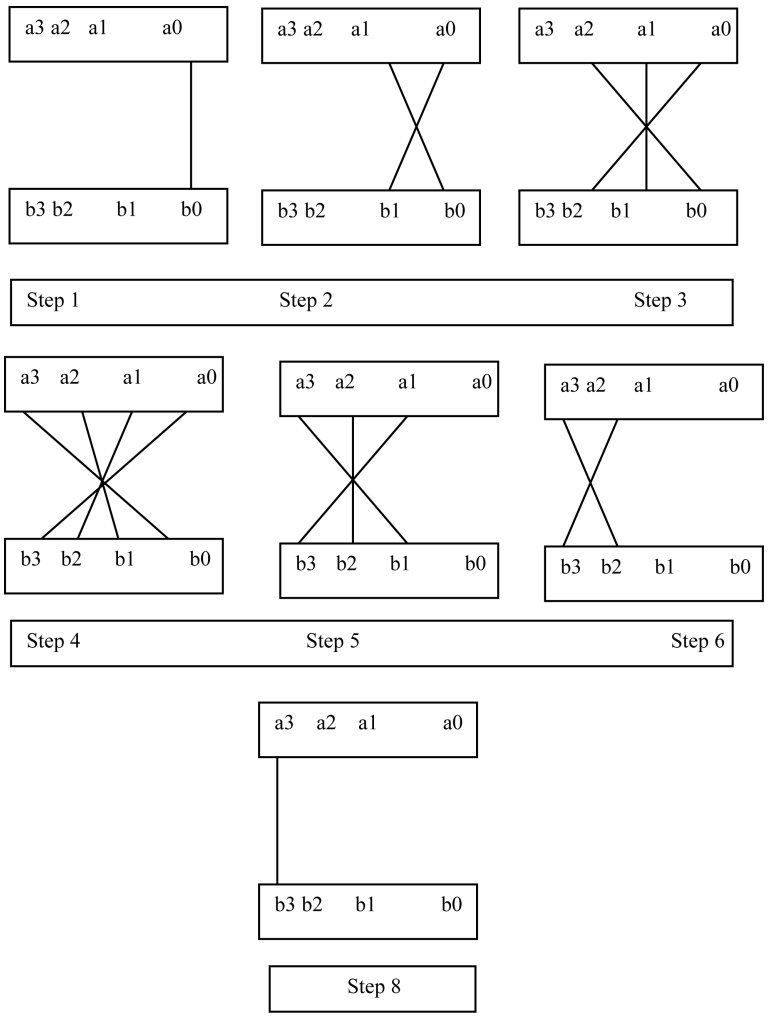

Figure 9. Line diagram for Urdhva Tiryagbhyam Sutra (step sequence from step1 to step7).

2.1. Vedic Multiplier

The 8 × 8 Vedic multiplier can be built from 2 × 2 Vedic multiplier. 8 × 8 Vedic multiplier requires 16 × 2 × 2 Vedic multiplier. 2 × 2 Vedic multiplier requires 4 multiplications and 2 half additions. To implement 8 × 8 Vedic multiplier it requires 64 multiplications and 32 half additions and 16 full additions. In contrast conventional array multiplier requires 64 multiplications and 50 full adders. So hardware complexity can be reduced using Vedic multipliers.

Consider two numbers with equal MSB and they are placed at equal distance from median value is taken. For this case if the input is taken in BCD form eight 2 × 2 Vedic multipliers and 8 bit adders are required. It requires 32 multiplications, 16 half additions and 8 full additions are required. Thus the multiplier can be implemented with less hardware architecture.

Reversible 8 × 8 Vedic Multiplier Architecture

The multiplier architecture is shown in **Figure 10**. In the proposed multiplier first LSB bits of multiplicand and multiplier are passed on to 4 × 4 Vedic multiplier. MSB bits of multiplicand and multiplier are multiplied and the result is once again added with MSB bits of multiplicand to get MSB of results. The algorithm works only for multiplicand and multiplier deviating from central value by equidistant.

Multipliers uses TSG gate based reversible Vedic multiplier or HNG gate based reversible Vedic multiplier. The adder block uses 8 HNG gates. The third input of HNG gate is Carry input. The last output of HNG gate is carry output. The fourth input of HNG gate is “0” input. The carry output is propagated to next stage carry input [3].

2.2. Logical Unit

It is an 8 bit logical unit. It consists of 8 peres gates. Peres gates generates AND logic and EXOR logic. The quantum cost of Peres gate is 4. There is only one garbage output. The Reversible logic unit architecture is shown in **Figure 11**. The inputs are A_7 - A_0 and B_7 - B_0. The input C_7 - C_0 is constant input which is 0. The $QQ1_7$ - $QQ1_0$ represents logical EXOR operation. The $RR1_7$ - $RR1_0$ represents logical AND operation.

2.3. Binary to Gray Code Converter Unit

It is an 8 bit binary to gray code converter unit. It consists of 8 Feynman gates. Feynman gates generate EXOR

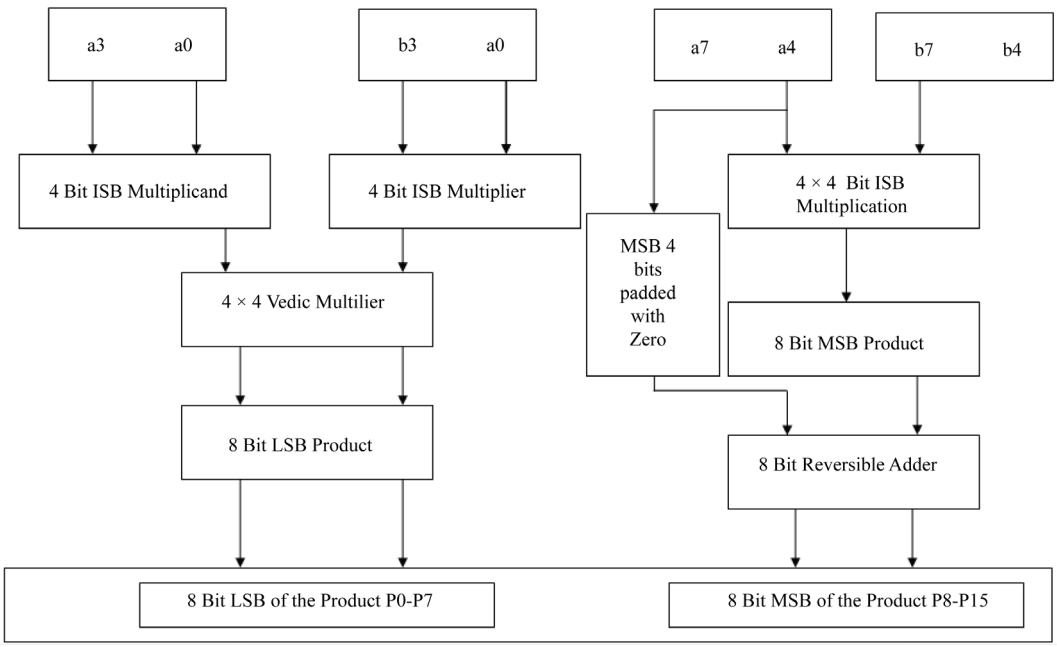

Figure 10. Multiplier architecture.

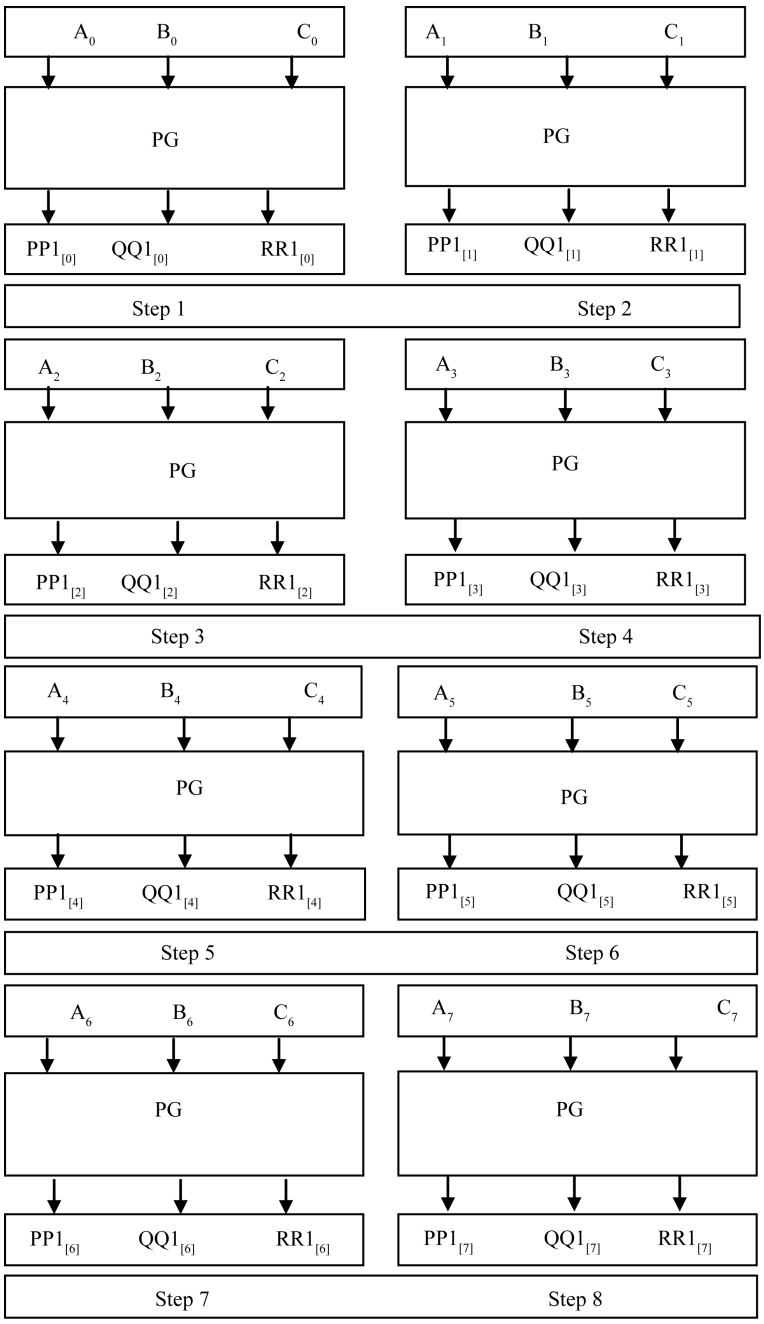

Figure 11. Reversible logic unit architecture.

logic. The quantum cost of Feynman gate is 1. There is only one garbage output. The Reversible Binary to Gray Code Converter Architecture is shown in **Figure 12**. The inputs to Feynman gate are A_7 - A_0. In this current bit is operated with previous bit. The $Q1_7$ - $Q1_0$ represents binary to gray code converted value.

2.4. Proposed Reversible ALU Architecture

The ALU consists of Arithmetic unit and logic unit. The Reversible ALU architecture is shown in **Figure 13**. The Reversible ALU consists of 8 bit reversible Vedic multiplier unit, reversible logical unit and reversible 8 bit binary to gray code converter. The logical unit consists of Peres gate which generates AND logic and EXOR logic. The EXOR logic is used to perform equality checking between two data.

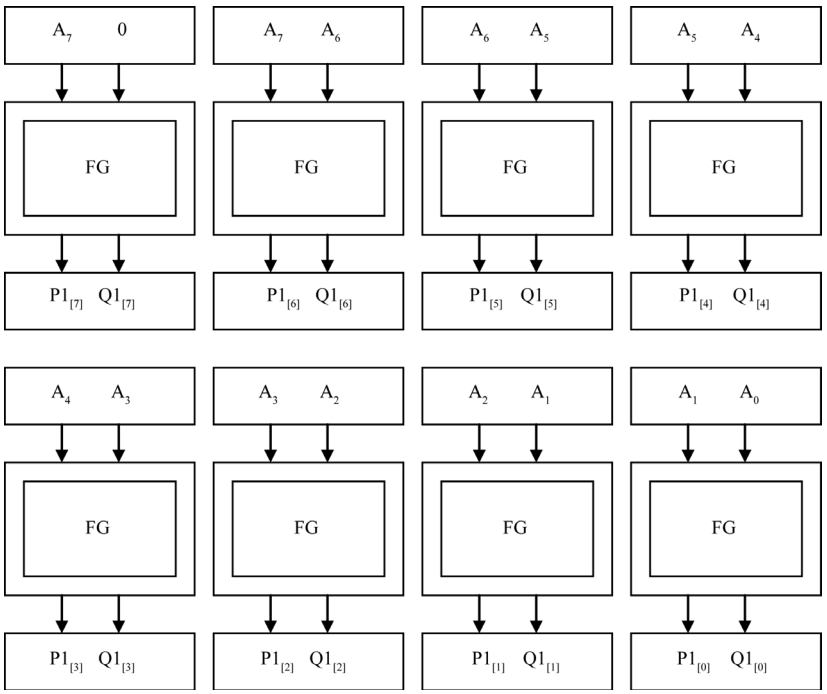

Figure 12. Reversible binary to gray code converter architecture.

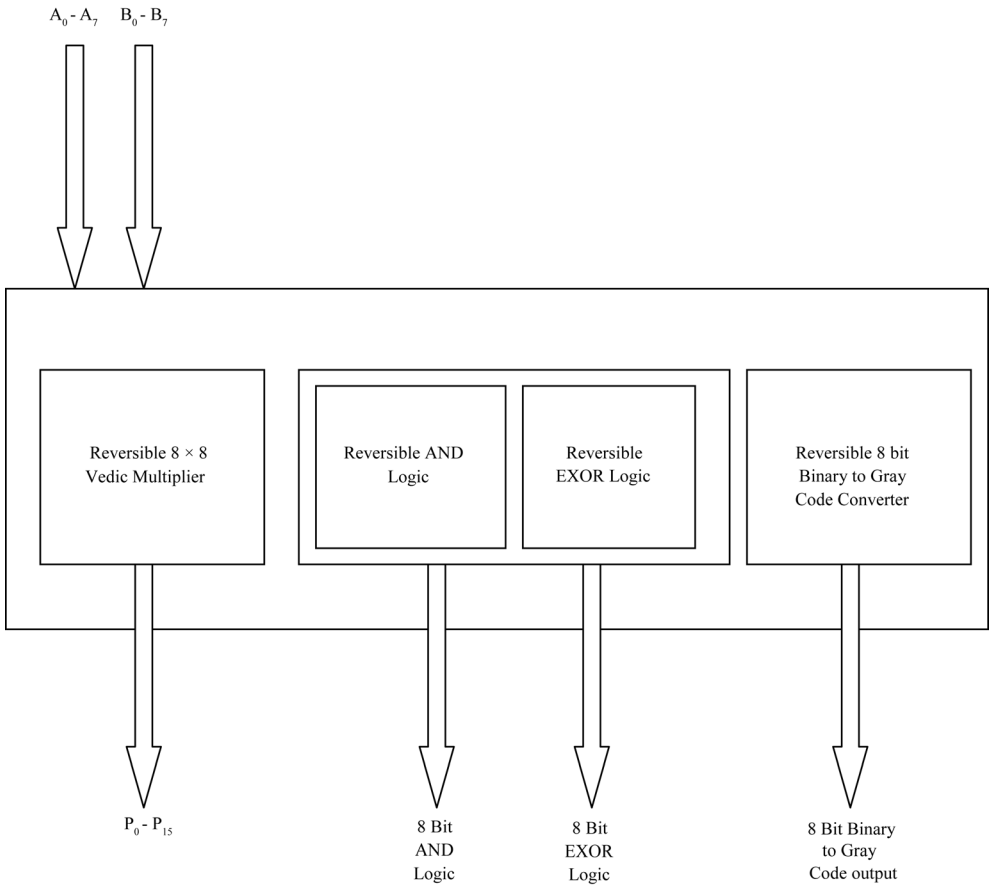

Figure 13. Reversible ALU architecture.

The binary to gray code converter uses 8 Feynman gate to generate gray code. Gray codes are also called as reflected binary codes. Since random data are generated, it may be used to generate parity bits. These parity bits are important in error correction systems. So these codes are used in error correction systems, digital TV transmission, etc., these codes are used in genetic algorithms. These gray codes are used in forward error correction systems. Data is transmitted over the channel. The data gets affected by noise. For a receiver in order to retrieve original data, it has to go for retransmission of data. This will consume more bandwidth. To reduce band width original data has to be recovered at the receiver end. This is called forward error correction. Here Reversible 8 × 8 multiplier is designed using TSG gates and HNG gates based on Vedic concept. 8 bit logical unit is designed using Peres gate where AND logic and EXOR logic are obtained. Peres gates are chosen because quantum cost is 4 which is less and number of logical functions are more. 8 bit binary to gray code converter uses Feynman gate. It gets single 8 bit input and produces corresponding output. Feynman gate is used because Quantum cost is 1.

3. Results and Discussion

The functional simulation of proposed multiplier architecture is simulated in Xilinx 9.2. The simulation Results for Reversible ALU is shown in **Figure 14**.

The applications of this ALU are multiplication, Binary to gray code conversion, Modulo 2 operation and Equality checking. In **Figure 14** a1 corresponds to MSB of multiplicand and c1 corresponds to LSB of multiplicand. b1 corresponds to MSB of multiplier and d1 corresponds to LSB of multiplier. h1 corresponds to MSB of final product 06. f1 corresponds to LSB of final product 18 in hexadecimal value equivalent decimal value is 24. $qq1_0$ - $qq1_7$ corresponds to 8 bit logical EXOR operation between A_0 - A_7 and B_0 - B_7 In the simulation results LSB and MSB bits are interchanged. $rr1_0$ - $rr1_7$ corresponds to 8 bit logical AND operation between A_0 - A_7 and B_0 - B_7. In the simulation results LSB and MSB bits are interchanged. $q1_0$ - $q1_7$ corresponds to 8 bit binary to gray code value.

The system has arithmetic unit, Logical unit and binary to gray code converter. The number of functions is more.

The Comparison of Reversible Vedic multipliers is shown in **Table 1**. The performance of different configurations of reversible 8 × 8 Vedic multipliers are analyzed and presented in **Table 1**.

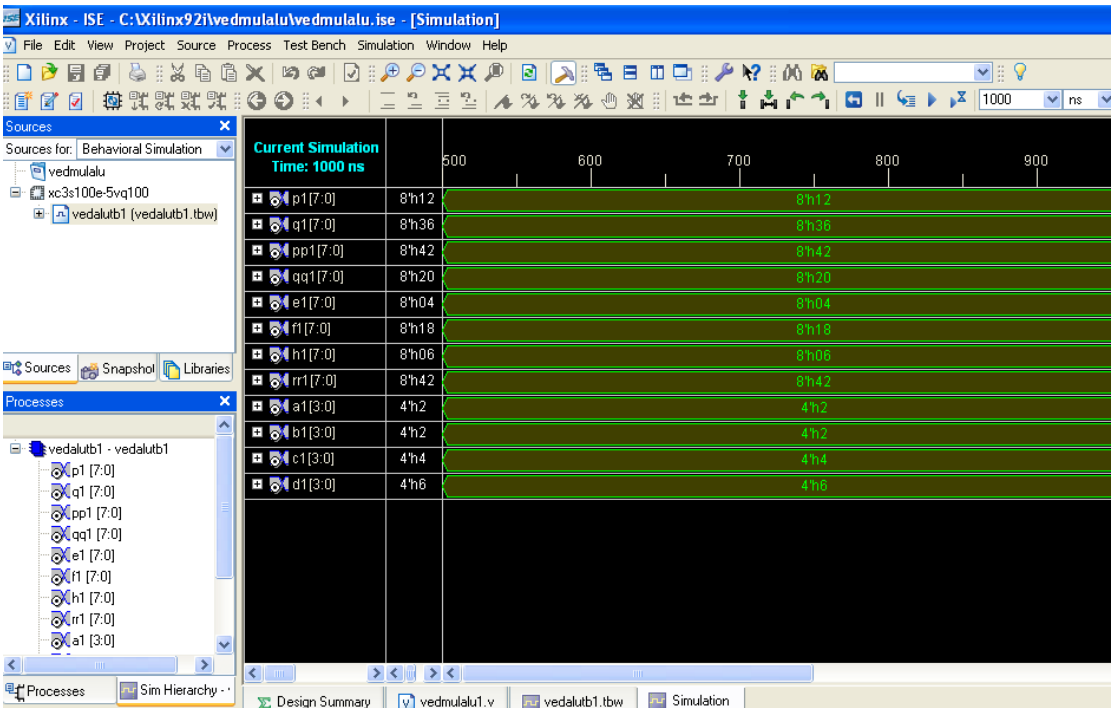

Figure 14. Simulation results for reversible ALU.

Table 1. Comparison of reversible vedic multipliers [3].

Summation Network	Multiplier Type	Partial Product Generation	Number of Gates	Quantum Cost	Number of Garbage Output	Total Logic Calculation	Number of Constant Input Lines
TSG gate	8 × 8 Vedic Multiplier	Taffoli Gate	60	488	116	184a + 156b + 216d	60
TSG gate	8 × 8 Vedic Multiplier	Peres Gate	60	456	116	196a + 156b + 216d	60
TSG gate [26]*	8 × 8 Vedic Multiplier	Fredkin Gate	60	488	116	*	60
HNGGate	8 × 8 Vedic Multiplier	Taffoli Gate	60	320	116	160a + 60b	60
HNGGate	8 × 8 Vedic Multiplier	Peres Gate	60	288	116	192a + 60b	60

*Not given in the literature.

The quantum cost for reversible 8 × 8 Vedic multiplier is calculated by the sum of quantum cost of two 4 × 4 reversible Vedic multiplier block and reversible adder block which can be stated mathematically as:

QC (Reversible 8 × 8 Vedic multiplier) = 2*(QC of Reversible 4x4 Vedic multiplier) + (QC of adder block).

Among the reversible 8 × 8 Vedic multiplier configurations HNG gate with peres gate offers low quantum cost. The number of garbage outputs is constant for all the cases. Among all combinations of multipliers, HNG gate with Taffoli gate partial product generation network offers low total logical calculations.

The number of constant input lines is same as that of number of gates required. From the table, reversible Vedic 8 × 8 multiplier designed using HNG gate shows effectiveness in terms of quantum cost, total logic calculations.

From the above table, it is found that in modern processors HNG gate based reversible Vedic multiplier architectures may be deployed to achieve high speed.

The Comparison of Conventional multipliers and reversible logic based multipliers is shown in **Table 2**. Since number of logic gates needed to implement adder module is less area will obviously be less in reversible logic.

The Comparison of various 8 × 8 Multipliers based on cell use and delay given by Thapliyal in [7] is shown in **Figure 15**. All multipliers are simulated in Xilinx platform using Virtex E XCV 300e device package, package BG 432 and speed grade-8.

The multiplier achieves a significant improvement in performance than other multipliers. The proposed multiplier has delay of 18.8 ns (47.3% logic delay and 52.7% routing delay) whereas the delay for traditional booth multiplier is 59.252 ns, which justifies the reduction in multiplication. But in terms of cell use Traditional array multiplier provides minimum cell use. Cell use is more for overlay booth multiplier, which indicates the area. Cell use is optimal in reversible 8 × 8 Vedic multiplier. The Comparison of various Multipliers based on delay is shown in **Figure 15**.

It is found that proposed reversible multiplier has less delay than existing one. The Comparison of Reversible Multipliers based on delay is shown in **Figure 16**.

From the above discussion it is found that this multiplier architecture provides an efficient arithmetic unit.

It is found that Quantum cost, number of gates, garbage output and number of constant input lines are less for proposed logical unit than existing one since existing logical unit uses PFAG gate whose quantum cost is 8 and Feynman gate whose quantum cost is 1. The Comparison of Reversible Logic Unit based on Quantum Cost is shown in **Figure 17**.

The quantum cost, number of gates and number of garbage output of Binary to Gray code Converter is 8 and total logical calculation is 8 α. Binary to gray code converter is used in ALU since binary to gray code converter finds its applications in error detection and correction and analog to digital conversion [29] [30].

From the above all it is found that multiplier unit is operating with less delay than the existing one and has less quantum cost. Logical unit also has less quantum cost. On a whole the ALU is efficient in terms of delay, quantum cost, number of gates, and total logical calculations. This multiplier based ALUs can be used in ATMEGA microcontrollers where 8 bit operation is performed [31].

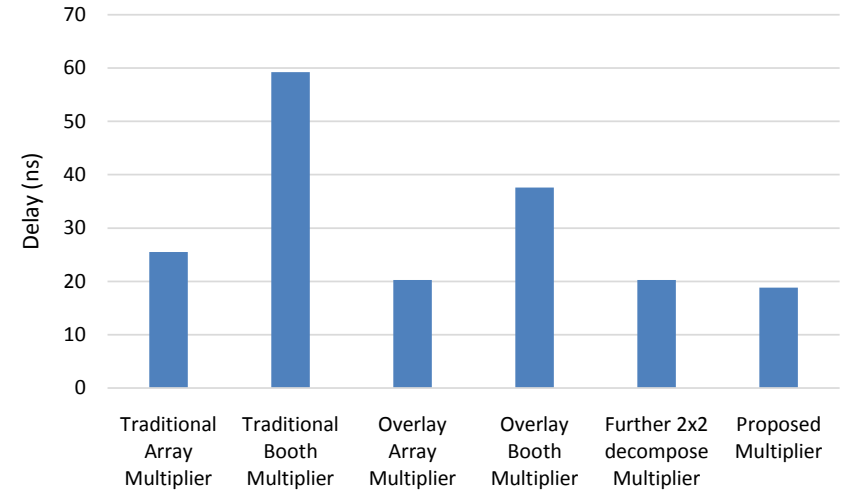

Figure 15. Comparison of various multipliers based on delay.

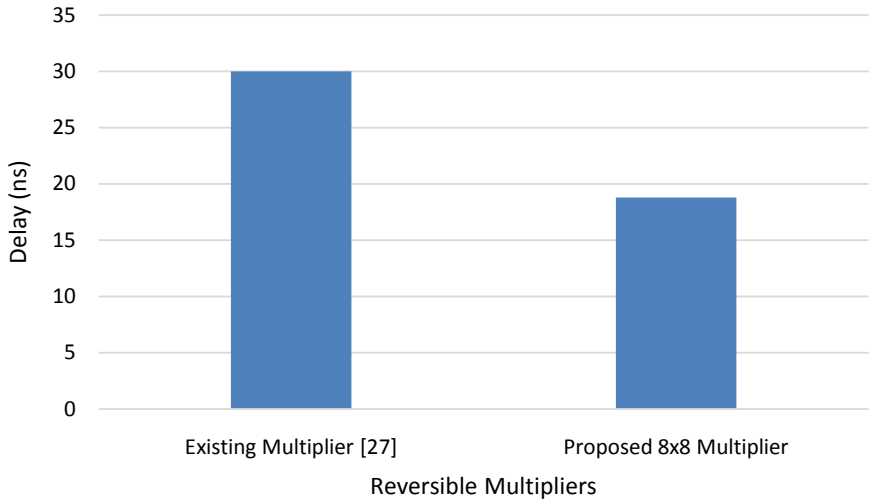

Figure 16. Comparison of reversible multipliers based on delay [27].

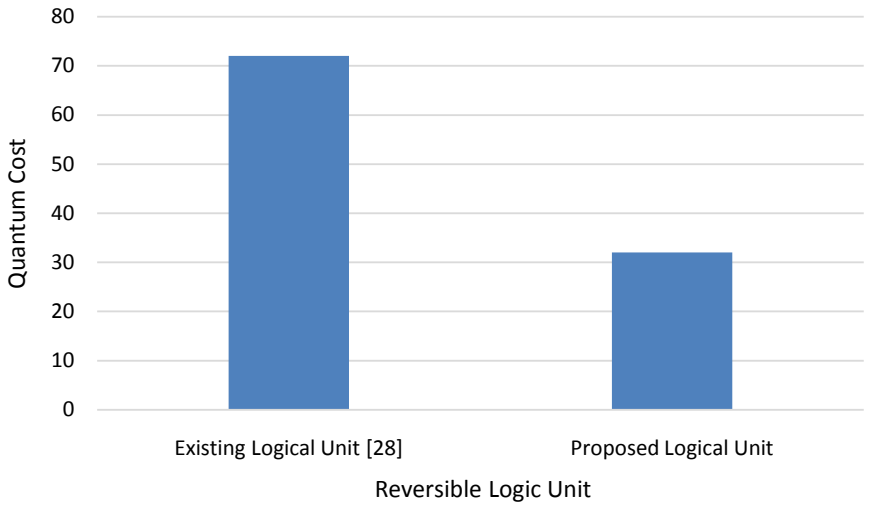

Figure 17. Comparison of reversible logic unit based on quantum cost [28].

Table 2. Comparison of conventional multipliers and reversible logic based multipliers.

Parameters	Conventional Method	Reversible Logic
Number of gates	88	28
Garbage outputs	-	116

4. Conclusion

In summary, the proposed reversible multiplier designed using HNG gate used in ALU shows better results in terms of delay and quantum cost. The proposed reversible logic unit offers better performance in terms of quantum cost. Hence the proposed reversible ALU as a whole performs better than the conventional method in terms of quantum cost and delay. In advanced processor architectures there is a dedicated multiplier unit based ALU. In future these irreversible ALU may be replaced with reversible Vedic multiplier based ALU to reduce the quantum cost and delay. Vedic mathematics can be explored to a greater extent to optimize the various VLSI architectures. It is presented above that when these systems are practically realized they require less number of reversible gates than the conventional method.

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