Algorithm Design of Variable Symbol Rate of QAM Cable Receiver Chip

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Abstract: Concerning with the system level design of QAM cable receiver chip for cable HDTV DSP-based modem application, a receiver structure with joint Quadrature Amplitude Demodulator is introduced, blind decision feedback equalizer (DFE) loop, variable symbol timing recovery loop, carrier recovery loop and AGC loop. The architecture of blind DFE, with Constant Modulus Algorithm (CMA) initialization block, forward and feedback filter, operates in the passband so that equalizer can be adjusted completely independent of carrier phase. The SPWTM simulation and FPGA test confirm that proposed scheme is robust against non-impulse noise, multi-paths and carrier error.

Keywords: QAM cable receiver; algorithm design; joint Operation

1 Introduction

The European Digital Audio-Visual Council(DAVIC) and Digital Video Broadcasting (DVB) standards have selected Quadrature Amplitude Modulation as the modulation format downstream delivery of video and data through coaxial cable networks. The specific application of QAM receiver is cable digital TV set top terminal and cable modem[1]. A QAM cable chip comprises QAM demodulator, synchronization loops and forward error correction(FEC) decoders. The algorithm of QAM receiver chip is adaptive in nature and need to process multiple receiver symbol before convergence is achieved. The algorithm is adaptive receiver structure and referred to as loops. It is certainty that a given loop cannot converge until one or more loops have sufficiently converged.

In high speed data communication system, the accurate timing recovery is critical to obtain the optimal system performance at the receiver. Inter symbol interference (ISI), due to channel induced distortion of the received signals and reflection from unterminated stubs , is familiar problem in digital transmission over bandlimited channels. A usual way of minimizing ISI is adaptive Decision Feedback Equalizer(DFE) in the receiver, in which the feed-forward equalizer(FFE) and feedback equalizer(FBE) are used to cancel the pre-cursor and post-cursor ghosts.

Since the higher error rates and error propagation prevent algorithm convergence under most practice channel condition, Decision-Directed LMS is usually impractical from cold start for high order constellation[2]. So, the four corners technique, which is proposed by Casas[3], and CMA blind equalization technique are used to update filter coefficient initially.

2 QAM Cable Receiver Chip Architecture

The input to the QAM cable receiver is an analog IF signal of up to 50MHz, typically, the IF signal has 36.15MHz center frequency with an 8MHz bandwidth for PAL based systems. The input signal is sampled by the ADC at approximately 28.92MHz for the 36.15MHz IF, the whole QAM receiver chip is given in figure 1.

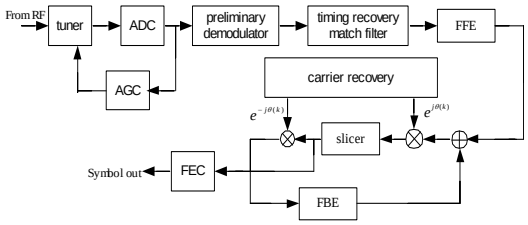

Figure 1. QAM cable receiver chip

2.1 AGC

An automatic gain control function provides two output signals to adjust the RF and IF analog gain stages, so that the A/D input signal is at the optimal range.

2.2 Preliminary Demodulation

Bring the input signals down close to baseband so that the receiver does not have to operate on the high frequency signals. Translation by fsamp/4 is accomplished by mul-

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tiplying the A/D out by sin(pi*n/2) and cos(pi*n/2) to produce the In phase and Quadrature component of the basedband QAM signals.

2.3 Timing R ecovery (TR)

Followed the QAM demodulator, the signal passes through a recirculating decimator, which is an attractive structure that requires one filter core and occupies less silicon area[4]. Figure 2 shows the simplified block diagram of the recirculating decimator architecture with select ratio of 2,4,8, which allows the chip to operate at any user specified symbol rate from 875k Baud to 7M baud. The half band filter is 19-tap with 10 nonzero coefficient in Canonic Signed –Digit(CSD) representation. All the clock signals are designed to be mutually exclusive so that the decimator filtering of all the stages can be computed with one half band filter.

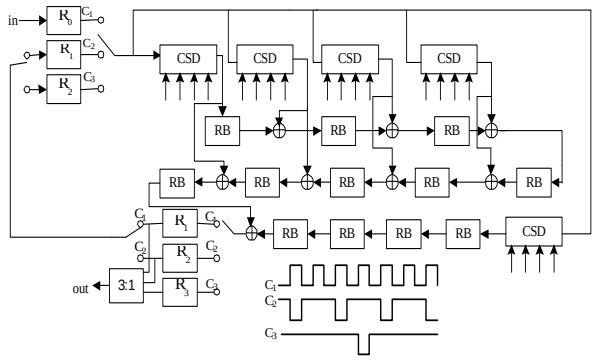

Figure 2. recirculating decimator FIR filter with selective power of two conversion rations

The corresponding transfer function is :

$$H(z) = h_0 z^{-2M+1} + \sum_{i=1}^{M} h_i (z^{-2M+2i} + z^{-2M-2i+1}) \qquad (1)$$

where $M = (N+4)/2, N = 19$ .In Figure 2, RB is register bank which is used to store the intermediate and output samples of each stage. The purpose of TR loop is to obtain the exact position in the center of the symbol. Two quantities must be determined, i.e. sampling frequency and particularly sampling timing phase. The digital TR architecture presented at this paper in Figure 3 provided more advantage over than the mixed approach. This approach has no control over the ADC sampling clock. Number Control Oscillator(NCO) employs the signal from the timing error signal that passed through the loop filter to produce a virtual gated clock to keep track of where the correct sampling time should have been. This sampling time used by the multi-phase interpolator filter to produce data that resample to virtual clock. Here, variables are defined as followed:

$f_{s/2}$: half of sampling rate; f_T :symbol rate, always slower than $f_{s/2}$; M :number of the samples per symbol(here,is 2); $R = f_{s/2}/(Mf_T)$ oversampling rate, always is irrational.

For DTV application, the performance of linear interpolator structure is inadequate. MMSE FIR interpolator with 16 taps is used.

The timing error can be extracted from product of two complex bandpass filter. Two complex bandpass filter with leaky structure are defined as followed

$$B_1(f) = B(f - f_1), B_2(f) = B(f - f_2)$$

with

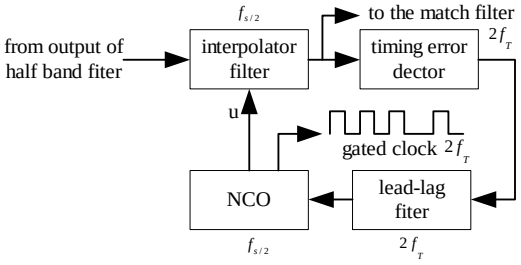

Figure 3. All digital timing recovery architecture

$f_1 = f_0 - 1/2f_T, f_2 = f_0 + 1/2f_T$,their impulse response being related to $b(t)$ by $b_i(t) = b(t)\exp j2\pi f_i t, i = 1,2$. In the timing, the complex output signals can be written as:

$$g_i(t) = \sum_n a_n s_i(t - nT) + n(t) * h_{b_i}(t), i = 1,2 \qquad (2)$$

where, s_i is defined by inverse fourier transforms:

$$s_i(t) = \int_{-\infty}^{+\infty} B(f - f_1) H(f - f_0) e^{j2\pi ft} df . i = 1,2 \qquad (3)$$

It [6] shows that for uncorrelated data symbol, timing error information can be extracted from sampling $\mathrm{Im}\, s_1^* s_2$.

Following the interpolator, the output of timing error detector is sent to a lead-lag filter, which consists of two path, the proportional path and integral path. From control theory, the proportional and integral path can be used to track out sampling phase error and sampling frequency error respectively.

The function of NCO is setting the interpolation phase for the interpolator filter and generation a gated clock, is used decided which of interpolator output should be skipped. The skipping of data can be accomplished in one of two ways, with single clock and with a gated clock. Because single clock has intrinsic drawback(insertion of a MUX before each register), gated clock is served in this paper. The NCO structure is given in Figure 4.

2.4. Dual Mode Blind Equalizer

Adaptive equalizer operates in a receiver to minimize intersymbol interference due to channel induced distortion of the received signals and to combat the effect of micro-reflections from impendence mismatches and reflection from unterminated stubs in high speed digital transmission over band-limited channels. The decision feedback equalizer(DFE) consist of programmable digital filter and coefficient updating circuits. The Decision directed Least Mean Square(DD-LMS) is used to update coefficient according to the following algorithm:

$$w_{(k+1,n)} = w_{(k,n)} + ue_k x^*_{(k-n)} \quad (4)$$

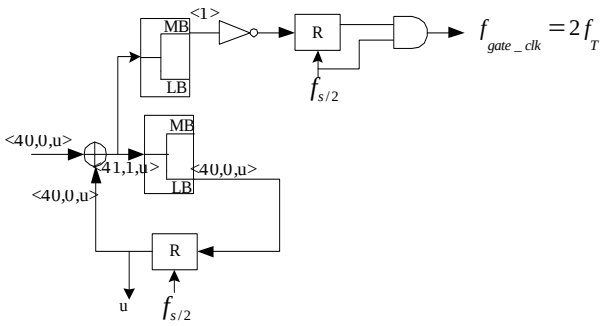

Figure 4. NCO with gate clock

where u is a step size parameter, e_k and $x_{(k-n)}$ are the error signal and input signal vector, respectively. The convergence properties of the DD-LMS given by (4) are governed by the u, because it determines the magnitude of the change or step that is taken by the algorithm in iteratively determining a useful coefficient vector. Instead of full precision multipliers, a simplifications of the LMS updating algorithm, input data sign LMS, is used.

Constant Modulus Algorithm(CMA), which is insensitive to carrier synchronization, is used to update coefficient for blind DFE initialization and reduce the symbol error rate to a level when the decision directed model can begin safely.

The fractionally space equalizer (FSE) mode performs better than the symbol space mode because of its wide bandwidth and is insensitive to the choice of sampling time. Theoretically, T/2 FSE requires circuit operating twice as fast as that of the symbol space equalizer. But the symbol decisions are made at the symbol rate. The poly-phase filter structure was proposed in former design has advantage, since it used the symbol-rated clock [7]. Combined dual mode DFE, CMA and carrier recovery, a modified DFE structure is shown in Figure 5. According to the OpenCable™ set top terminal core requirement, DFE has 24 Feedforward taps and 24 Feedback taps. Figure 6 sh-ows a block diagram of dual mode feedforward equalizer, mux2 selects data path 0 to construct a conventional symbol-rated equalizer, selects data path 1 to construct T/2 FSE. In this mode, the coefficient is separated into odd tap and even tap. The input data (output of TR) with a rate twice as high as the symbol rate are load to DFE, in T/2 space mode, data sampled by the positive edge of the symbol rate clock are load to the even taps and data sampled

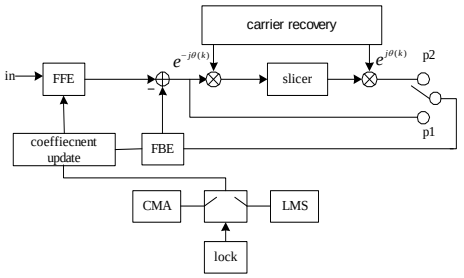

Figure 5. Blind DFE incorporated CR

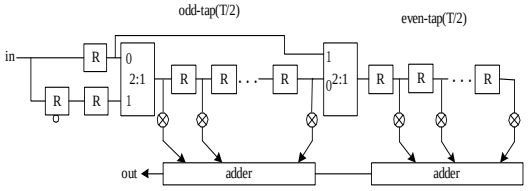

Figure 6. block diagram of dual mode (feedforward equalizer)

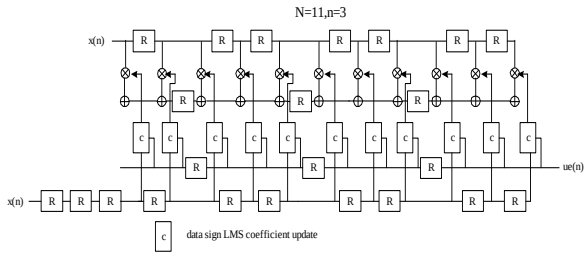

Figure 7. hybrid for m LMS adaptive FIR fi ter(odd-tap)using retiming

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by the negative edge of the symbol rate clock are load to the odd taps.

The directed FSE structure proposed in Figure 6 has computation delay, the critical path is too long .The transpose form overcomes this problem by inserting intermediate delays between each multiply/add operation. For filter with many taps, the power consumption and input data bus limit performance. To implement low-power consumption adaptive equalizer for implementation, The hybrid form (a mixture of direct form and transposed form), one of pipelined structure without introducing extra latency, is applied to the DFE.

The hybrid form is compromise between direct and transposed form for both speed and power [8]. It is based on the retiming principle, i.e. in a system, applying a unit delay to all input is equivalent to applying a unit delay to all outputs. The circuit shown in Figure 7 corresponds to the case of odd tap filter in Figure 6 implemented as 3 tap modules(N=11,n=3).In this case, all filter taps are delayed by $D = \text{int}((N-1)/n)$, the LMS tap update is given by:

$$w_k(n+1) = w_k(n) + ue(n-D)\text{sgn}[x^*(n-D)] \qquad (5)$$

The adders in the output path of the filter are implemented as carry-save Adders(CSA) which are smaller and fasters.

2.5 Decision Directed Carrier Recovery

A widely decision-directed carrier synchronization loop is to remove any residual carrier phase and frequency offset as well as high frequency noise induced by the RF turner. The decision directed carrier synchronization algorithm is described as Figure 8.

3 Joint Operation and Results

The process of the whole chip is given as followed:

The first step of the loop which are allowed to acquire is AGC loop, so the signal at input of A/D is set appropriately.

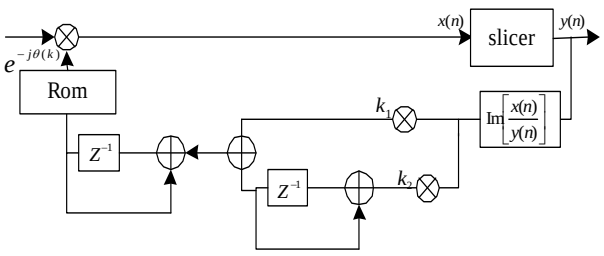
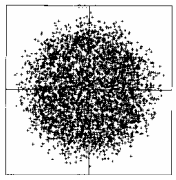


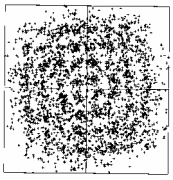
Figure 8. Decision directed carrier recovery block

The signal is digitized, quadratture downconverted to complex value baseband representation. At this point, the signal isn't synchronous with symbol rate and contains the residual carrier frequency. Symbol timing and carrier frequency acquisition are the next step to be perform the symbol frequency is recovery,the resampling of the complex value signal to exactly two samples per symbol. Owing to lack of carrier lock, additive noise, the constellation, shown in Figure 9(a), from the simulation of fixed pointed SPW™, at this point shows no features of bauded distortion. Once symbol timing is obtained, the signal can be blind equalized. Firstly, path p1 is selected in Figure 5 so that a linear IIR structure is used. The equalizer coefficients are adapted from cold start using CMA update. As CMA is carrier invariant, therefore adjust the coefficients without accurate carrier removal. But residual carrier term must be removed. Four corners technique is used. The carrier tracking is operated in a coarse fashion by treating signal as if it is QPSK.Figure 9(b) shows the constellation after the CMA and four corners carrier recovery. After a prescribed number of symbol, path p1 is selected in Figure 5 is also selected, but adaptive coefficients update algorithm is replaced by the DD-LMS. Once the signal has been equalizer and carrier component has been removed. The path p2 is selected in Figure 5, so the non-linear DFE structure is used, path p2 contains a de-rotator and rotator in order to accomplish the slicing on baseband. The passband equalizer output is multiplied by the carrier offset $e^{-j\theta(t)}$ to form the baseband soft decision, the output of the soft decision is multiplied by the $e^{j\theta(t)}$ to re-rotated to form passband sample. The carrier loop and equalizer loop are switched into the decision-directed mode. After a prescribed number of symbols, the constellation resulting from this step is shown in Figure 9(c). The demodulated signal's SNR is 33.5dB.

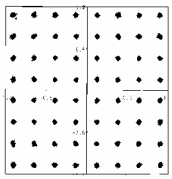
The SPW™ float point and Hardware Design System(HDS) simulation were used to verify above algorithm, Figure 9 is the HDS results. The output of the lead lag filter in TR and carrier loop is given in Figure 9(d),(e) respectively. Xilinx VirtexTM-II 3000 FPGA were employed to testify the all QAM demodulator chip function based on the SPW™ HDS results.



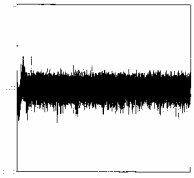
(a) symbol timing sync



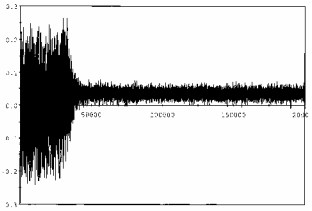
(b) blind Equalizer but no carrier extraction



(c) Decision-directed DFE and carrier track loop



(d) output of lead lag filter of TR



(e) output of lead lag filter of carrier recovery loop

Figure 9. Constellation of 64-QAM signal and the output of lead lag filter

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