The Design and Realization of the Digital Multiplexer based on Electric Power Carrier Communication in Sports facility

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Abstract: The electric power carrier communication is the special communicated way of electrical power system, one kind of double CPU, the low power loss, the low cost digital multiplexer has been designed in conducted the full research to this communicated way, which is satisfied the need of the electric power correspondence transmission system ,especially in sports facility. This article is elaborated the digital multiplexer's hardware and the software principle of design in detail, carries on the simulation using the monolithic integrated circuit simulator, has achieved the satisfactory effect through the debug .

Keywords: Multiplexer; CPU;double RAM;synchronization

1 Introduction

The electric-power line carrier communication, a special communication mode of electric power system, is a highly efficient one suitable for power system communication, especially power dispatching communication, with electric-power lines used as the carrier and substations used as the terminal. Its main features are as follows: only in need of a couple of carrier equipment can non-interrupt and long-range communication be established with the power line carrier; carrier equipment can be directly installed into the two ends of power line ,namely inside the substations, so that the quite short distance between equipment and users is able to improve reliability; when transmission lines have been built and wave trapper, coupling band capacitor, filter, cable and carrier equipment have been set up, then debug can be carried out, and establishment of communication can be fairly quick in doing so, which is simple engineering works. It is very quickly to use in the sports facility's application.

2 The Principle of Digital Multiplex Technology

In digital communication network, some low-speed digital signals in general need merging into a high-speed signal and then transmitting through high-speed channel for the enlargement of transmission capacity and improvement in transmission efficiency. Digital multiplexing is precisely a kind of professional technique that realizes merging of low-speed digital signals. In digital communication network, digital multiplexing is not only such a special technique, coexisting with source coding, digital transmission and digital switching, but also the basis of other technique, such as frame adjustment in network synchronization, line multiplexing in line concentrator, time division access in digital switching, etc. Digital multiplex system, whose structure drawing has been shown by figure 1, consists of digital multiplexer and digital demultiplexer. The former is a device responsible for merging two or more branch digital signals into single combined-channel digital signal in a way of time-division multiplexing; the latter is a device to decompose a combined-channel digital signal into the original branch digital signals. They are usually installed together as a whole known as multiplex demultiplexer, multiplexer for short [1] .

From the principle of time-division multiplex communication[2], it is known that each branch digital signals at the input-end of multiplex unit have to be synchronous, that is, the moment when they take effect has to maintain correct phase relation with the local corresponding timing signal, but at the input end of adjustment unit there is no such demand. If branch digital signals input by multiplexer synchronize with local timing signal, adjustment unit only need to adjust phase, sometimes even not, and this multiplexer is known as synchronous multiplexer; if the input branch

digital signals and the local timing signal are asynchronous, that is corresponding moment when they become effective do not occur at the same rate, adjustment unit will undertake the adjustment of frequency and phase for synchronizing digital signals, and this one is named asynchronous multiplexer; effective moment of inputting branch digital signals appears at the same standard rate, relative to the local corresponding timing signal, and any changes about rate are restricted to the prescriptive range of tolerable error, this multiplexer is termed quasi-synchronous multiplexer.

3 The Overall Design of Digital Multiplexer

3.1 The Hardware Design of Digital Multiplexer

The whole system is composed of PCM encoding and decoding, compression of speech, CPU1, CPU2, dual-port RAM, display, etc[3].

PCM encoding and decoding function can be performed by a piece of MC145480 chip which switches A/D with D/A. MC145480, a general single channel filter of PCM codec with both presampling filter and reconstruction filter, can tolerate all sorts of clock format, such as short frame synchronization, long frame synchronization, Internal Data Connection (IDC) and General Circuit Interface (GCI) timing device; the chip is fitted with a 1.575v reference voltage in accuracy and has no need of external components; its design applies to both synchronous transmission and asynchronous transmission; it has two alternatives--U-law and A-law companding, and the system adopts A-law companding.

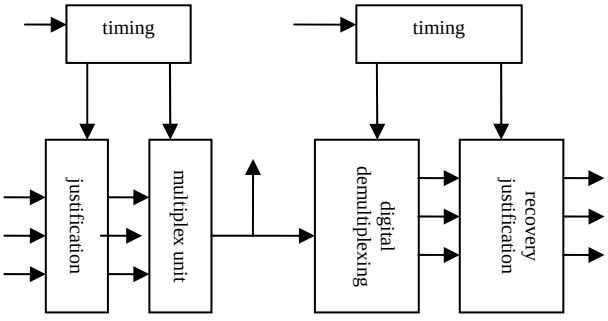

Figure 1. Structure drawing of digital multiplex system

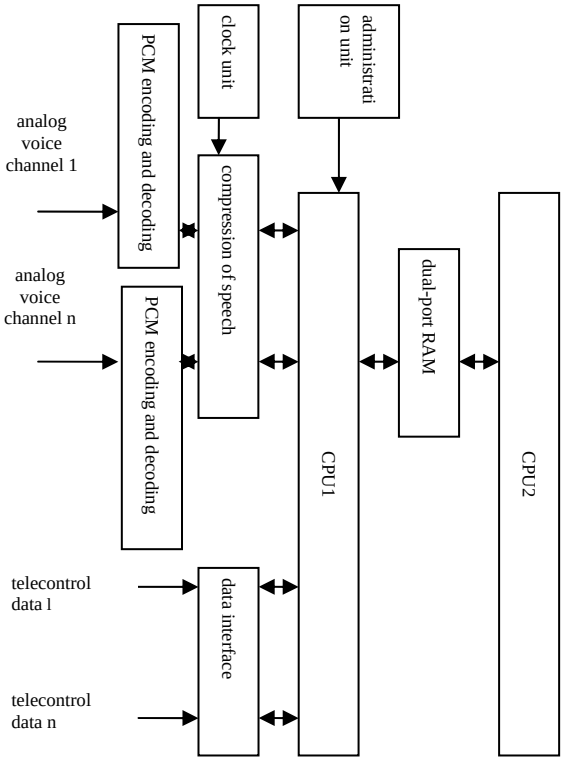

Figure 2. system constitution chart

AMBE-2000TM encoder fulfils the function of compressing[4], encoding and decoding speech. The coding process includes as follows: inputting PCM speech data at a frame of 20ms, speech spectrum with decision of unvoiced and voiced sounds, decision of data rate, dynamic adjustment of data threshold, compressing and packing speech data, etc. Compressed encoding packet which is 34 bytes forming at last is provided for Microprocesso CPU1 to process and accomplish data storage.

Clock circuit mainly completes circuit design of the total clocks which encoding and decoding needs. The clocks the whole system needs all derive from the clock produced by the same crystal oscillator, or the same clock source. Therefore, the whole system is synchronous.

Dual-port RAM performs a role of storing speech and data received from distance and collected from near-end, but equally it functions as a shared mailbox of double CPU to store markers, pointers, etc. and coordinate the work of the two CPUs.

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3.2 The Software Design of Digital Multiplexer

Due to the special structure of multiplex branch information, CPU1 puts the collected data and speech into dual-port RAM. Since both memory and CPU operate data and speech by 8bits, the method of multiplexing by bytes is applied for the convenience of programming.

CPU1 mainly collects and reduces speech and data, but it cannot function normally until CPU2 synchronizes with remote end. CPU2 is the core of multiplex system for speech and data and accomplishes it through multiplex and demultiplex pointers according to frame structure. In the meanwhile, it communicates and exchanges data with CPU1 through dual-port RAM. The software of complete CPU2 is divided into two parts: main program and interruption sub program. Interruption sub program deals with multiplexing and demultiplexing data and speech demanded strictly in real time, while main program is responsible for the rest. Main program consists of multiplexing and demultiplexing and its flow chart has been shown by figure.3; figure.4 shows flow chart of CPU2 interruption sub program.

The process of initialization contains: defining reading and writing pointers of each branch, defining double CPU communication sign and setting serial port and timer. Because of real time demanded strictly in the process of speech communication, the serial port and timer need setting up correctly.

In the process of synchronized checking, only hunting for three synchronization codes can the local side be confirmed to be synchronous, at the same time, examining the other side's state, multiplexing and demultiplexing can be carried out normally provided that the other side is synchronized as well.

4 The Debugging Process and Simulation Results

The system employs the monolithic integrated circuit simulator as simulating device to debug. Inserting the simulator on the target board instead of CPU

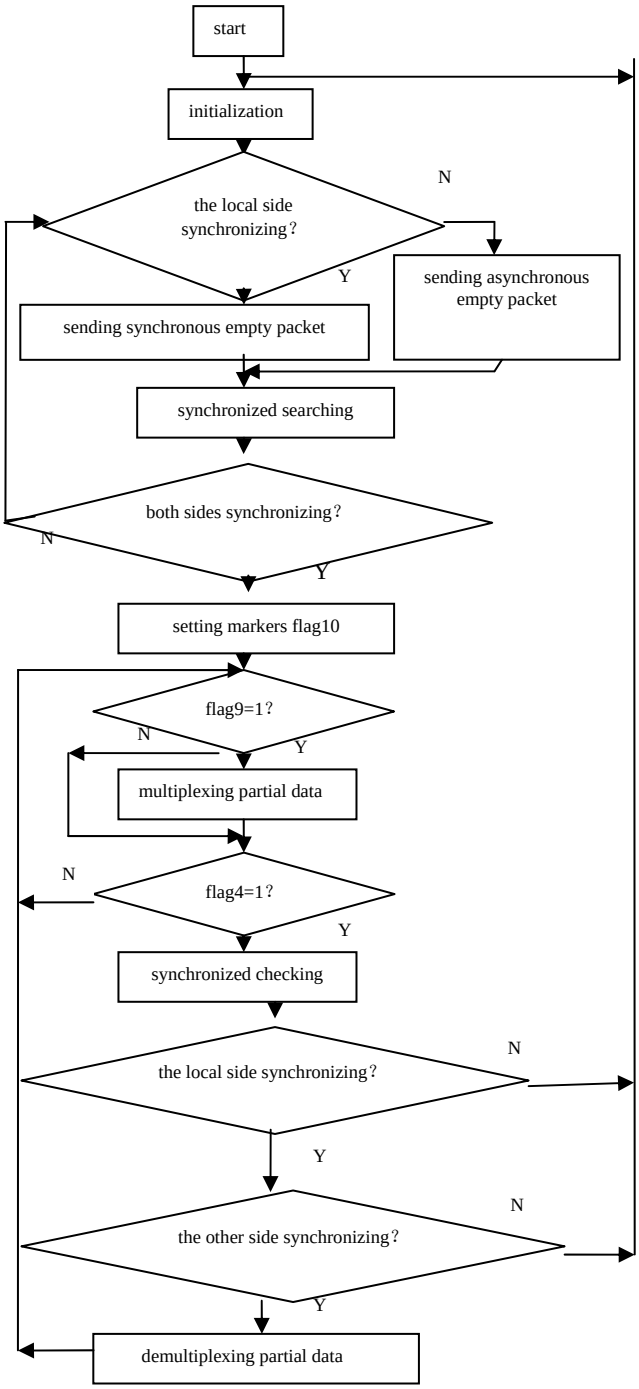

Figure 3. Flow chart of CPU2 main program

component, through PC computer modifying program on line, examining the content stored in memory and register, and making the observed data correspond to reality, all the demanded functions can be fulfilled by program at last.

The whole system carries on the debug step by step: (1) One-way work of debugging the single-channel voice:

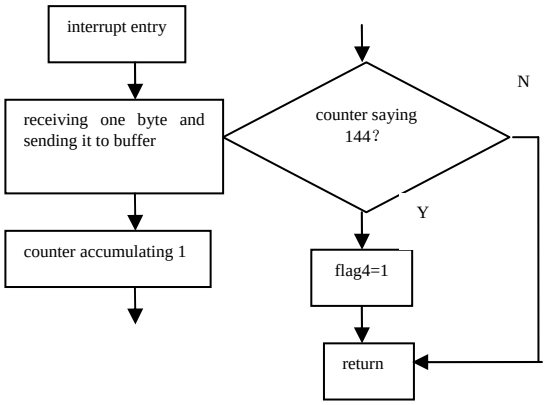

Figure 4. Flow chart of CPU2 interruption sub program

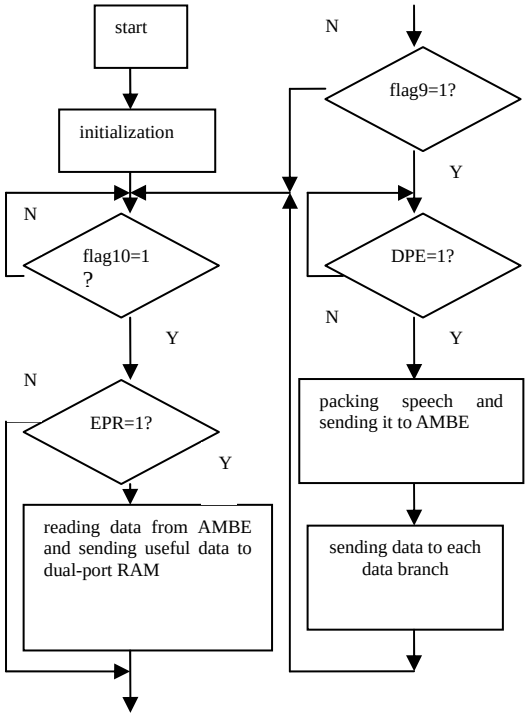

Figure 5. Flow chart of CPU1 program

Figure 5 shows the flow chart of CPU1 program. simulation experiment do not use carrier at the present time. Instead, near end's and distal end's multiplex and demultiplex system link up. The local side speaks after off-hook and the other side manages to hear, and the single-channel debug achieves success. (2) Single channel's double talk debug: modify program based on the first step, and both sides can talk in real time after off-hook, which proves devices and lines normal. (3) One-way communication debug of multiplexing multi-channel speech: multiplex two channel voices on the local side and modify program, the results show the other side succeeds in hearing it respectively through two telephones. One-way multiplex debug succeeds. (4) Two way communication debug of multiplexing multi-channel speech, modify program first, then both sides multiplex and demultiplex two voice channels and conduct a two-way talk in real time on the two telephones of each end. The results are two sides of each channel manage to talk and that voice is clear comparatively and that partial speech channel is debugged in success.(5) After voice channel has been debugged successfully and partly, in multiplex and demultiplex frames add data and debug partly, at last connect the modem and then debug speech communication. Since both sides spend a bit longer time holding modem, it takes about ten seconds for the whole system to establish synchronization and work normally.It is the very suitable sports facility to apply for short time consuming, high safety coefficient and low expense.

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