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Realization of DQPSK-DSSS Modulator on FPGA

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Abstract: This paper uses the phase selected by logic to achieve DQPSK-DSSS modulator, which is consisted of PN generator, Mod-2 addition, S/P, differential code, phase selected by logic and DDS. A method of realizing the modulator based on FPGA is presented using VHDL and basic component of quartusII 5.1 tools of Altera. The proposed method is verified by simulation experiment.

Keywords: DQPSK modulator; DDS; FPGA

1 Introduction

[1] Shows that spread spectrum is a modulation technique which increases the transmit signal bandwidth. There are several benefits obtained in exchange for this increased bandwidth. First, spread spectrum modulation mitigates the effect of inter symbol interference (ISI) and narrowband interference. In addition, spread spectrum also "hides" the signal beneath the noise floor. There are two common forms of spread spectrum: direct sequence and frequency hopping. Since direct sequence spread spectrum (DSSS) is more commonly used, we will focus on this technique. With ultra large scale integrated circuit appearance, Field Programmable Gate Array (FPGA) has used widely in the communication system day by day. At present many kinds of methods to realize DSSS modulation in transmission based on FPGA have been proposed.

This paper mainly discusses the relevant topics that DSSS modulation is realized by Differential Quadrature Phase Shift Keying (DQPSK) which is realized by a Direct Digital frequency Synthesis (DDS) technique. A phase change from one to another is simply controlled by two arrays. This technique can be applied simply and conveniently. The model is simulated on the base of QuartusII5.1, a FPGA development platform developed by Altera.

2 Model of DQPSK-DSSS Modulator

The block diagram shown in Figure 1 illustrates the method for impressing the pseudo-noise (PN) sequence on the transmitted signal is to alter directly the data sequence by mod-2 addition with the PN sequence, and the adder outer is used in conjunction with the DQPSK modulation to shift the phase of the DQPSK signal is called a direct sequence (DS) or a pseudo-noise (PN) spread spectrum signal.
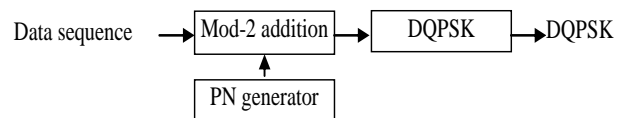

Figure 1. Block diagram of DQPSK-DSSS modulator

3 Basic Principle of DQPSK Modulation

There are two kinds of implementation for DQPSK modulator, one is phase selected by logic, and the other is quadrature modulation. This paper uses the phase selected by logic to achieve DQPSK modulator. The modulator is consisted of S/P, differential code, phase selected by logic and DDS in this paper, as shown in Figure 2.

4 Realization of DQPSK-DSSS Modulator on FPGA

4.1 DS Circuit

In the model shown in Figure 1, the DS circuit is consisted of PN generator and mod-2 adder circuits, which are realized by QuartusII5.1 shown in Figure 3. PN spread-spectrum sequence used in this paper is m sequences, which is also the longest linear shift register sequences. Pseudo-random sequence is used in code length of 31 m-sequence in this paper, so we use five D flip-flop to produce 31 m sequence, tap location [2 5], its polynomial is f (x) = x5 + x2 + 1.Mod-2 addition is realized by logic xor gate. The PN sequence and the infor-
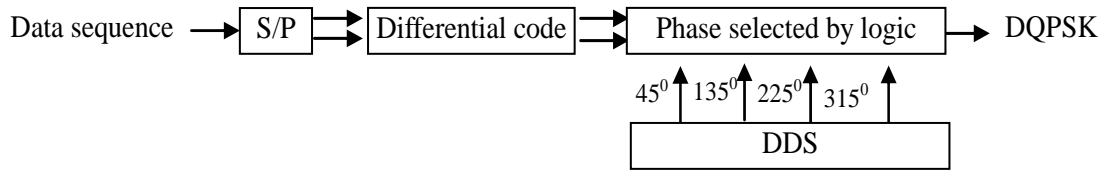
Data sequence → S/P ⇒ Differential code ⇒ Phase selected by logic → DQPSK

45^0 ↑ 135^0 ↑ 225^0 ↑ 315^0 ↑

DDS

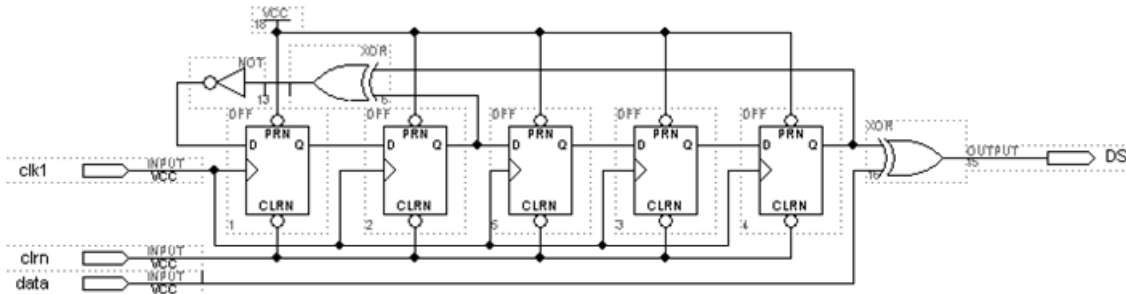**Figure 2. Block diagram of DPSK modulator**

Figure 3. DS circuit

mation data are mod-2 addition, and the PNsequence has a much narrower than the data, so as to achieve the purpose of spread spectrum.

4.2 Serial-to-Parallel and Differential Code Circuit

The data sequence is separated by the serial-to-parallel converter (S/P) to form the odd-numbered-bit sequence for I-channel and the even-numbered-bit sequence for Q-channel. The circuit for S/P is shown as Figure 4.
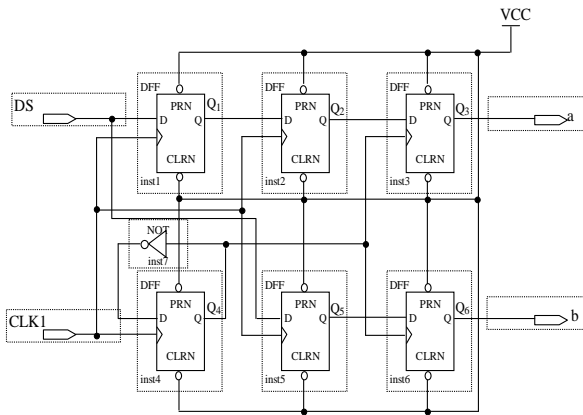

Figure 4. SP circuit

Differential coder converts absolute code into relative code. Let {a} be the original binary data sequence, then a differentially encoded binary data sequence {r} is pro-

duced according to the following rule.

$$Z_{ir} = Z_{ia} + Z_{i-1r} \tag{1}$$

In Formula (1), a subscript designates absolute code, r subscript designates relative code; sign i is the serial number of quaternary symbol, Here sign + indicates modulo-4 addition.

$$Z_{ia} = a_i \bullet 2^1 + b_i \bullet 2^0$$
$$Z_{ir} = c_i \bullet 2^1 + d_i \bullet 2^0 \tag{2}$$

According to Formula (2), we get the result as follow.

$$c_i \bullet 2^1 + d_i \bullet 2^0$$
$$= a_i \bullet 2^1 + b_i \bullet 2^0 + c_{i-1} \bullet 2^1 + d_{i-1} \bullet 2^0$$
$$= (a_i + c_{i-1})2^1 + (b_i + d_{i-1})2^0 \tag{3}$$
$$= (a_i \oplus c_{i-1} \oplus b_i \bullet d_{i-1}) \bullet 2^1 + (b_i \oplus d_{i-1}) \bullet 2^0$$

Then we can obtain the following formula.

$$c_i = a_i \oplus c_{i-1} \oplus (b_i \bullet d_{i-1})$$
$$d_i = b_i \oplus d_{i-1} \tag{4}$$

From Formula (4), we can obtain quaternary differential coding circuit, which is showed as Figure 5. Figure 5 shows the simulation result of quaternary differential encoding. Here clk2 is the clock signal, a b is the absolute code; c d is the relative output code.
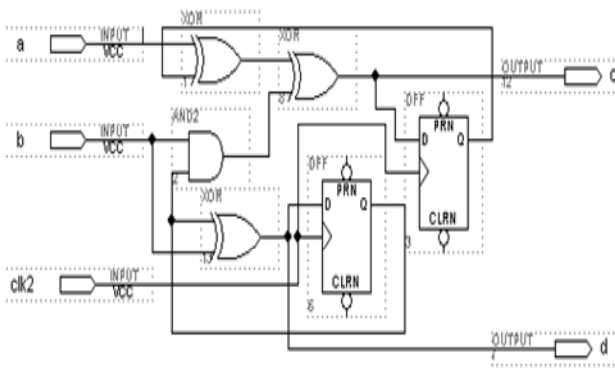
Figure 5. Differential code circuits

4.3 Four-Phase Carrier Generator

Figure 6 showed Four-phase carrier generator that typically consists of two accumulators and a Look Up Table (LUT). DDS as reported in the literature [2-4] generally consisted of phase accumulator, LUT and phase selected by logic which consisted of phase modulator.
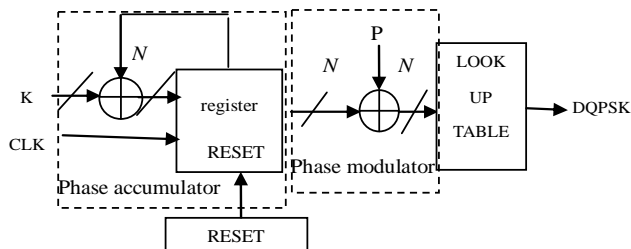

Figure 6. Block diagram of four-phase carrier generator

4.3.1 LUT

The DDS is used for generating waveforms by LUT which the samples of a harmonic function are stored in. Samples may be stored either in the distributed memory or in the block memory in FPGA structure. If data line width of phase-accumulator is N, there are 2N sampling points. Calculating the amplitude of 2N sampling points using other tool to, then the phase increment of two adjacent sampling points is $2\pi/2N$, the phases of 2N sampling points are determined by the amplitude of the sampling points, LUT stored the amplitude of 2N sampling points in turn, so the allusive relationship is established between the phase of the sampling point (memory address) and the amplitude.

4.3.2 Phase accumulator

Assuming that the initial value of phase accumulator is 0 and cumulative step length for the frequency control word is K, then every clock cycle (1/fclk) for the phase increment is $K\times2\pi/2N$, getting a complete sine wave cycle needs $2\pi/(K\times2\pi/2N)=2N/K$ cumulative times, so Tout, the output signal cycle, is $(1/fclk)\times2N/K$, fout, the frequency of the output signal, is $K\times fclk/2N$.

4.3.3 Phase modulator

When the rising edge of each two-bit symbol is advent, a reset signal (RESET) is produced to clear the DDS phase accumulator, then the initial phase of carrier signal is only controlled by the phase control word (P) in order to ensure the initial phase is in line with the carrier phase for the symbol QI. While in other cases, let the sum of the phase accumulator output and P is the phase for the common carrier signal to realize phase modulation.

In this paper, let N=10, firstly we calculate the amplitudes of $2^{10}=1024$ sampling points and express them with 8-bit binary. When phase is $\pi/4$ and $3\pi/4$, the corresponding amplitude is 218, the storage address is 0001111111 and 0101111111 respectively; when phase is $5\pi/4$ and $7\pi/4$, the corresponding amplitude is 38, storage address is 1001111111 and 1101111111 respectively.

```
if clk'event and clk='1' then b<=QI(1); c<=QI(0);
if (clk1h='1' or clk1l='1' or clk2h='1' or clk2l='1') then
case QI is
when "00"=>uuu<="1001111111";reset<='1';
when "01"=>uuu<="0101111111";reset<='1';
when "10"=>uuu<="1101111111";reset<='1';
when "11"=>uuu<="0001111111";reset<='1';
when others=>uuu<="0000000000";reset<='1';
end case;
else uuu<=uuu+"0001000000";reset<='0';
end if;
```

The above VHD code is used in this paper to complete the circuit of phase selected by logic. As it showed, if the rising edge of each QI symbol is advent ,the $\pi/4$, $3\pi/4$, $5\pi/4$, $7\pi/4$ phase is selected separately, then the circuit produces four different phase of the carrier.
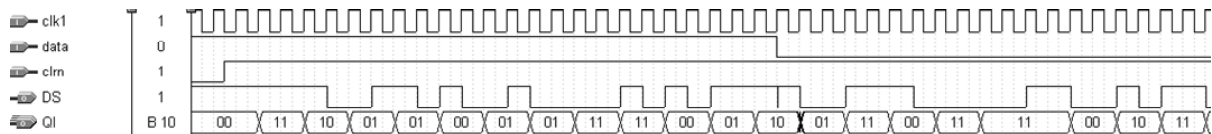
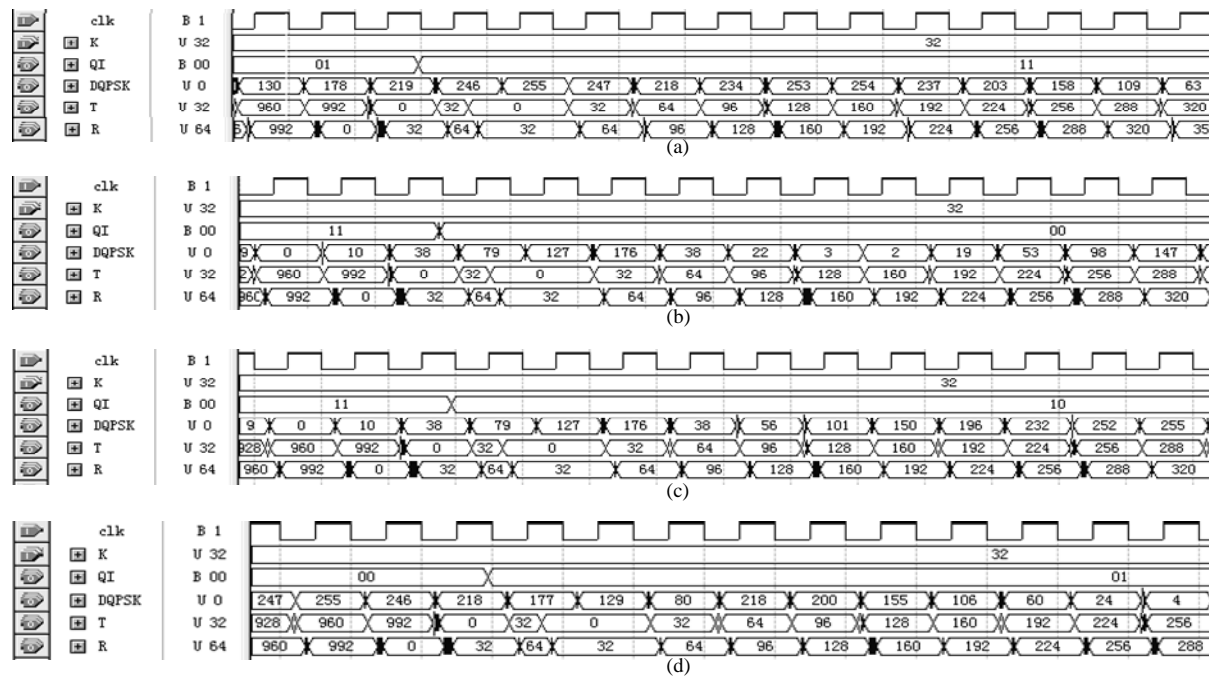**Figure 7. Simulation of from DS to differential code circuits**

Figure 8. Simulation of DQPSK modulator

5 Simulation Results

In the simulation experiment, let fclk=294912Hz，M=48，K=32, then fclk1=fclk/M=6144Hz, fclk2=3072Hz, fout, the carrier frequency is K×fclk/2N=9216Hz, the simulation results by Quartus Ⅱ 5.1 are shown as Figure 7 and Figure 8.

In Figure 7, clrn is a reset signal, clk1 is the input clock signal, PN is m sequence, the simulation output PN sequence: 0000011001011011110101000100111. From Figure 3, the information data and PN are mod-2 addition, and when the data is 0, DS is the same as PN, when the data is 1, DS and PN is opposite. Finally, the DS signal through the serial-to-parallel conversion, differential encoder is to be two coded signals QI, the output simulation result is correct.

In Figure 8 (a), when QI is 11 and the first rising edge of the clock signal clk is advent, RESET signal resets the DDS register (T=0), the phase accumulator output R is

32 and keep the value for one clock cycle; when QI is 11 and the third rising edge of the clock signal clk is advent, DQPSK is 218, which is consistent with the theoretic analysis when QI is 11, the initial phase of the carrier is π/4, the amplitude is 218. Similarly, when QI is 00, 10, 01, respectively, the simulation results are shown as Figure 8 (b-d). The third rising edge of the clock signal clk is advent; the results of the initial phase of the carrier and the amplitude are also consistent with the theoretical analysis results. Although DQPSK is produced after three clock cycle, the delayed time of the symbol QI is same, which does not affect the realization of QPSK; On the other hand, the delay time is less than one-third of the system clock cycle, it can be ignored.

6 Conclusions

The direct sequence spread spectrum is one of the most used spread-spectrum approach in two areas of the military anti-jamming communications and mobile

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communication systems. So it is imperative to actively carry out the study of direct sequence spread spectrum communications. [5] shows that realization of DQPSK-DSSS modulator on FPGA overcome many defects of traditional analog modulator such as large volume, high expense, debugging difficultly and long production cycle. The innovation of this article lies in that the system is achieved with FPGA in addition to DA, which has a certain reference value for the realization of other modulator (such as QPSK, 8PSK, QAM, etc.), as well as the application in the software radio on FPGA.

7 Acknowledgements

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