

Robust Optimization for Gate Sizing Considering Non-Gaussian Local Variations

Jin Sun, Janet M. Roveda

Department of Electrical and Computer Engineering, The University of Arizona, Tucson, USA

Email: sunj@email.arizona.edu, wml@ece.arizona.edu

Received 1 July 2014; revised 2 August 2014; accepted 11 August 2014

Copyright © 2014 by authors and Scientific Research Publishing Inc.

This work is licensed under the Creative Commons Attribution International License (CC BY).

<http://creativecommons.org/licenses/by/4.0/>



Open Access

Abstract

This paper employs a new second-order cone (SOC) model as the uncertainty set to capture non-Gaussian local variations. Then using robust gate sizing as an example, we describe the detailed procedures of robust design with a budget of uncertainty. For a pre-selected probability level of yield protection, this robust method translates uncertainty budgeting problems into regular robust optimization problems. More importantly, under the assumption of non-Gaussian distributions, we show that within-die variations will lead to varying sizes of uncertainty sets at different nominal values. By using this new model of uncertainty estimation, the robust gate sizing problem can be formulated as a Geometric Program (GP) and therefore efficiently solved.

Keywords

Robust Gate Sizing, Second Order Cone, Geometric Programming, Budget of Uncertainty, Parameter Variations

1. Introduction

Due to the decreasing feature sizes, the advanced sub-wavelength semiconductor fabrication techniques fail to control precisely dopant diffusion [1] [2] and are unsuccessful in printing geometric features accurately [3]. Consequently, a significant amount of process variations are introduced into the integrated circuits. These variations have caused substantial changes in the device and interconnect electrical parameters. The parametric yield of manufacture process and performance are thus in jeopardy. This is the main reason why process variations are the key topics of recent research studies.

Most research publications [1]-[3] classify process variations into inter-die or global and intra-die or local two components. Here, the global variations include variations between different chips, either in the same wafer or different wafers. Local variations include variations existing in different devices or interconnect within the same chip. Global variations are in general modeled as Gaussian distributed random variables. Local variations, on the

other hand, are not easy to capture. One reason is that local variations, also random in nature, exhibit strong spatial correlations. To illustrate, two devices or interconnects are strongly correlated if they are spatially close to each other. If they are far apart, the correlations may be neglected. In addition, [4] and [5] have pointed out that it is not accurate to use Gaussian distribution to model local variations. In particular, [4] suggested a new statistical model, the Matern model, to capture the local variations based on the measurement data for 90 nm chips. The contributions of this paper can be summarized as follows. First, we propose a new Second-Order Cone (SOC) uncertainty model for characterizing parameter variations. This new SOC model extracts the quadratic and even higher order spatial variations with regard to correlations. Given certain probability for performance, we show how to translate budget uncertainty problems to yield-guaranteed robust optimization problems. By employing the SOC estimation model under yield-guaranteed timing constraints, we can translate the robust gate sizing problem into a standard GP formulation and conduct a budget of uncertainty between timing yield and gate size variations. Finally, we thoroughly verify the accuracy of our models against Gaussian distribution based models with a number of circuits. The rest of the paper is organized as follows. Section 2 describes the concepts of budget of uncertainty, non-Gaussian distributed variations and their impact on defining uncertainty set for variation estimation. Section 3 introduces the Second-Order Cone (SOC) estimation model for characterizing parameter uncertainties. Section 4 develops the proposed robust optimization technique by using the SOC uncertainty model and the notion of uncertainty budgeting. Section 5 demonstrates experimental results, and finally Section 6 concludes this paper.

2. From Uncertainty Budgeting to Robust Gate Sizing

Most research works on timing analysis and gate sizing use a posynomial function to model gate delay for individual components [6]-[10]. In [8] the authors proposed a class of generalized posynomial models to approximate gate delays. The timing constraints can be represented in the following form:

$$d_j(X) = \sum_{k=1}^K c_k \cdot x_1^{a_{1k}} x_2^{a_{2k}} \cdots x_n^{a_{nk}} = \sum_{k=1}^K c_k \cdot \left(\prod_{i=1}^n x_i^{a_{ik}} \right) \quad (1.1)$$

where the j -th constraint function $d_j(X_0)$ represents the path delay at gate j , which is in posynomial form. If the multiplicative coefficients c_k 's are allowed to be any real number, then $f(X)$ is called a signomial. As there are no restrictions on the sign of coefficients c_k 's, signomials are expected to estimate delay functions more accurately. In this work, we employ the signomial model for gate delay approximation. We use an automated procedure of posynomial/signomial fitting to determine the best-fit coefficients, exponents and the number of terms in the signomial delay function. The fitting procedure starts with a single monomial term for delay approximation, and gradually increase the number of monomial terms in the signomial function until the fitting error is less than a pre-determined threshold value.

Design optimization affected by process introduced variations has been a focus of recent research efforts [11]-[14]. How to formulate the design optimization depends on the models of variations. Indeed, it has also been pointed by [15] that "solutions to optimization problems can exhibit remarkable sensitivity to perturbations in the parameter". Process variations are generally modeled as random variables. A nature way is to formulate design optimization affected by parameter uncertainty as a stochastic optimization problem. In this section we will use gate sizing, a typical circuit design problem, as an example to explain how to employing the notion of uncertainty budgeting to translate a in general NP-hard stochastic problem [16] into a tractable robust optimization problem.

Due to process variations, the components of vector X_0 , *i.e.* the gate sizes, have been assigned random variations around their nominal values. In this sense gate sizes are no longer deterministic quantities but random variables. As a consequence the gate delay becomes variational as well. Let $\delta X = [\delta x_1, \delta x_2, \dots, \delta x_n]$ represent the variations in gate sizes, the objective function $\sum_i \alpha_i x_i$ and constraint function $d_j(X_0)$ in (1.1) will be replaced by $\sum_i \alpha_i (x_{i0} + \delta x_i)$ and $d_j(X_0 + \delta X)$ respectively. Therefore, the gate sizing problem under parameter uncertainties becomes the following stochastic optimization formation:

$$\begin{aligned}
& \text{minimize : } \mathbb{E} \left[\sum_i \alpha_i x_{i0} \right] \\
& \text{subject to : } \text{Prob} \left\{ d_j (X_0 + \delta X) \leq T_{\text{spec}} \right\} \geq \eta \\
& \quad X_{\min} \leq X_0 \leq X_{\max} \\
& \text{variables : } X_0 = [x_{10}, x_{20}, \dots, x_{n0}]
\end{aligned} \tag{1.2}$$

As shown in (1.2), stochastic optimization tries to find the optimal nominal design parameters such that under the impact of parameter variations around these nominal values, the objective function is optimized in an average sense (*i.e.* the mean value), and constraints are satisfied with a probabilistic guarantee η .

The most simplistic formation of uncertainty set is to use interval information and model a parameter under variation as a symmetric and bounded random variable \tilde{x}_{i0} that takes values in $[x_{i0} - \hat{x}_i, x_{i0} + \hat{x}_i]$. The half-length \hat{x}_i measures the precision of the estimate. Associated with the uncertain data \tilde{x}_i , we define the random variable $\gamma_i = (\tilde{x}_i - x_{i0})/\hat{x}_i$ which obeys an unknown but symmetric distribution, and takes values in $[-1, 1]$. All resulting γ_i 's form an uncertainty set:

$$\mathcal{U} = [\gamma_1, \gamma_2, \dots, \gamma_n] \tag{1.3}$$

The main limitation of robust optimization is the lack of probabilistic description of parameter uncertainty and the conservativeness of optimization results due to the assumption of a complete guarantee of full yield. In this case, we might ask for probabilistic guarantees for the robust solution that can be computed *a priori*, *i.e.* as a function of the structure and size of the uncertainty set. This provides a notion of a budget of uncertainty, which allows the designer a level of flexibility in choosing the tradeoff between robustness and performance, and also allows the ability to choose the corresponding level of probabilistic protection. To be specific, the robust optimization with uncertainty budgeting can be formulated as:

$$\begin{aligned}
& \text{minimize : } \sum_i \alpha_i x_{i0} \\
& \text{subject to : } d_j (X_0, \mathcal{U}(X_0, \eta)) \leq T_{\text{spec}} \\
& \quad X_{\min} \leq X_0 \leq X_{\max} \\
& \text{variables : } X_0 = [x_{10}, x_{20}, \dots, x_{n0}]
\end{aligned} \tag{1.4}$$

where \mathcal{U} stands for the uncertainty set, of which the size can be computed *a priori* given a pre-selected η . Note that uncertainty set \mathcal{U} is usually modeled as a function of both nominal design parameters and probabilistic guarantee. Still use the example of interval uncertainty set (1.3) to interpret, we define a parameter as a budget of uncertainty for timing constraint:

$$\sum_{i=1}^n \gamma_i \leq \Gamma. \tag{1.5}$$

The parameter Γ , which belongs to $[0, n]$, is interpreted as the maximum number of parameters that can deviate from their nominal values. If $\Gamma = 0$, all γ_i 's are forced to 0, and there is no protection against uncertainty. If $\Gamma = n$, the timing constraint is completely protected against uncertainty, which yields a very conservative solution. If $\Gamma \in (0, n)$, the designer makes a trade-off between the protection level of the constraint and the conservativeness of the solution. In later part, we show that by employing the concept of second order cone, there exists a convenient and efficient uncertainty set that provides such flexibility at different level of yield protection.

3. Parameter Variations and Uncertainties Characterization

The two main problems in budgeting uncertainty in robust optimization are to set up an appropriate uncertainty set for parameter uncertainty and establish the dependency of probabilistic guarantee on the structure and size of uncertainty set. This section first discusses estimation models for characterize parameter variability. We start with introducing the previously used UE method and its disadvantages. A new USOC method will then be proposed to overcome the limitations of UE method.

Ellipsoidal uncertainty set (UE) [11] [17] [18] is widely used to model parameter uncertainty, by using the maximal inscribed ellipsoid inside the variation region. For any vector $X \in R^n$ with random perturbation around its nominal value X_0 , the parameter variability can be estimated by an uncertainty ellipsoid in R^n , which has the form [19]:

$$\left\{ X \mid (X - X_0)^T P^{-1} (X - X_0) \leq 1 \right\} \quad (1.6)$$

where P represents the covariance matrix. The nominal vector X_0 is the center point of the uncertainty ellipsoid. An alternative representation of an uncertainty ellipsoid is:

$$\left\{ X_0 + P^{1/2} u \mid \|u\|_2 \leq 1 \right\}. \quad (1.7)$$

The vector u is introduced to characterize the movement of X around X_0 , and $\|u\|_2$ is the 2-norm of vector u . The parameter variations are considered to be bounded within the ellipsoid region. Covariance matrix P determines how far the uncertainty ellipsoid extends in every direction from X_0 . The lengths of radiuses λ_1 and λ_2 , and their directions are given by the eigenvalues of matrix P .

In this work we propose a novel uncertainty set to model parameter uncertainties by employing the concept of a second order cone (SOC). Mathematically, a unit second order cone of dimension k is defined as [20]:

$$\left\{ \begin{bmatrix} U \\ r \end{bmatrix} \mid U \in R^{k-1}, r \in R, \|U\| \leq r \right\} \quad (1.8)$$

where U is a vector of dimension $k-1$. For the random vector X of gate sizes, by introducing an auxiliary variable r , the variation vector δX can be represented by a second order cone, which is defined as a set:

$$\left\{ (\delta X, s) \mid \|\delta X\|_2 = \|X - X_0\|_2 \leq s, s \geq 0 \right\} \quad (1.9)$$

where $\|\delta X\|_2 = \delta X^T \delta X$ is the 2-norm of variation vector δX . A general-form second-order cone can be extended from the unit case in (1.9):

$$\left\{ (\delta X, s) \mid \|A\delta X + b\|_2 \leq c^T \delta X + d \right\} \quad (1.10)$$

where problem parameters are $A \in R^{l \times n}$, $b \in R^n$, $c \in R^n$ and $d \in R^n$. For illustrative purpose, in what follows we use the simple case of unit SOC to explain the advantageous of SOC uncertainty set over ellipsoidal uncertainty set. Referring to the example shown in Figure 1(a), a 3-dimensional (3D) cone has continuously changing radiuses to their 2D slices. The intersections of the 3D cone and feasible region thus provide the corner case distances to the nominal case. For example in Figure 1(a), the cone-feasible region intersection captures one corner case (Point A) with radius s_1 . If we push the cone through the feasible region continuously, more corner cases with different distance to the nominal point will be captured. As an example, a new corner point B is identified with a different radius s_2 . The elastic radius s in fact restricts how far the parameter variations can perturb from their nominal values.

Having explained the formation of SOC uncertainty set, a nature question is how to determine an explicit form of s_{\max} in terms of nominal design parameters. We use a fitting technique to find out the relationship between s_{\max} and nominal gate sizes by sampling gate size variations from their distribution information. As introduced before, local variations are difficult to capture, especially in the presence of strong spatial correlation. Following [4] [21] [22] the die can be considered as consisting of a grid of $n_1 \times n_2$ locations. A location on the chip will be denoted by $l = (x, y)$ where x is the horizontal coordinate and y is the vertical coordinate. Each grid field will be considered as a random variable with mean μ_k , where μ_k does not depend on the location l but is dictated by the inter-die variations and varies from chip to chip. The parameter variations at any two locations l and l' on the same chip will be correlated. The correlation is typically strong at nearby locations and weak for locations far away from each other. The covariance between two locations l and l' only depends on the distance $h = \|l - l'\|$ between l and l' . Then the distribution of parameter variation is completely determined by its covariance function, which can be written as:

$$\text{Cov}(x(l), x(l')) = \sigma_l \sigma_{l'} \rho(\|l - l'\|). \quad (1.11)$$

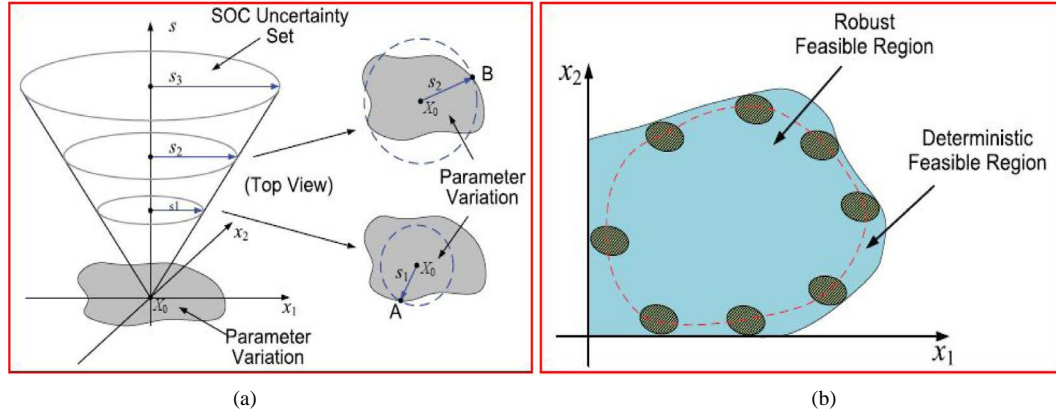


Figure 1. Basic Conceptual Explanation. (a) The 3D representation for 2D parameter variations; (b) Robust feasible region in robust optimization.

The parameter σ_l is a scale parameter (σ_l^2 is the variance of $x(l)$) and the function ρ is called the correlation function. Note that the scale parameters σ_l , $\sigma_{l'}$, and the correlation function ρ may be different for different grids.

A simple and natural model that allows for correlation between different locations is the exponential model. For this model the correlation function ρ decays exponentially as a function of the distance $h = \|l - l'\|$, *i.e.*

$$\rho(h) = e^{-\lambda_i h}, \quad \lambda_i \geq 0. \quad (1.12)$$

Note that as λ_i increases the correlation decays faster as a function of the distance. The exponential model is attractive because of its simplicity but it is not very flexible in capturing a wide range of correlation structures. Another popular and more flexible class of correlation functions is the Matern class [23], in which correlation function is parameterized by two parameters, θ_{1i} and θ_{2i} , and has the functional form:

$$\rho(h) = \frac{1}{2^{\theta_{2i}-1} \Gamma(\theta_{2i})} \left(\frac{2h\sqrt{\theta_{2i}}}{\theta_{1i}} \right)^{\theta_{2i}} \mathcal{K}_{\theta_{2i}} \left(\frac{2h\sqrt{\theta_{2i}}}{\theta_{1i}} \right), \quad (1.13)$$

where $\mathcal{K}_\alpha(\cdot)$ denotes the modified Bessel function of the second kind of order α , and $\Gamma(\cdot)$ denotes the Gamma function. According to Matern correlation function defined in (1.13), and assuming that parameter variation is truncated at its 3σ value, we perform random sampling and capture the furthest variation deviated from the nominal values. This distance will then be identified as the s_{\max} value at this particular design point X_0 . Having a set of simulation data pairs (X_0, s_{\max}) collected throughout the range of possible parameter values, we assume s_{\max} has a 1) linear $s_{\max} = \sum_{i=1}^n c_i x_i + \sum_{i=1}^{n-1} \sum_{j=i+1}^n d_{ij} x_i x_j + k$, and 2) quadratic

$s_{\max} = \sum_{i=1}^n c_i x_i^2 + \sum_{i=1}^n d_i x_i + \sum_{i=1}^{n-1} \sum_{j=i+1}^n e_{ij} x_i x_j + h$ relationship with the nominal values of gate sizes, and performed

nonlinear regression and linear regression, respectively. The fitting results show that linear fitting yields considerable approximation error compared with quadratic fitting. More importantly, the maximum approximation error of linear fitting indicates that linear assumption of s_{\max} function tends to yield overly optimistic estimation of parameter variations, *i.e.* to produce a smaller size of SOC estimation region than required. This result validates the necessity of quadratic fitting in SOC modeling. In addition, linear-form SOC model causes significant delay violations (up to 9%). On the contrary, because of its high approximation accuracy, the delay violation caused by quadratic-form model is as low as <1%, which demonstrates that the gate sizing results are robust to random parameter variations. To reduce the computation cost of fitting SOC set size, we assume that the fitting parameter A is diagonal, and parameter $b = 0$.

4. Uncertainty Budgeting with SOC Uncertainty Set

This section discusses how to conduct budgeting of uncertainty based on the SOC uncertainty set defined in

Section 3. We first explain the physical meaning underlying uncertainty budgeting for robust optimization. Then we provide a first-order approximation to associate yield protection level with the size of the SOC estimation set, which will be further incorporated in the optimization framework. By employing the yield-guaranteed SOC set the robust gate sizing problem can be finally formulated into a standard geometric program.

4.1. Feasible Region in Robust Design

We claim that it is necessary to distinguish the feasible region in deterministic gate sizing and that in robust gate sizing. In the deterministic case, if no parameter variations are considered, the backward mapping of timing constraints (as well as the bounding constraints) form a feasible region in design space, as shown in **Figure 1(b)** (denoted by the solid line). We define this region as deterministic feasible region:

$$\text{DFR} : \{X \mid d_j(X) \leq T_{\text{spec}}, X_{\min} \leq X \leq X_{\max}\}. \quad (1.14)$$

Any design point included in this region is a feasible design candidate in deterministic gate sizing. Now consider robust gate sizing under gate size variations (without budget of uncertainty), a design candidate is considered to be feasible in robust optimization only if all possible variations around it will be bounded by the deterministic feasible region. In this sense, some design candidates close to the boundary of deterministic feasible region will be identified as infeasible candidates as the uncertainty associated with them may exceed the deterministic. All points that are feasible in robust sense form a new region, which is defined as robust feasible region:

$$\text{RFR} : \{X_0 \mid d_j(X_0 + \delta X_0) \leq T_{\text{spec}}, X_{\min} \leq X_0 \leq X_{\max}\}. \quad (1.15)$$

As shown in **Figure 1(b)**, robust feasible region is a subset of deterministic feasible region, and is dependent on the variation range of gate size variations.

We further incorporate the chance constraint with yield protection level η (refer to (1.2)). In this case the robust feasible region becomes:

$$\text{RFR} : \{X_0 \mid \text{Prob}\{d_j(X_0 + \delta X_0) \leq T_{\text{spec}}\} \geq \eta\}. \quad (1.16)$$

Here for better interpretation the gate size bounding constraints ($X_{\min} \leq X_0 \leq X_{\max}$) is not shown. Obviously if we loosen the yield requirement, the robust feasible region will be changed accordingly. We will obtain a relatively larger robust feasible region for a smaller value of η , as some candidates identified as infeasible at higher protection level η become feasible at lower level (as shown in **Figure 2(a)**). However, as claimed previously, the calculation of probabilistic constraint is intractable as it requires an explicit probabilistic distribution and intensive computation cost. One possible solution is to associate the yield requirement with the size of SOC uncertainty set and conduct uncertainty budget accordingly. To be specific, if a relatively lower yield level is required, it is reasonable that we accordingly choose a relatively smaller size of uncertainty set to model gate size variations, considering that the resulting timing violation can be tolerated to some extent. In this manner we avoid intensive computation of probabilistic constraint, and do not need to change the optimization framework. The robust feasible region with uncertainty budgeting is therefore defined as:

$$\text{RFR} : \{X_0 \mid d_j(X_0, \mathcal{U}(X_0, \eta)) \leq T_{\text{spec}}\} \quad (1.17)$$

where $\mathcal{U}(X_0, \eta)$ is the SOC uncertainty set estimating the parameter variations, which is now dependent on not only the nominal values but also the yield requirement. If we are able to appropriately choose the size of the SOC set, the resulting robust feasible region in (1.17) could be a good approximation of the robust feasible region defined in (1.16). As shown in **Figure 2(b)**, by changing the size of SOC set in accordance with yield level η , we are able to obtain a similar robust feasible region as in stochastic optimization and therefore close gate sizing results compared with stochastic optimization. Apparently the key question here is how to establish an efficient mapping relationship between yield protection level η and the size of SOC uncertainty set.

4.2. Yield-Guaranteed Uncertainty Set

With consideration of budget of uncertainty, we rewrite the SOC set for parameter variations as follows:

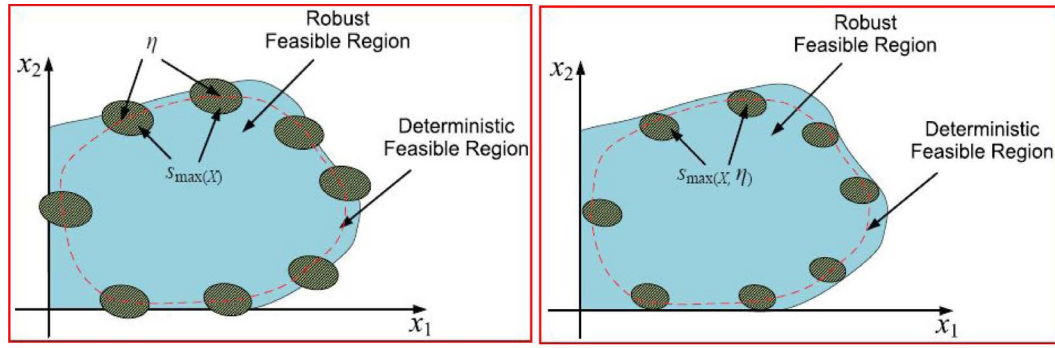


Figure 2. Robust Feasible Region with and without Budget of Uncertainty. (a) Robust feasible region at yield protection level η ; (b) Robust feasible region with budget of uncertainty.

$$\|A\delta X(\eta) + b\|_2 \leq s_{\max}(X)\Omega(\eta) \quad (1.18)$$

where $\Omega(\eta)$ is a scaling factor of the SOC set size for a specific yield protection level. We assume parameter variations will be enclosed by this scaled SOC set. Note that the parameter variations defined here is dependent of η , as a result we use $\delta X(\eta)$ to differentiate it from the physical parameter variations δX . For simplicity we let $b = 0$ in this model. Assume that the physical parameter variations obey a multivariate Gaussian distribution $\delta X \sim N(\mu, P)$ where P denotes the covariance matrix. We can derive that the uncertainty defined by the scaled SOC set, *i.e.* $\delta X(\eta)$ also follows a scaled Gaussian distribution:

$$\delta X(\eta) \sim N(\Omega\mu, \Omega^2 P) \quad (1.19)$$

We now discuss how to approximate the scaling factor Ω when applying the SOC uncertainty set to the timing constraint. Applying a first-order Taylor series expansion to the probabilistic delay function yields:

$$\text{Prob}\{d_j(X_0 + \delta X(\eta)) \leq T_{\text{spec}}\} = \text{Prob}\left\{d_j(X_0) + \sum_{i=1}^n \underbrace{\left(\frac{\partial d_j}{\partial x_i}\right)}_{g_i(x)} \bigg|_{x_0} \delta x_i(\eta) \leq T_{\text{spec}}\right\} \geq \eta. \quad (1.20)$$

By substituting (1.19) into (1.20), it is possible to approximate the probabilistic constraint by a Gaussian CDF (Cumulative Distribution Function) and reveal the mapping relationship between η and Ω . We start with analyzing the independent case. If the design parameters are all uncorrelated, since $\delta x_i(\eta) \sim N(\Omega\mu_i, \Omega\sigma_i)$, following probability theory we can derive that delay metric obeys the following Gaussian distribution:

$$d_j = d_j(X_0) + \sum_{i=1}^n g_i(x) \delta x_i(\eta) \sim N\left(\underbrace{d_j(X_0) + \left(\sum_i g_i(X)\right)\Omega\mu_i}_{\mu_{d_j}}, \underbrace{\left(\sum_i g_i(X)\right)\Omega\sigma_i}_{\sigma_{d_j}}\right). \quad (1.21)$$

Therefore the probabilistic constraint function can be approximated as:

$$\text{Prob}\{d_j \leq T_{\text{spec}}\} = \text{Prob}\left\{\frac{d_j - \mu_{d_j}}{\sigma_{d_j}} \leq \frac{T_{\text{spec}} - \mu_{d_j}}{\sigma_{d_j}}\right\} = \Phi\left(\frac{T_{\text{spec}} - \mu_{d_j}}{\sigma_{d_j}}\right) \geq \eta \quad (1.22)$$

where $\Phi(\cdot)$ is the cumulative distribution function for a standard Gaussian variable. Therefore, for a required level of yield protection, we can refer to Gaussian distribution table to find $\Phi^{-1}\left(\frac{T_{\text{spec}} - \mu_{d_j}}{\sigma_{d_j}}\right)$ and further calculate the scaling factor Ω .

For a specific yield level η , we use the method described above to conduct uncertainty budgeting and obtain the optimal gate sizes satisfying yield requirement η . Based on the gate sizing results we run Monte-Carlo simulation to determine the frequency of delay violations, *i.e.* the percentage that circuit delay exceeds the timing constraint T_{spec} , and compare the violation rate by uncertainty budgeting with the expected violation rate for specified η value. The results demonstrate good accuracy of the approximation method used in budget of uncertainty.

We focus on formulating the set of constraint functions $d_j(X_0 + \delta X)$. For small parameter variations from their nominal values, the variational constraint function $d_j(X_0 + \delta X)$ can be approximated by a first-order Taylor series expansion:

$$d_j(X_0 + \delta X) = d_j(X_0) + \nabla d_j(X_0) \cdot (X + \delta X - X_0) + \sum_{i=1}^n \left(\frac{\partial d_j}{\partial x_i} \right) \bigg|_{x_{i0}} \delta x_i \quad (1.23)$$

where $\nabla d_j(X_0)$ represents the gradient of delay function d_j calculated at the nominal values of gate sizes, and δX denotes the random variations around nominal gate sizes x_{i0} 's.

From (1.23) we observe that the variational function $d_j(X_0 + \delta X)$ consists of two components: 1) the deterministic part $d_j(X_0)$, which is in signomial form; and 2) the variational part $\sum_{i=1}^n \left(\frac{\partial d_j}{\partial x_i} \right) \bigg|_{x_{i0}} \delta x_i$, consisting of a gradient term and a parameter variation term. On the other hand, all possible perturbation values in the parameter variation term are required to satisfy the timing constraint T_{spec} . In other words, the complete variational function (1.23) has to be smaller than this user-defined delay specification. This is equivalent to:

$$d_j(X_0) + \max_{\forall \delta X} \left\{ \sum_{i=1}^n \left(\frac{\partial d_j}{\partial x_i} \right) \bigg|_{x_{i0}} \delta x_i \right\} \leq T_{\text{spec}}. \quad (1.24)$$

which indicates that the maximum possible value of the variational function must be bounded by timing constraint T_{spec} . In what follows, the variational delay constraint is modeled as the deterministic constraint (1.24).

After one step of transformation, the constraint function is still not in standard GP form, and further transformations are necessary for GP formulation. We show that by employing the SOC estimation model and introducing a set of slack variables, the variational constraint function can be eventually transformed into a set of standard posynomials. The formulation procedure is applicable to delay models in form of any signomial. Posynomial delay models can be certainly addressed in the same manner since a posynomial is a special case of a signomial.

We employ the SOC representation, which is described in Section 3, to address the parameter variation term δX . Given a gate size vector $X \in R^n$ with nominal vector X_0 , parameter variations around the nominal values are characterized by a SOC estimation model:

$$\|AX + b\|_2 \leq \underbrace{\sum_{i=1}^n c_i x_i^2 + \sum_{i=1}^n d_i x_i + \sum_{i=1}^{n-1} \sum_{j=i+1}^n e_{ij} x_i x_j + h}_{S_{\text{max}}(X)} \quad (1.25)$$

where S_{max} is an auxiliary parameter introduced to manipulate parameter perturbation range. The variations are considered to be bounded within the SOC region defined in (1.25), and the boundary condition S_{max} determines the size of the SOC region. Note that S_{max} itself is dependent on the nominal value of design parameters. As shown in (1.25), S_{max} is a conic function of the nominal gate sizes. In addition to the linear terms of design parameters, it also includes a set of quadratic terms for the purpose of capturing the nonlinearity of the SOC size, as well as a set of cross terms for the purpose of capturing the correlations among design parameters. We have applied both linear regression and nonlinear regression techniques to fit the form of S_{max} function (refer to the section of experimental results). The fitting results show that the assumption of conic-form S_{max} function yields much less fitting errors and achieves good approximation accuracy.

We will show that by employing the conic-form SOC estimation model and introducing a set of slack variables, the variational constraint function can be eventually transformed into a set of standard posynomials. The formulation procedure is applicable to delay models in form of any signomial. Posynomial delay models can be certainly addressed in the same manner since a posynomial is a special case of a signomial. The robust gate sizing problem is generalized as follows:

$$\begin{aligned} \text{minimize : Area} &= \sum_{i=1}^n \alpha_i x_i \\ \text{subject to : } d_j(x) + \max_{\forall \delta X} \left\{ \sum_{i=1}^n \left(\frac{\partial d_j}{\partial x_i} \right) \delta x_i \right\} &\leq T_{\text{spec}} \end{aligned} \quad (1.26)$$

$$\|AX + b\|_2 \leq S_{\max}(X) \quad (1.27)$$

$$X_{\min} \leq X \leq X_{\max}$$

$$\text{variables : } X, s_1, s_2, z_1, z_2$$

The objective is already a posynomial and satisfies standard GP requirement. There are two constraints which are not in standard GP form, a robust delay constraint and the conic-form SOC constraint for uncertainty estimation. As described above, the conic-form SOC constraint (1.27) can be translated into a general-form SOC interpretation, and therefore can be accurately approximated by a set of linear constraints [24]. Further GP formulation are required. We will focus on formulating the delay constraint (1.26). We rewrite the delay function as follows:

$$d_j(X) = \sum_{k=1}^K c_k \cdot \prod_{l=1}^n x_l^{a_{lk}}. \quad (1.28)$$

where c_k and a_{lk} can be any real number. The derivative of delay function at x_i is then given by:

$$\frac{\partial d_j}{\partial x_i} = \sum_{k=1}^K a_{ik} c_k \cdot \prod_{l \neq i} x_l^{a_{lk}} \cdot x_i^{a_{ik}-1}. \quad (1.29)$$

By combining the results in (1.28) and (1.29) we can express the constraint function (1.24) explicitly:

$$\sum_{k=1}^K c_k \prod_{l=1}^n x_{l_0}^{a_{lk}} + \max_{\forall \delta X} \left\{ \sum_{i=1}^n \left(\sum_{k=1}^K a_{ik} c_k \prod_{l \neq i} x_{l_0}^{a_{lk}} x_{i_0}^{a_{ik}-1} \right) \cdot \delta x_i \right\} \leq T_{\text{spec}} \quad (1.30)$$

where x_{i_0} 's represent nominal gate sizes, and δx_i 's the corresponding size variations. For conciseness we do the following substitution for (1.30):

$$g_{ik}(X) = a_{ik} c_k \prod_{l \neq i} x_{l_0}^{a_{lk}} x_{i_0}^{a_{ik}-1}.$$

In above equation, c_k stands for the multiplicative coefficient and a_{ik} stands for the exponent index in posynomial delay function (1.28), therefore $g_{ik}(X)$ could be either positive or negative, bringing the difficulty in GP formulation since a standard posynomial does not allow negative coefficients. To address this problem, We further introduce two vectors $\Phi_+, \Phi_- \in R^n$ to collect the positive and negative coefficients in (1.30) respectively. To be more specific, the components of vectors Φ_+ and Φ_- are generalized as follows:

$$\begin{cases} \phi_{+,i} = \sum_p g_{ip}(X) & \text{for } \forall a_{ip} > 0, i = 1, 2, \dots, n \\ \phi_{-,i} = \sum_q g_{iq}(X) & \text{for } \forall a_{iq} < 0, i = 1, 2, \dots, n \end{cases} \quad (1.31)$$

Having explained the definition of Φ_+, Φ_- in (1.31), we further translate (1.30) into the following expression:

$$\sum_{k=1}^K c_k \prod_{l=1}^n x_{l_0}^{a_{lk}} + \max_{\forall \delta X} \left\{ \sum_{i=1}^n \left(\sum_{k=1}^K g_{ik}(X) \right) \cdot \delta x_i \right\} = \sum_{k=1}^K c_k \prod_{l=1}^n x_{l_0}^{a_{lk}} + \max_{\forall \delta X} \{ \langle \Phi_+, \delta X \rangle + \langle \Phi_-, \delta X \rangle \} \leq T_{\text{spec}} \quad (1.32)$$

where $\langle a, b \rangle$ denotes the inner product of two vectors a and b . Following the well-known Cauchy-Schwarz inequality:

$$\langle a, b \rangle \leq \|a\|_2 \cdot \|b\|_2, \quad (1.33)$$

an equivalent expression for (1.33) is given by:

$$\sum_{k=1}^K c_k \prod_{l=1}^n x_{l_0}^{a_{lk}} + \|\Phi_+\|_2 \cdot \|\delta X\|_2 + \|\Phi_-\|_2 \cdot \|\delta X\|_2 \leq T_{\text{spec}}. \quad (1.34)$$

By employing the SOC estimation model and following norm properties, gate size variations can be estimated as:

$$\|\delta X\|_2 \leq \frac{1}{\|A\|_2} (S_{\max}(X) - \|b\|_2) \quad (1.35)$$

Substituting (1.35) into (1.34) yields the following constraint:

$$d(X) + \frac{\|\Phi_+\|_2 + \|\Phi_-\|_2}{\|A\|_2} (S_{\max}(X) - \|b\|_2) \leq T_{\text{spec}}. \quad (1.36)$$

One more step of formulation is to introduce two more slack variables r_1 and r_2 to substitute Φ_+ and Φ_- :

$$\begin{aligned} r_1 &= \|\Phi_+\|_2 \Leftrightarrow r_1^2 = \Phi_+^T \Phi_+ \\ r_2 &= \|\Phi_-\|_2 \Leftrightarrow r_2^2 = \Phi_-^T \Phi_- \end{aligned} \quad (1.37)$$

Putting all the formulation results together, we conclude that the variational constraint function (1.24) has been replaced by an equivalent set of constraints:

$$\sum_{k=1}^K c_k \prod_{l=1}^n x_{l_0}^{a_{lk}} + \frac{r_1 + r_2}{\|A\|_2} (S_{\max} - \|b\|_2) \leq T_{\text{spec}} \quad (1.38)$$

$$\Phi_1^T \Phi_1 r_1^{-2} \leq 1 \quad (1.39)$$

$$\Phi_2^T \Phi_2 r_2^{-2} \leq 1 \quad (1.40)$$

which is very close to a standard GP expression with the new decision variable set: (X, r_1, r_2) . The quadratic terms in constraints (1.39) and (1.40) are already in standard posynomial form by expanding them:

$$\Phi_1^T \Phi_1 = \sum_{i,j} \phi_{1,i} \phi_{1,j}, \quad \Phi_2^T \Phi_2 = \sum_{i,j} \phi_{2,i} \phi_{2,j}.$$

Above expansion indicates that the quadratic terms both are summations of posynomials with all positive multiplicative coefficients, therefore the constraints (1.39) and (1.40) are also posynomials and they satisfy the requirements of GP formulation.

The last step is to transform the signomial constraints into posynomial constraints. [25] introduces an efficient way of such conversion. After such transformation, the final formulated GP can be efficiently solved by existing GP tools. In real application, this formulation procedure is repeated for all delay constraints, and the final formulated GP problem can be solved by convex optimization tools. It is worth emphasizing that if we take uncertainty budgeting into account, the formation of s_{\max} will be dependent on not only the conic-form fitting function, but also the yield-determined size of the SOC uncertainty set.

5. Experimental Results

In this section we present the robust gate sizing results on ISCAS benchmark circuit. All simulations and experiments were performed on a quad-core 2.8-GHz machine with 4-GB memory. In simulation part, we use the 65nm technology node provided by PTM model [26]. The coefficients in gate delay functions are extracted from HSPICE simulation data. We assume 20% process variations for all gate sizes around their nominal values. An convex optimization software GPPLAB [27] was used to solve the final GP problem. The optimization

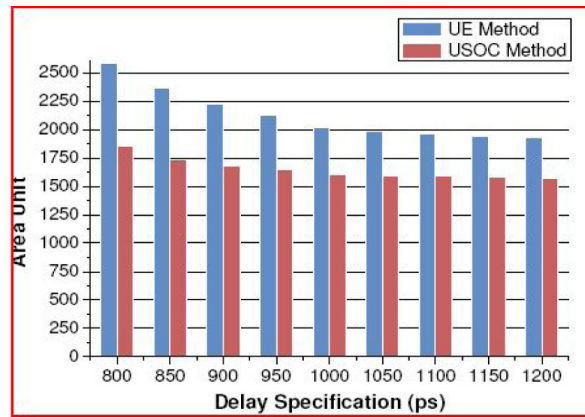


Figure 3. Area costs for C432 circuit with different delay specifications UE means Uncertainty Ellipsoidal USOC refers to the new method.

objective is to minimize the total area $\sum_i \alpha_i x_i$, where α_i denotes the number of transistors in gate i , and gate size x_i stands for the ratio of area of gate i to that of a minimum sized inverter. **Figure 3** demonstrates this experimental result. We compared delay specification and area consumption of uncertainty ellipsoidal (UE) and our proposed method USOC. It can be noticed that with the same delay specification, we have 20% of reduction in area consumption.

6. Conclusion

This paper presents a novel uncertainty estimation model for robust gate sizing under process variations. The new model employs the concept of SOC to accurately characterize local variations around nominal gate sizes. With gate size variations characterized in SOC estimation, the robust gate sizing problem can be formulated into a standard geometric program, and therefore can be efficiently solved by existing GP solvers.

References

- [1] Boning, D. and Nassif, S. (2001) Models of Process Variations in Device and Interconnect. In Chandrakasan, A., Bowhill, W.J. and Cox, F., Eds., *Design of High-Performance Microprocessor Circuits*, Chapter 6, IEEE Press, 98-115.
- [2] Roy, S. and Asenov, A. (2005) Where Do the Dopants Go? *Science*, **309**, 388-390.
- [3] Orshansky, M., Milor, L. and Hu, C. (2004) Characterization of Spatial Intrafield Gate CD Variability, Its Impact on Circuit Performance, and Spatial Mask-Level Correction. *IEEE Transactions on Semiconductor Manufacturing*, **17**, 2-11. <http://dx.doi.org/10.1109/TSM.2003.822735>
- [4] Hargreaves, B., Hult, H. and Reda, S. (2008) Within-Die Process Variations: How Accurately Can They Be Statistically Modeled? *Proceedings of ASPDAC*, Seoul, 21-24 March 2008, 524-530.
- [5] Veetil, V., Sylvester, D., Blaauw, D., Shah, S. and Rochel, S. (2009) Efficient Smart Sampling Based Full-Chip Leakage Analysis for Intra-Die Variation Considering State Dependence. *Proceedings of DAC*, San Francisco, 26-31 July 2009, 154-159.
- [6] Wang, J., Das, D. and Zhou, H. (2007) Gate Sizing by Lagrangian Relaxation Revisited. *Proceedings of ICCAD*, 111-118.
- [7] Ketkar, M., Kasamsetty, K. and Saptnekar, S. (2000) Convex Delay Models for Transistor Sizing. *Proceedings of DAC*, 655-660.
- [8] Kasamsetty, K., Ketkar, M. and Saptnekar, S. (2000) A New Class of Convex Functions for Delay Modeling and Its Application to the Transistor Sizing Problem. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **19**, 779-788. <http://dx.doi.org/10.1109/43.851993>
- [9] Shyu, J.M., Sangiovanni-Vincentelli, A., Fishburn, J.P. and Dunlop, A.E. (1988) Optimization-Based Transistor Sizing. *IEEE Journal of Solid-State Circuits*, **23**, 400-409. <http://dx.doi.org/10.1109/4.1000>
- [10] Cong, J., Lee, J. and Vandenbergh, L. (2008) Gate Sizing by Lagrangian Relaxation Revisited. *Proceedings of International Symposium on Physical Design (ISPD)*, 10-14.

- [11] Singh, J., Nookala, V., Luo, Z. and Sapatnekar, S. (2011) A Geometric Programming-Based Worst Case Gate Sizing Method Incorporating Spatial Correlation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **53**, 464-501.
- [12] Li, X., Gopalakrishnan, P., Xu, Y. and Pileggi, L. (2007) Robust Analog/RF Circuit Design with Projection-Based Performance Modeling. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **26**, 2-15. <http://dx.doi.org/10.1109/TCAD.2006.882513>
- [13] Hsiung, K.L., Kim, S.J. and Boyd, S. (2008) Tractable Approximate Robust Geometric Programming. *Optimization and Engineering*, **9**, 95-118. <http://dx.doi.org/10.1007/s11081-007-9025-z>
- [14] Xu, Y., Hsiung, K.L., Li, X., Pileggi, L.T. and Boyd, S.P. (2009) Regular Analog/RF Integrated Circuits Design Using Optimization with Recourse Including Ellipsoidal Uncertainty. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **28**, 623-637. <http://dx.doi.org/10.1109/TCAD.2009.2013996>
- [15] Bertsimas, D., Brown, D.B. and Caramanis, C. (2008) Theory and Applications of Robust Optimization. *SIAM Review*, **27**, 295-308.
- [16] Dyer, M. and Stougie, L. (2006) Computational Complexity of Stochastic Programming Problems. *Mathematical Programming: Series A and B*, **106**, 423-432. <http://dx.doi.org/10.1007/s10107-005-0597-0>
- [17] Xu, Y., Hsiung, K.L. and Li, X. (2005) Opera: Optimization with Ellipsoidal Uncertainty for Robust Analog IC Design. *Proceedings of Design Automation Conference*, Anaheim, 13-17 June 2005, 632-637.
- [18] Johnson, R.A. and Wichern, D.W. (2002) Applied Multivariate Statistical Analysis. Prentice Hall, Upper Saddle River.
- [19] Boyd, S. and Vandenberghe, L. (2004) Convex Optimization. Cambridge University Press, New York.
- [20] Lobo, M., Vandenberghe, L., Boyd, S. and Lebret, H. (1998) Applications of Second-Order Cone Programming. *Linear Algebra and Its Applications*, **284**, 193-228. [http://dx.doi.org/10.1016/S0024-3795\(98\)10032-0](http://dx.doi.org/10.1016/S0024-3795(98)10032-0)
- [21] Xiong, J., Zolotov, V. and He, L. (2006) Robust Extraction of Spatial Correlation. *Proceedings of International Symposium on Physical Design*, San Jose, 9-12 April 2006, 2-9.
- [22] Chang, H. and Sapatnekar, S. (2003) Statistical Timing Analysis Considering Spatial Correlation Using a Single Pert-Like Traversal. *International Conference on Computer Aided Design, ICCAD-2003*, 9-13 November 2003, 621-625.
- [23] Stein, M.L. (1999) Interpolation of Spatial Data. Springer, New York. <http://dx.doi.org/10.1007/978-1-4612-1494-6>
- [24] Ben-Tal, A. and Nemirovski, A. (2000) Robust Solutions of Linear Programming Problems Contaminated with Uncertain Data. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **88**, 411-424.
- [25] Chiang, M. (2005) Geometric Programming for Communication Systems. Now Publishers, Hanover.
- [26] Nanoscale Integration and Modeling (NIMO) Group (2011) Predictive Technology Model (ptm). <http://ptm.asu.edu>
- [27] Boyd, S.P. (2011) Stephen p. Boyd—Software. Website, August. <http://stanford.edu/~boyd/software.html>

Scientific Research Publishing (SCIRP) is one of the largest Open Access journal publishers. It is currently publishing more than 200 open access, online, peer-reviewed journals covering a wide range of academic disciplines. SCIRP serves the worldwide academic communities and contributes to the progress and application of science with its publication.

Other selected journals from SCIRP are listed as below. Submit your manuscript to us via either submit@scirp.org or [Online Submission Portal](#).

