Open Access Library Journal
2019, Volume 6, e5689
ISSN Online: 2333-9721
ISSN Print: 2333-9705

Design and Implementation of a New Multilevel Inverter Employing Reduced Components

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How to cite this paper: Feloups, C.E.S. and Mohamed, E.E.M. (2019) Design and Implementation of a New Multilevel Inverter Employing Reduced Components. *Open Access Library Journal*, **6**: e5689.
https://doi.org/10.4236/oalib.1105689

Received: August 9, 2019
Accepted: September 17, 2019
Published: September 20, 2019

Abstract

This paper focuses on an implementation of new topology which can synthesize multi-level output voltage at the load terminals. The proposed inverter consists of two main parts; level generation part and polarity generation part. Level generation part is responsible for generating voltage levels at its end while; polarity generation part is a traditional H-bridge which is used to provide inversion of the output voltage levels. Single-phase seven-level inverter has been presented from the proposed multilevel inverter. This topology offers reduced number of switching components compared with many recent available topologies particularly for high number of levels. Due to the multi-level output voltage, low total harmonic distortion (THD), less circuit complexity, less cost and high efficiency can be obtained. A conventional PI controller is used for load voltage regulation to obtain output voltage near to sinusoidal. Computer-aided using the dSPACE_CP1103 controller and experimental setup are carried out to provide the validity and effectiveness of the proposed inverter.

Subject Areas

Electric Engineering

Keywords

Efficiency, Multilevel Inverter (MLI), Seven-Level, Single-Phase, Total Harmonic Distortion (THD), Voltage Control

1. Introduction

Through the last decade, the progress of power electronics along with the regular cost reduction, reliability, power capability and high efficiency, has made it the most alerting for researchers' attention [1]. This progress has made the ability to

develop voltage source inverters (VSI) which can control voltage and frequency simultaneously, therefore they are considered the best solution for many applications. The conventional three-level H-bridge inverter circuit is the first generation of inverter topologies [2] [3]. As many applications require high efficiency with fewer harmonic contents, a demand for the higher voltage rating multilevel inverter (MLI) has evolved.

One of the leading advances for MLIs is the improvement in power electronics which have been used to fulfill the requirements for many applications for low/medium voltage electrical utility [4]. MLI is a good solution for improving the performance of many industrial applications such as renewable energy systems [5], motor drives [6], uninterruptable power supplies (UPS), flexible AC transmission systems (FACTS) [7], etc. Another advantage of MLI is discarding the need for a step-up transformer which is needed in high voltage applications that reduces the overall cost and size of the inverter circuits [8].

A high number of the stepped output voltage from MLI leads to the output voltage shape to be close to a sinusoidal waveform. This leads to the high quality in output voltage with good total harmonic distortion (THD), low dv/dt stress in addition to the reduction in output filter size [9]. They are promising as they become more attractive due to their inherent merits as it becomes cheaper, lighter, and compact. Mainly, popular topologies of MLIs are categorized into 1) diode-clamped MLI (DCMLI) which was proposed by Nabae *et al.* [10], 2) flying capacitor MLI (FCMLI) which was introduced by Meynard and Foch [11] and 3) cascaded H-bridge MLI (CHBMLI) [12] [13].

DCMLI has two advantages over conventional H-bridge inverter; the higher voltage capability and a reduced harmonic content. However, it suffers from the unbalance of voltage in the DC-link capacitors, on the other hand, it requires a large number of clamping diodes, which increases the complexity with higher voltage levels [14] [15]. FCMLI has lesser number of required DC voltage sources [16] however, it has two main problems; it requires a large number of capacitors in addition to the difficulty to achieve the capacitor voltage balance [17] [18]. In order to overcome the limitations of DCMLI and FCMLI, CHBMLI has been presented.

CHBMLI consists of several H-bridge inverters with separate DC voltage sources. It has two structures, namely the symmetric and the asymmetric CHBMLI [19] [20]. In symmetric CHBMLI, all the separated DC voltage sources have the same magnitudes. However, it utilizes a large number of power switches in addition to gate drive circuits to obtain a large number of levels, which increases the cost of the overall circuit. A lesser number of power switches had been used in the asymmetric structure, on the other hand, it suffers from voltage stress in most of the power switches and voltage sources [21]. The main challenging issue is to obtain a high number of levels with lesser voltage stress, fewer power switches in addition to lesser DC voltage sources. Recently, many topologies have been recommended as a replacement for CHBMLI.

In order to generate more number of levels, many researchers have presented

many developed topologies. Each one of these topologies has merits and demerits due to the number of used components such as power switches and DC voltage sources, power losses and voltage stress on the switches. Using a large number of power switches, gate drive circuits in [22] leads to increased circuit size and manufacturing costs. By using the bidirectional switches to obtain more number of levels, the number of power switches and drive circuits in [23] is reduced. However, a large number of components conduct in each mode which may lead to high power loss. In [24] a single phase seven-level inverter has been proposed by using only seven power switches in addition to two power diode. However, this topology uses a large number of components.

The modular multilevel inverter (MMLI) has been proposed in [25]. To generate higher levels by this topology, three components (one DC source and two power switches) are added which increases the number of components. In order to overcome the aforementioned issues, a new multilevel inverter has been presented in this paper. The proposed topology has an optimum number of power components and hence fewer gate drive circuits in addition to less circuit layout complexity for a high number of levels compared with other topologies mentioned in [22] [23] [24] [25].

2. Proposed Single-Phase Multilevel Inverter

Figure 1 shows a modified structure for the proposed single-phase MLI which reduces the overall circuit by one power switch compared with the proposed circuits in [26] [27]. The proposed MLI comprises of "n" segments each segment is composed of a DC voltage source in series with one power switch without fast recovery diode. Only the first segment has one DC voltage source, with value of V_1, and one power switch, S_1, with a fast recovery diode where diode is used to generate the first level, in contrast, the power switch is used to provide a freewheeling path for inductive loads.

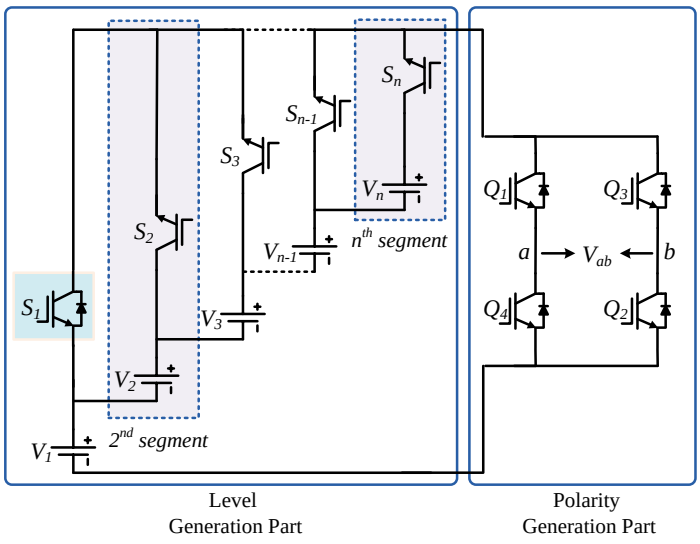


Figure 1. Proposed modular multilevel inverter.

For the proposed MLI, the relation between the number of symmetric *DC* voltage sources, N_{DC}, and the number of power switches, N_{Sw} based on the maximum number of levels, N_{levels}, and are calculated as follows:

$$N_{DC} = \frac{N_{\text{levels}} - 1}{2} \tag{1}$$

$$N_{Sw} = \frac{N_{\text{levels}} - 1}{2} + 4 \tag{2}$$

The device rating of the power switch in any topology must be selected carefully. This is because most of the power switches may block different voltage. Maximum blocked voltage is the most important parameter and must be taken into account in construction of any MLI topology as the cost of MLI based on this value. *MBV* is calculated by summing the blocked voltage across each power switches. The blocked voltage of power switches in level and generation parts in addition, *MBV* values are calculated as follow:

$$Vb_{S1} = Vb_{S2} = Vb_{S3} = \cdots = Vb_{Sn} = V_{DC} \tag{3}$$

$$Vb_{Q1} = Vb_{Q2} = Vb_{Q3} = Vb_{Q4} = n * V_{DC} \tag{4}$$

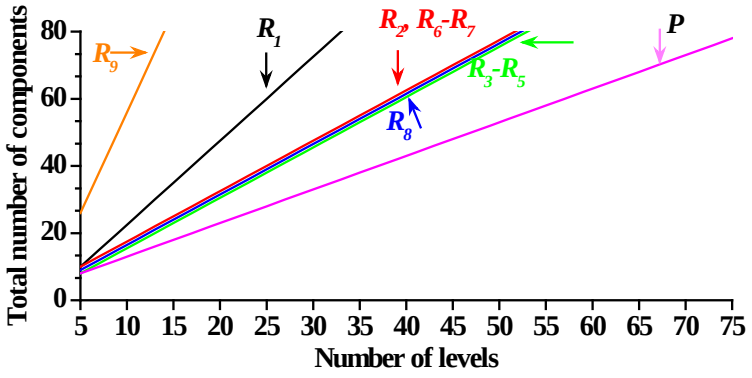
$$MBV = 5n * V_{DC} \tag{5}$$

DC voltage sources in level generation part can be replaced with series-connected capacitors supplied from single *DC* voltage source where the *DC* source can be adopted by some applications such as photovoltaic system. However, the voltage across the capacitors will deviate during the switching process at generating levels. Therefore, it is necessary to balance the voltage across the capacitors.

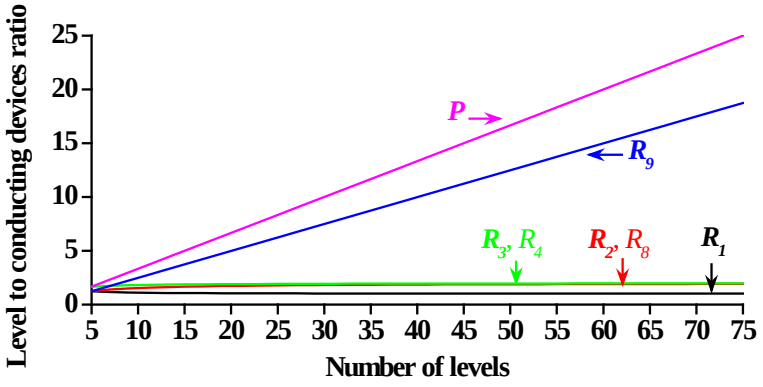
To strengthen the powerful merit of the proposed topology, several comparisons have been presented to verify the merits and demerits of the proposed MMLI. Several topologies of MMLI have been presented in the past few years which have the ability to provide symmetrical and asymmetrical operation. To make the comparisons fair and rational, all topologies used in the comparisons are used in its symmetrical operation. The proposed inverter for simplicity in comparisons is mentioned as "P". CHB-MLI is presented in [28]. This topology is considered for comparisons by "R_1". Another topology is presented in [22] which offers symmetry and asymmetry from its structure is described in "R_2". "R_3" describe an MLI presented in [28] based on switched DC sources which can offer asymmetry operation. Several topologies are presented in [25] [29] [30] [31] [32] which offer modularity with low number of components are described by "R_4"-"R_8". A high number of components topology is presented in [33] which is described by "R_9".

The main aim of introducing new topology is the increment in number of levels using lower number of components. As the number of components increased, the switching losses, size, and cost will increase. The comparisons between different topologies must be made in the requirements of switching de-

vices to present switching losses and in the total number of components to present overall cost of the presented topology for a given number of levels. In addition, the maximum blocked voltage by the power switches must be taken into account as it provides the overall cost of the presented topology. Figure 2(a) presents the comparison between the proposed topology "P" and most recent topologies. As shown, the proposed inverter presents lower number of components for introducing higher number of levels. Another important term in introducing any topology is the number of conducting devices for generating given number of levels. Level to conducting devices ratio (LCD) means the number of conducing devices including power switches and diodes are included for a given number of levels. This ratio provides amount of losses based on number of conducting devices. High LCD ratio means low number of conducting devices along with low switching losses and high efficiency the topology will offer at higher number of levels. Figure 2(b) displays LCD ratio comparison with different topologies. As seen, the proposed inverter offers better values of LCD ratio compared with other presented topologies as only three devices conduct at any level. While, as shown in Figure 2(c), "R_1" and "R_3" offer lower value of blocked voltage compared with the proposed topology and "R_4". However, the proposed topology still offers better value compared with other topologies.



(a)



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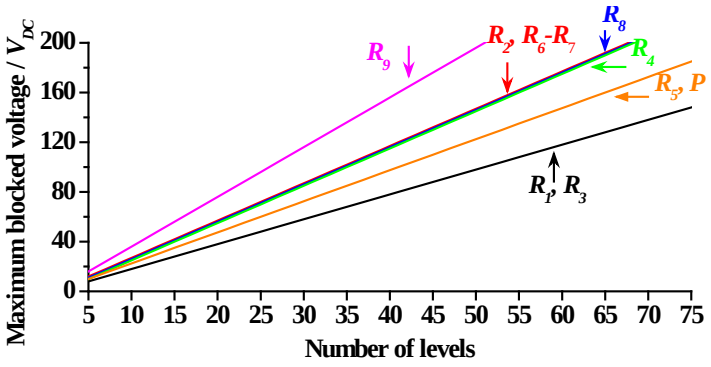


(c)

Figure 2. Comparison between the proposed topology with other topologies.

3. Single-Phase Seven-Level Inverter

3.1. Configuration

The structure of the proposed single-phase seven-level PWM inverter is indicated in Figure 1. This topology comprises three symmetrical DC voltage sources and seven power switches. The inverter output voltage will have seven state *i.e.* $3V_{dc}$, $2V_{dc}$, V_{dc}, 0, $-V_{dc}$, $-2V_{dc}$, and $-3V_{dc}$. It consists of two parts; the polarity generation part which is a conventional H-bridge inverter and the level generation part. As shown in this figure the switches Q_1, Q_2, Q_3, Q_4 and S_1 should be power switches with an antiparallel diode to provide the path for load current, however, power switches S_2 and S_3 should be without anti-parallel diode to avoid the short circuit problem between DC voltage sources. As the power switches are not ideal so dead-time has been taken into account. The main function of the polarity generation part is to obtain the zero state on the AC load voltage while, the main purpose of the level generation part is to obtain different output voltage levels.

3.2. Generation of Levels

In order to achieve a balanced output voltage levels, the DC voltage sources in each segment must be symmetrical ($V_1 = V_2 = V_3 = V_{dc}$). As the load is bi-directional, the output voltage from the proposed inverter has ten states as illustrated in Table 1. The output voltage levels according to the ON state condition are indicated in Figure 3.

4. Switching Algorithm

The switching pattern for the proposed seven-level PWM inverter is generated by comparing a rectified sinusoidal reference signal (*i.e.* V_{ref}) with three in-phase triangle carrier signals (*i.e.* V_{car1}, V_{car2}, and V_{car3}) having same switching frequency, same peak value but different in offset voltage which is the level shifted PWM (LSPWM) methodology as shown in Figure 4. The intersection between V_{ref} and V_{car1} occurs with a modulation index (MI), as calculated

Table 1. Switching states.

State	Output voltage (V_{ab})	Direction of output current (I_{out})	Switches in ON states
1)	$3V_{dc}$	Positive	S_3, Q_1, Q_2
2)	$2V_{dc}$	Positive	S_2, Q_1, Q_2
3)	V_{dc}	Positive	D_{S1}, Q_1, Q_2
4)	V_{dc}	Negative	S_1, D_{Q1}, D_{Q2}
5)	0	Positive	Q_1, D_{Q3} or Q_2, D_{Q4}
6)	0	Negative	Q_3, D_{Q1} or Q_4, D_{Q2}
7)	$-V_{dc}$	Positive	S_1, D_{Q3}, D_{Q4}
8)	$-V_{dc}$	Negative	D_{S1}, Q_3, Q_4
9)	$-2V_{dc}$	Negative	S_2, Q_3, Q_4
10)	$-3V_{dc}$	Negative	S_3, Q_3, Q_4

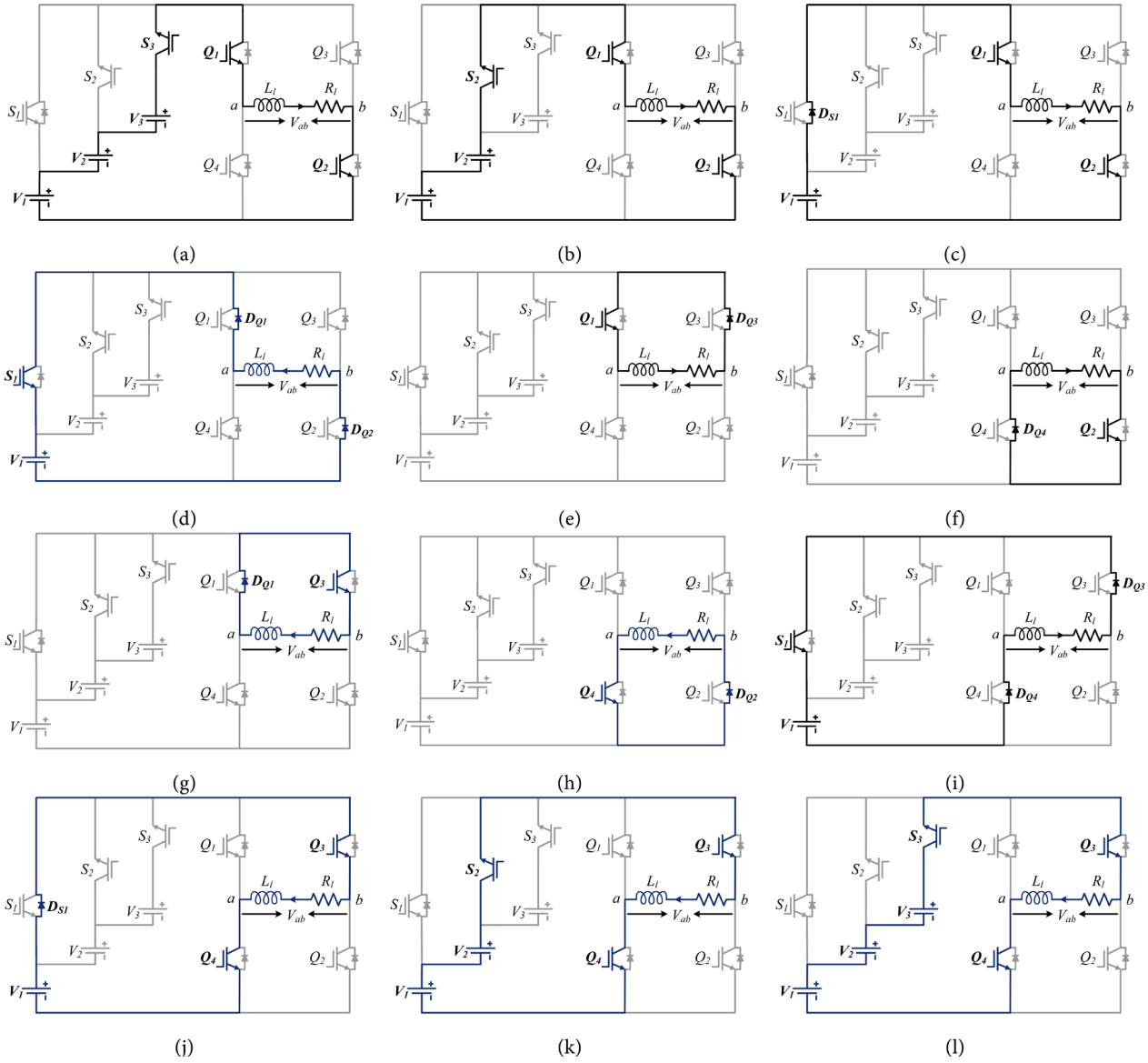


Figure 3. Generation of output voltage levels.

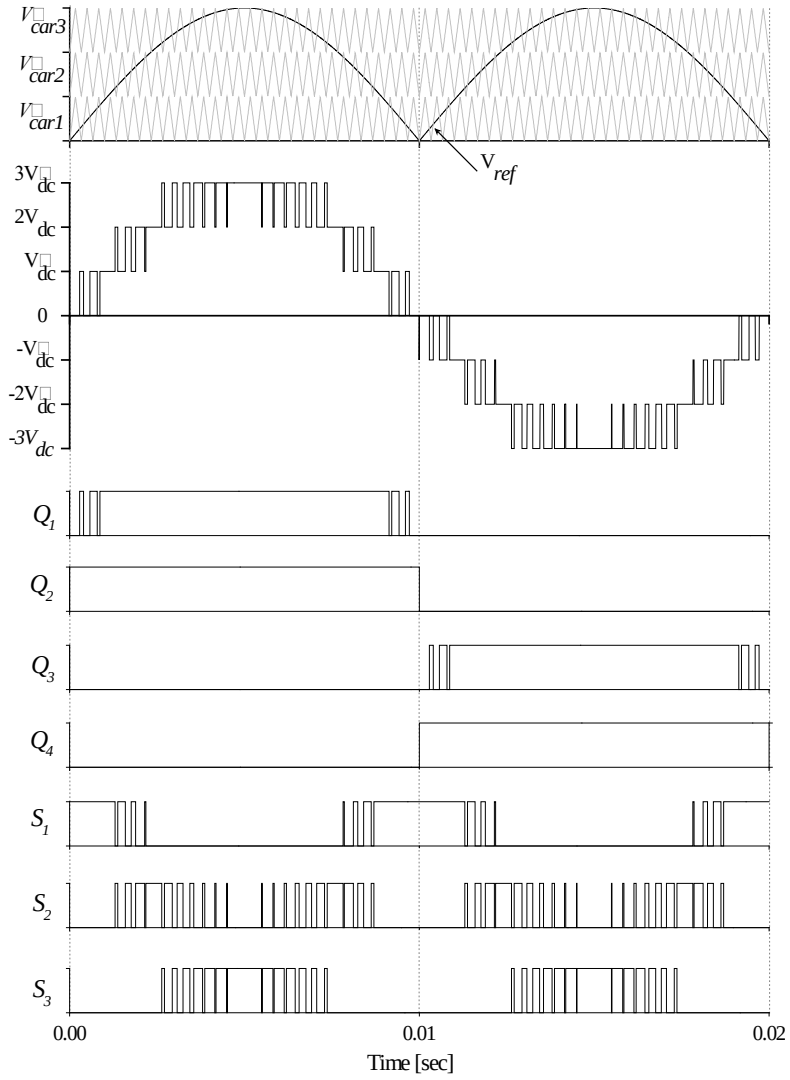


Figure 4. Switching pattern of single-phase seven-level inverter.

by Equation (6), between 0 and 0.33 and the output voltage will have three levels *i.e.* $\pm V_{dc}$, 0). However, if the intersection occurs between V_{ref} and V_{car2}, MI will be in the range of 0.33 and 0.67 and the output voltage will have five levels (*i.e.* $\pm V_{dc}$, , $\pm 2V_{dc}$, 0). By contrast, if the intersection occurs between V_{ref} and V_{car3}, MI will be greater than 0.67 and the output voltage will have seven levels (*i.e.* $\pm 3V_{dc}$, $\pm 2V_{dc}$, $\pm V_{dc}$, 0).

$$MI = \frac{A_m}{3A_c} \tag{6}$$

5. Voltage Control Strategy

The closed loop voltage regulation of the proposed seven-level inverter is shown in **Figure 5**. In order to reduce the ripple contents in output voltage and current of the load, an LC filter has been used. A PI controller is used to regulate the output voltage V_{out} at the load terminals to be near sinusoidal similar to the

reference voltage V_{out}^{*}. The actual voltage is compared with the reference one to obtain an error signal which applied to a PI controller to provide the modulated signal (U). After that, the modulated signal is compared with the LSPWM carriers to provide the switching states.

6. Experimental Validation

The overall experimental prototype has been implemented and tested to prove the validity of the proposed inverter. Figure 6 presents the experimental prototype of the proposed seven-level inverter. The experimental results for all variables are taken by a digital oscilloscope (Tektronix MSO2014). The output load current (I_{out}) is measured using a current probe (Tektronix TCP 300). The dSPACE_CP 1103 is chosen as the controller for the proposed inverter and experimental results' efficiency is taken by power analyzer (Yokogawa WT1800). THD analysis of the terminal and load voltages (V_{ab}, V_{out}) at different values of MI are also calculated. The single-phase seven-level inverter is implemented using the five power switches (Q_1, Q_2, Q_3, Q_4 and S_1) with MOSFET (IRFP460) in contrast, the two power switches (S_2 and S_3) as IGBT/without anti-parallel diode (IGW50N65F5FKSA1).

A single-phase seven-level inverter to feed a stand-alone resistive load in addition to an LC filter has been evaluated. Experimental results have been investigated at 10 kHz as a switching frequency (F_{sw}) with three identical DC voltage sources of 50 V. The experimental parameters are given in Table 2. Dead time is taken into account with 2 μs. As mentioned before, the number of output levels depends mainly on MI; different values of MI are investigated to prove the validity of the proposed inverter.

Table 2. Experimental system parameters.

Input DC voltage source ($V_1 = V_2 = V_3$)	50 V
Rated power	250 W
Fundamental frequency	50 Hz
Switching frequency (F_{sw})	10 kHz
Dead-time	2 μs
Load parameters	
Resistance load [R_l]	42 Ω
R-L load [R_l, L_l]	72 Ω, 160 mH
Filter parameters	
L_f	7 mH
C_f	5 μF
PI controller gains	
Proportional gain [K_p]	0.005 A/V
Integral gain [K_i]	10,000 A/V.s

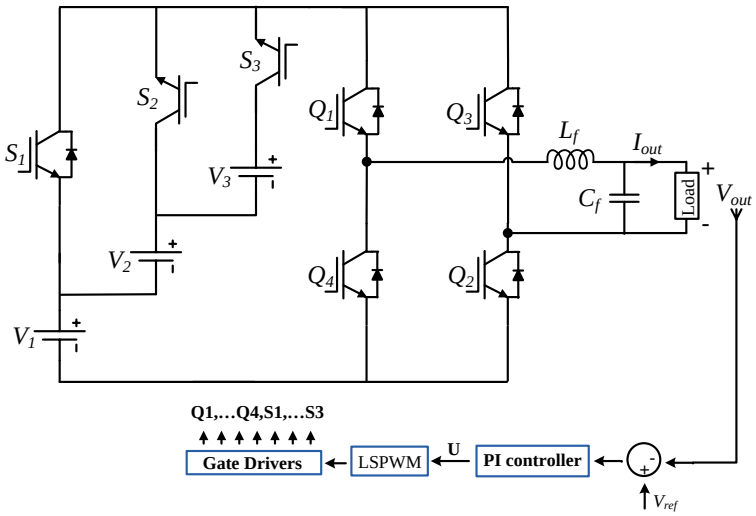


Figure 5. Control scheme.

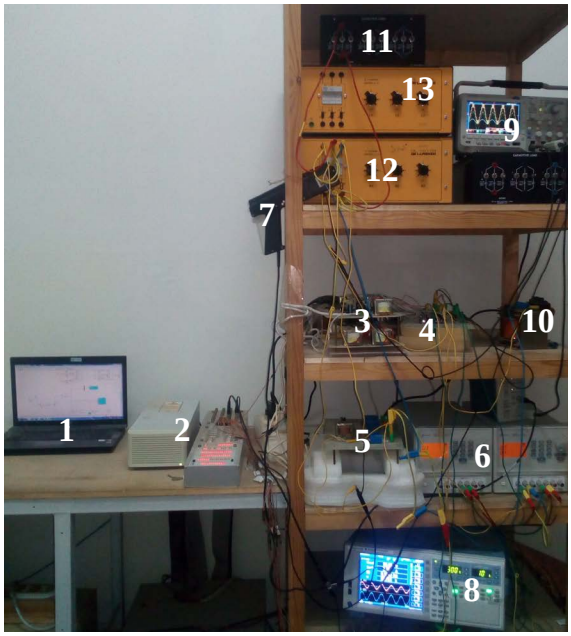
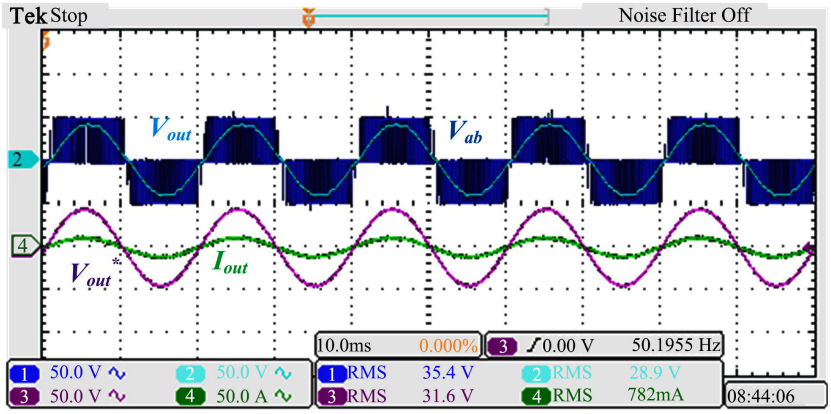


Figure 6. Experimental prototype. 1) PC; 2) dSPACE_CP1103; 3) Gate drive circuit; 4) Proposed MLI; 5) Voltage sensor circuit; 6) DC voltage sources; 7) Current probe; 8) Power analyzer WT1800; 9) Oscilloscope Tektronix; 10) Inductive filter; 11) Capacitive filter; 12) Resistive load; 13) Inductive load.

Figure 7 shows the experimental results of the inverter output voltage (V_{ab}), reference and load voltage (V_{out}^{*}, V_{out}) and load current (I_{out}) at different values of MI. The proposed inverter output can be three, five, and seven levels. Figure 7(a) provides the inverter three-level voltage, reference, output voltage, and output current for MI = 0.3 and the peak value of 45 V of reference voltage. As can be seen the actual load voltage follows the reference voltage. The THD has been reached (up to 600 kHz) from **58.27%** for inverter output voltage to **5.02%** for the load output voltage. For MI = 0.6, the inverter provides five levels at its

output for a peak value of 90 V as shown in Figure 7(b) with THD of **31.46%** and **2.42%** for the inverter and load output voltage, respectively. The seven-level result is shown in Figure 7(c) by taking reference voltage as 135 V as a peak value at MI = 0.9. **21.82%** and **2.13%** are the THD values for the inverter and load output voltage, respectively. From Figures 7(a)-(c), it is clear that the load output voltage (V_{out}) tracks the reference voltage (V_{out}^{*}).



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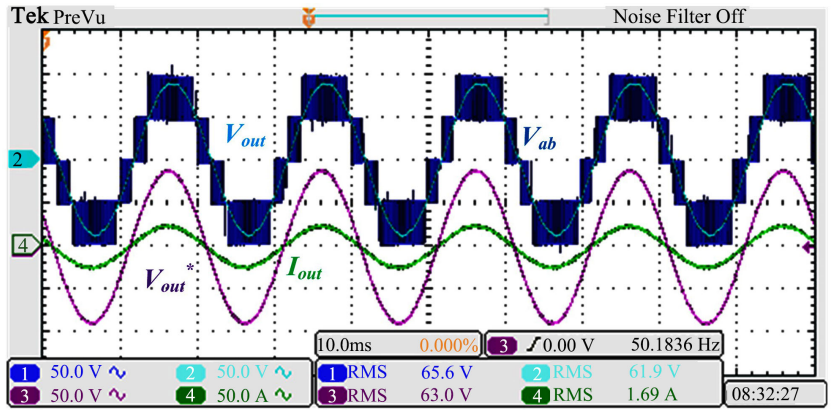

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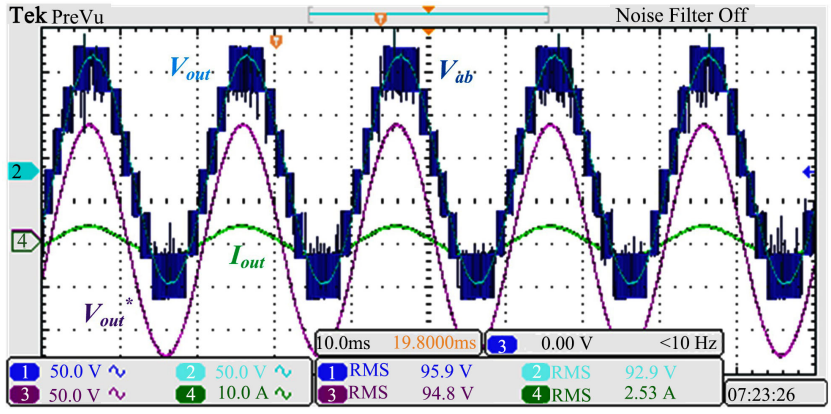


(c)

Figure 7. Experimental results for single-phase seven-level inverter with resistive load. (a) MI = 0.3; (b) MI = 0.6; (c) MI = 0.9.

In order to ensure the stability of the proposed inverter, a step change in the inverter output voltage according to change in the modulation index has been made. Figure 8 provides a change in MI from 0.3 to 0.9 thus the number of the output voltage changes from three-level to seven-level with resistive load of 42 Ω. As shown, the output voltage provides fast response to the step change. Figures 9(a)-(c) present the RMS value of output voltage and current, and the output power and inverter efficiency for MI = 0.3, 0.6, and 0.9, respectively.

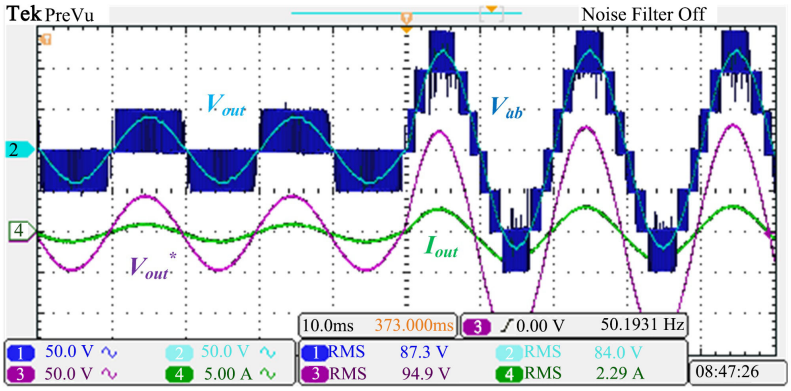


Figure 8. Experimental results for single-phase seven-level inverter with step change in MI.

(a)

(b)

(c)

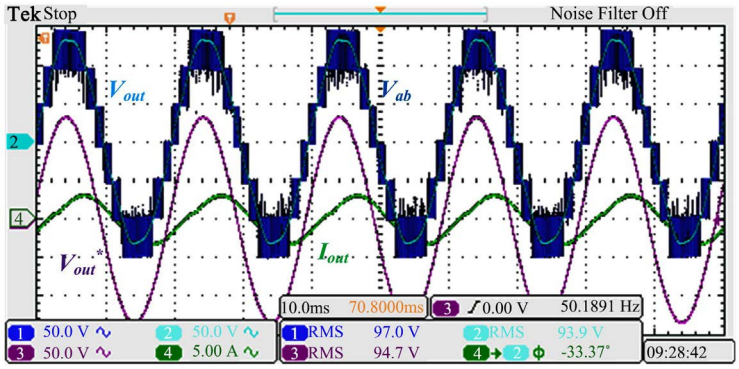
Figure 9. Experimental results for output power and efficency. (a) MI = 0.3; (b) MI = 0.6; (c) MI = 0.9.

Also, the proposed inverter has been operated when the load is R-L load of (R_l = 72 Ω and L_l = 160 mH). The experimental results with R-L load are shown in **Figure 10**. Seven-level output voltage at MI = 0.9 with inductive load is shown in **Figure 10(a)** while, a step change has been made with inductive load as shown in **Figure 10(b)**. As seen that the proposed inverter can be operated under variation in MI and type of load. **Figure 11** presents the efficiency with different values of output power.

A comparison has been made with recent topologies in the value of the efficiency and THD of the proposed inverter as presented in **Table 3**. From **Table 3**, THD of the proposed inverter is better than in [24] for seven-level output voltage due to the switching pattern used in the mentioned reference has distorted the output voltage also efficiency is better due to lower switching devices used in the proposed inverter. Also, five-level output voltage in [25] almost has better efficiency compared with the proposed inverter with five levels due to the inverter is operated at higher rated power compared with the proposed inverter. As shown from the figure the inverter efficiency is increased and THD is reduced with an increment of MI.

7. Conclusion

In this paper, a new multilevel inverter topology was proposed which can be extended to any number of levels by adding one DC source and one power switch for the repeating stages. A comparative study presented the merits of the proposed inverter which offers lower circuit components, total blocked voltage, and level to switching device ratio compared with most recent topologies, thereby reducing circuit complexity and total cost. Experimental results have been carried out to provide the validity of the proposed topology for a voltage closed-loop operation under variation on types of load and modulation index. The experimental results provide low THD value of 2.13% for the load output



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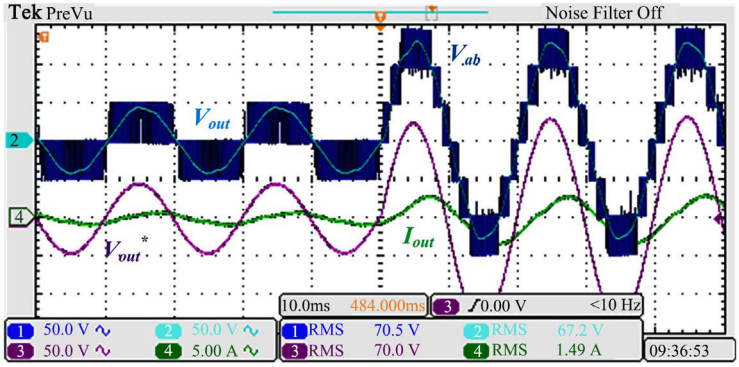

(b)

Figure 10. Experimental results with inductive load. (a) MI = 0.9; (b) Step change in MI.

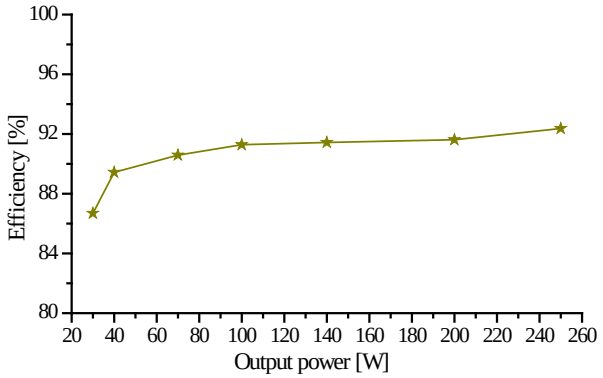

Figure 11. Efficiency versus output power.

Table 3. Comparison in THD and efficiency.

Ref.	THD of V_{out}	Efficiency	Number of levels
[22]	2.4%	-	Five
[23]	5.4%	-	Five
	3.9%	-	Seven
[24]	3%	89%	Five
	5%	92%	Seven
[25]	3%	90.7%	Five
Proposed MLI	**2.42%**	**90.4%**	**Five**
	2.13%	**92.18%**	**Seven**

voltage and efficiency of 92%. The low THD value and high efficiency present the strength of the proposed inverter.

Acknowledgements

The authors would like to thank General Administration of Postgraduate Studies and Researches-Scientific Research Administration-South Valley University for financial support of this work.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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