

Comparative Methodical Assessment of Established MOSFET Threshold Voltage Extraction Methods at 10-nm Technology Node

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Abstract

Threshold voltage (V_{TH}) is the most evocative aspect of MOSFET operation. It is the crucial device constraint to model on-off transition characteristics. Precise V_{TH} value of the device is extracted and evaluated by several estimation techniques. However, these assessed values of V_{TH} diverge from the exact values due to various short channel effects (SCEs) and non-idealities present in the device. Numerous prevalent V_{TH} extraction methods are discussed. All the results are verified by extensive 2-D TCAD simulation and confirmed through analytical results at 10-nm technology node. Aim of this research paper is to explore and present a comparative study of largely applied threshold extraction methods for bulk driven nano-MOSFETs especially at 10-nm technology node along with various sub 45-nm technology nodes. Application of the threshold extraction methods to implement noise analysis is briefly presented to infer the most appropriate extraction method at nanometer technology nodes.

Keywords

Threshold Voltage, Constant Current Source Technique, Linear Extrapolation Technique, Threshold Voltage Estimation Techniques, Short Channel Effects, Drift Diffusion Model, Resistive Load Inverter, Noise Margin Analysis

1. Introduction

Incessant abridging of IC technology, together with precision of V_{TH} control techniques and reduction in SCE, is asserting the V_{TH} to very low values. For proper operation of MOSFET, we need to evaluate exact threshold voltage (V_{TH}). Perfectly appraised V_{TH} is required to provide proper gate control over device channel conduction (see **Figure 1**). The tens of millivolts miscalculation cannot be neglected as it can prompt serious er-

rors in circuit functionality. Especially for robust nano-scale design of analog circuits with high speed operation, precise valuation of V_{TH} is essential to illustrate the exact device behaviour [1] [2] [3] [4]. Device matching also depends on the estimated V_{TH} values. V_{TH} is frequently used for accessing and predicting device performance. It is also commonly used to check the inconsistency due to manufacturing process technological parameter fluctuations. Other applications of V_{TH} can be listed as to evaluate reliability factors such as radiation damage, hot carrier, stress, temperature instability, ageing degradation etc.

The threshold voltage parameter is largely extracted directly from the transfer characteristics of the device. There is no critical point in the I_D - V_{GS} curve that can be recognized as threshold point due to sub-threshold leakage current. This creates vagueness in V_{TH} estimation. The weak inversion region shows exponential deviations while strong inversion shows linear/quadratic deviations. However, the V_{TH} is identified amid weak and strong inversion transition region [5] [6]. V_{TH} also depends on several device parameters (Gate width, Gate Overlap, Gate length, biased bulk, temperature etc.) and process technology limitations (C_{ox} , t_{ox} , doping concentration (NA) etc.) [7] [8]. This makes V_{TH} estimation more challenging.

In consideration to the above, this paper presents the study and analysis of numerous V_{TH} extraction methods at various sub 45-nm technology node. The outcomes of the analysis are implemented on a simple resistive load inverter for computing noise margins to infer the performance of various threshold voltage extraction methods at sub 45-nm technology node.

Rest of the paper is organized as follows. Section 2 categorizes several threshold voltage extraction methods on the basis of their assessment methodology. Section 3 to Section 8 discuss and evaluate the various mentioned threshold voltage extraction methods at 10-nm technology node and other sub 45-nm technology nodes. Further, Section 9 presents the tabulated compiled simulation results, comparison and discussion for various sub 45-nm technology nodes. Application of the threshold extraction methods to implement noise analysis is briefly presented in Section 10. Finally, concluding remarks

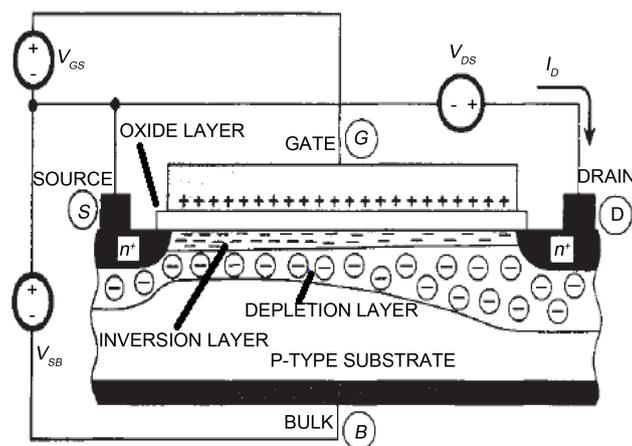


Figure 1. Source referred n-channel MOS transistor biasing.

are conferred in Section 11.

2. Threshold Voltage Estimation Techniques

Ideally, V_{TH} of a device is the critical gate voltage below which the drain to source current (I_D) is zero, But practically, sub-threshold leakage current exists for V_{GS} below V_{TH} . As the drain current doesn't drop abruptly to zero and hence, it becomes challenging to precisely determine the critical point at which switching of I_D takes place. Due to this reason, several procedures presented in literature use diverse descriptions to extract the V_{TH} of the MOSFET but still has a scope for improvement to correctly evaluate V_{TH} [9] [10]. This paper revisits V_{TH} extraction techniques and examines these for simplified square-sized NMOS device at 10-nm technology node. For precise evaluation of the methods, the process is reiterated in similar conditions on other sub 45-nm technology nodes [11] [12].

For simplicity, the threshold extraction methods have been categorized into six main groups on the basis of their assessment methodology as:

- 1) I_D based extraction methods;
- 2) Derivative of I_D based extraction methods;
- 3) Integral of I_D based extraction methods;
- 4) Self-extraction methods;
- 5) Deviation based extraction methods;
- 6) Hybrid extraction methods.

It is considered that the threshold voltage changes with the change in the operating region of the MOSFET specifically in linear/ triode region and saturation region. Distinctive efforts are made to accurately calculate the V_{TH} in both the operating regions [13] [14] [15]. Hence the corresponding respective values of V_{TH} are evaluated as V_{LIN} and V_{TSAT} for all the discoursed methods on our test device. **Figure 1** shows the basic biasing settings for n-channel MOSFET. The test device considered is a square-sized uniformly doped bulk driven n-channel nano-MOSFET with 10-nm channel length. The source and drain regions are laterally identical with gradual doping characteristics. Special effects were considered to extract the realistic output of the device. **Figure 2** represents the transfer characteristics of our test device.

3. ID Based Extraction Methods

These methods use the drain current (I_D) directly in the extraction method of threshold voltage. Some common methods listed underneath are briefly discussed below.

3.1. Constant Current Source (CCM) Method

This method determines V_{TH} as the gate voltage for an arbitrary critical drain current ($I_{DCRITICAL}$) value [16] [17]. To estimate the V_{TH} using this method, I_D versus V_{GS} graph is plotted on a semi-logarithmic scale for two extreme values of V_{DS} *i.e.* high biased and low biased. For our test device, we considered $V_{DS} = 0.9$ V and $V_{DS} = 0.1$ V respectively. The $I_{DCRITICAL}$ is technology reliant, generally considered as $(0.1 \mu A) \times (W/L)$, where W

and L are the gate width and gate length.

$$V_{TH} = V_{GS} | I_{DCRITICAL} \tag{1}$$

$I_{DCRITICAL}$ referred in Equation (1) is designated such that V_{TH} is on the transition point of linear-sub-threshold region of the device [11] [18] [19].

Implementation of CCM on Test Device

The technique was implemented on our test device square-sized NMOS with 10-nm technology node and was repeated in similar conditions on other sub 45-nm technology nodes. **Figure 3** represents the simulated results and extraction output (V_{TLIN} and V_{TSAT}) using CCM on our test device.

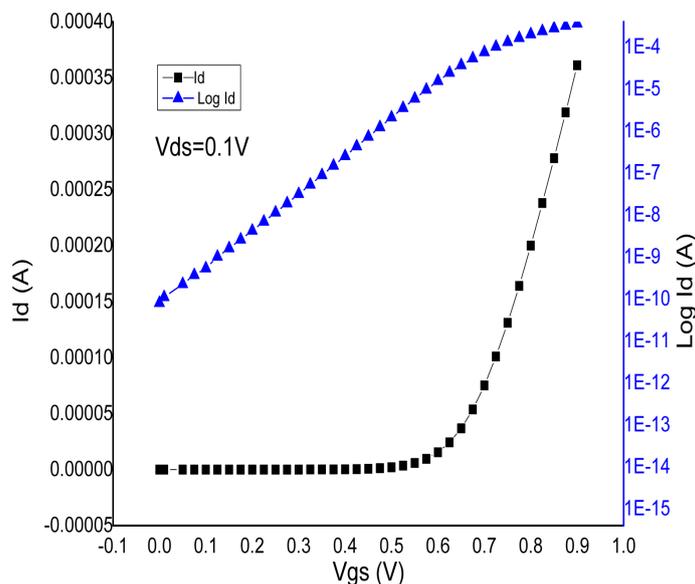


Figure 2. Transfer characteristics of the test device for $V_{DS} = 0.1$ V.

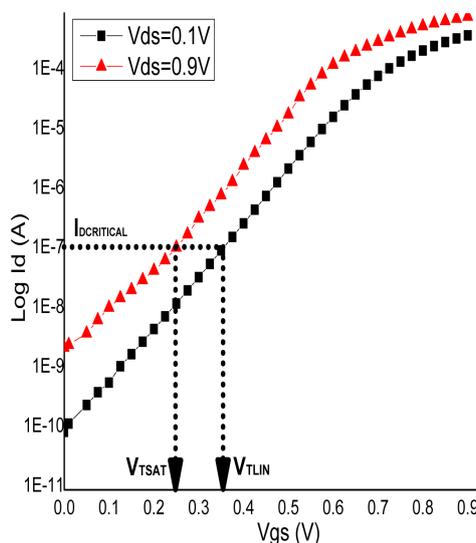


Figure 3. Extraction of V_{TSAT} and V_{TLIN} using CCM for $V_{DS} = 0.9$ V and $V_{DS} = 0.1$ V.

The outcome of the results was as follows:

$$V_{TSAT} = 0.25 \text{ V @ } V_{DS} = 0.9 \text{ V}$$

$$V_{TLIN} = 0.35 \text{ V @ } V_{DS} = 0.1 \text{ V .}$$

3.2. Drift-Diffusion Equality (DDE) Method

Diffusion current governs the total current in sub-threshold region whereas drift current dominates in strong inversion region. This DDEM process states that by applying low drain voltage ($V_{DS} \approx 0.1 \text{ V}$), the threshold voltage is the distinctive gate voltage at which the condition $I_{DRIFT} = I_{DIFFUSION}$ holds true [20] [21]. Hence, statistically we can represent the threshold voltage value as:

$$V_{TH} = V_{GS} | I_{Drift} = I_{Diffusion} \tag{2}$$

where I_{Drift} and $I_{Diffusion}$ represent the drift current and diffusion current respectively.

Implementation of DDEM on Test Device

The technique was implemented on the test device.

The outcome of the result was as follows:

$$V_{TLIN} = 0.44 \text{ V @ } V_{DS} = 0.1 \text{ V .}$$

The DDEM process has the restriction of low biased $V_{DS} = 0.1 \text{ V}$. Since the device is always made to operate in linear region, hence the saturation region threshold voltage V_{TSAT} could not be calculated. **Figure 4** shows the simulated results of our test device for I_{DRIFT} and $I_{DIFFUSION}$ with the variation in V_{GS} to extract the threshold voltage.

4. Derivative of ID Based Methods

These methods use the derivative or the higher order derivate of the drain current value in the extraction method of threshold voltage. Fundamental V_{TH} extraction methods using this respective technique are briefly discussed below.

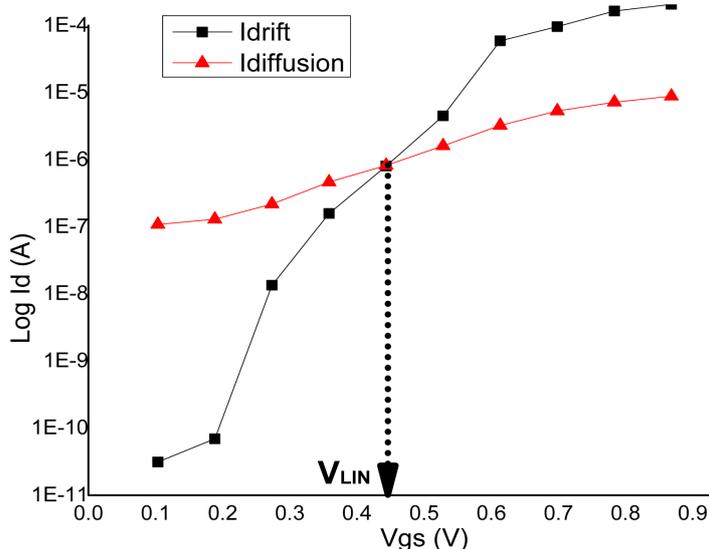


Figure. 4. Extraction of V_{TH} using DDEM on the test device for $V_{DS} = 0.1 \text{ V}$.

4.1. Linear Extrapolation (LEM) Technique

In this LEM technique, we determine the V_{TH} of the transistor using transconductance (g_m) and I_{DS} - V_{GS} curve. The g_m is defined as the derivative (slope) of I_D - V_{GS} relationship. The extreme g_m obtained on the I_D - V_{GS} characteristic curve is used to extrapolate the gate voltage (V_{GS}) as shown in **Figure 5**. The attained V_{GS} is extracted V_{TH} for the given conditions. The I_D for linear region is associated with V_{GS} as:

$$I_D \propto (V_{GS} - V_{TH} - V_{DS}/2) V_{DS} \quad (3)$$

This LEM process provides clear steps for V_{TH} assessment but it is partial to linear region of operation *i.e.* for low values of V_{DS} . Maximum g_m point is not obtainable for higher values of V_{DS} . Furthermore, the DIBL effect also comes into picture for higher V_{DS} and diminishes effective V_{TH} values. Apart from these issues, this method also lacks to determine a constant V_{TH} as dissimilar methods used for attaining maximum g_m values. g_m also depends on SCEs such as velocity saturation, overlap variations, extrinsic resistance, channel length modulation and so on. This reliance of g_m and critical point of maximum g_m is tough to accurately model. Henceforth, this produces loopholes in this process to precisely evaluate the V_{TH} .

Implementation of LEM on Test Device

The technique was implemented on the test device.

The outcome of the result was as follows:

$$V_{TLIN} = 0.67 \text{ V} @ V_{DS} = 0.1 \text{ V}.$$

As described above, the Maximum g_m is not obtainable for higher values of V_{DS} . Hence special efforts were made to calculate V_{TSAT} using this method. **Figure 5** shows the transfer characteristics of the test device and the g_m variation with the variation in V_{GS} at constant $V_{DS} = 0.1 \text{ V}$.

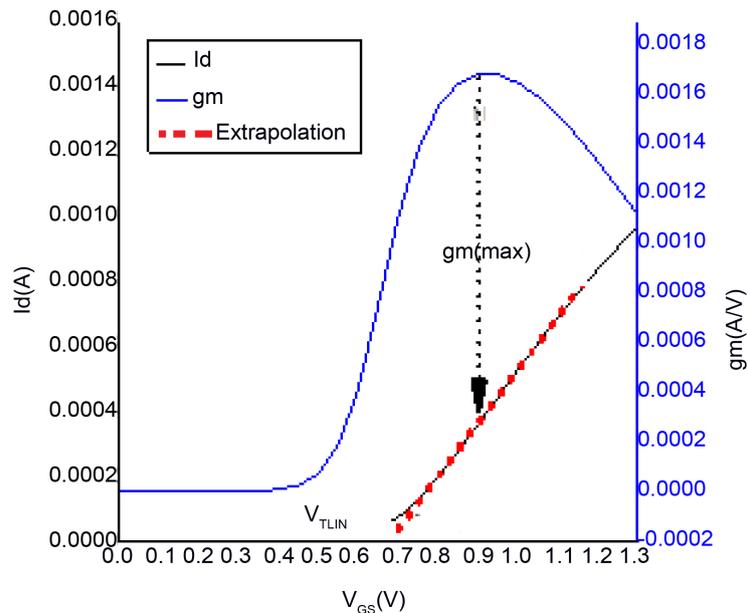


Figure 5. Extraction of V_{TLIN} using LEM for $V_{DS} = 0.1 \text{ V}$.

4.2. Quadratic Extrapolation (QEM) Method

Technique named Quadratic Extrapolation Method (QEM) is also called as “Linear Extrapolation in Saturation Region”. It is used to calculate threshold voltage using LEM in saturation region (V_{TSAT}). As mentioned in LEM, the I_D for linear region is proportional to $(V_{GS} - V_{TH})$. Similarly, I_D in saturation region is proportional to $(V_{GS} - V_{TH})^2$ as shown in Equation (4):

$$I_D \propto (V_{GS} - V_{TH})^2 \tag{4}$$

Hence V_{TSAT} can be extracted by extrapolating the curve $\sqrt{I_D}$ versus V_{GS} at the inflexion point of the curve as shown in **Figure 6**.

Implementation of QEM on Test Device

The technique was implemented on the test device.

The outcome of the result was as follows:

$$V_{TSAT} = 0.46 \text{ V @ } V_{DS} = 0.9 \text{ V .}$$

4.3. Second-Derivative (SD) Method

The second-derivative method (SDM), formerly entitled as transconductance change method [21] [22], was developed to avoid dependence on series resistances. It evaluates V_{TH} as the V_{GS} value at which the derivative of the transconductance (*i.e.*, $dg_m/dV_G = d^2I_D/dV_G^2$) is a maximum. To intricate the logic, it uses the ideal case of a simple Level = 1 MOSFET SPICE model, where $I_D = 0$ for $V_G < V_T$, and I_D is directly proportional to V_G for $V_G > V_T$. With these suppositions, dI_D/dV_G becomes a step function, which is zero for $V_G < V_T$ and is a positive constant for $V_G > V_T$. Therefore, d^2I_D/dV_G^2 will go to infinity exactly at $V_G = V_T$. Such a simple assumption is apparently not true in a real device, and thus d^2I_D/dV_G^2 will not turn out to be infinite at V_T . However, it will exhibit a maximum value at $V_{GS} = V_{TH}$. **Figure 7** shows the SDM output waveform of the test device for V_{TLIN} extraction at constant $V_{DS} = 0.1 \text{ V}$.

The execution of this SDM process in the linear region is extremely sensitive to

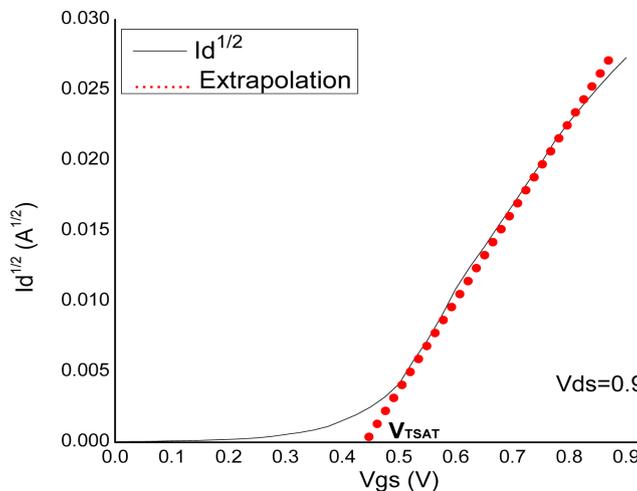


Figure 6. Extraction of V_{TSAT} using QEM for $V_{DS} = 0.9 \text{ V}$.

measurement error and noise, as the second derivative amounts to applying a high-pass filter to the measurement [23].

Implementation of SDM on Test Device

The technique was implemented on the test device. The process was widely affected by noise. Special possessions of filtration and smoothing of curve were considered to extract the correct output as shown in **Figure 8**.

The outcome of the result was as follows:

$$V_{TLIN} = 0.62 \text{ V at } V_{DS} = 0.1 \text{ V}$$

$$V_{TSAT} = 0.49 \text{ V at } V_{DS} = 0.9 \text{ V}.$$

4.4. Third-Derivative (TD) Method

In this TDM process, it has been proposed that the V_{TH} can be extracted from the value

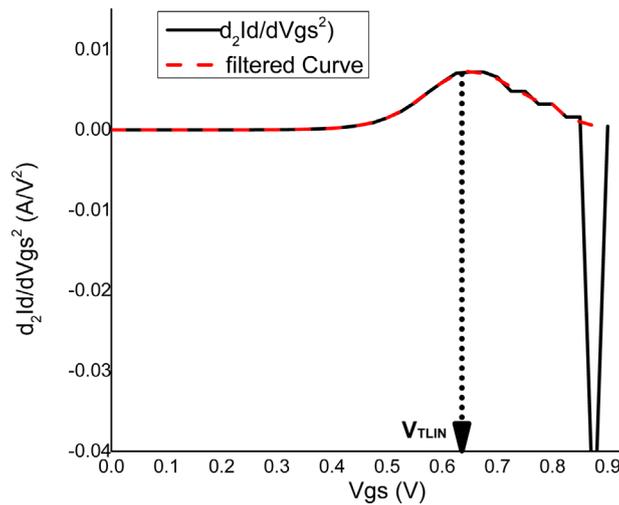


Figure 7. Extraction of V_{TLIN} using SDM for $V_{DS} = 0.1 \text{ V}$.

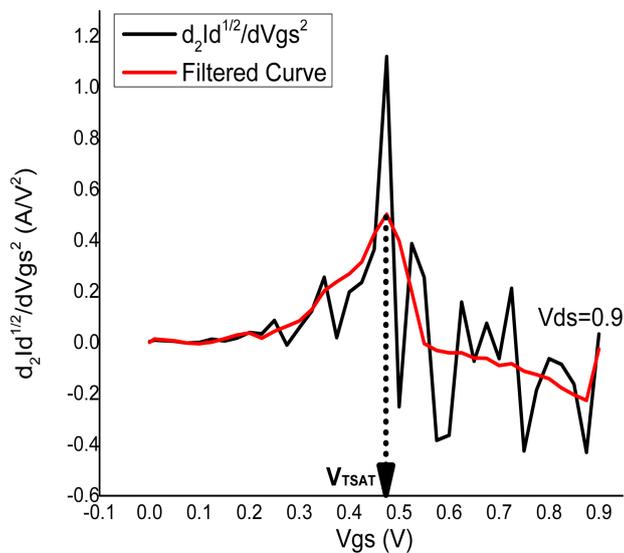


Figure 8. Extraction of V_{TSAT} using SDM for $V_{DS} = 0.9 \text{ V}$.

of V_{GS} at which the third derivative of the current I_D (*i.e.*, $d^3I_D = dV_{GS}^3$) has a maximum value [24]. Conversely, the maxima and minima of the third derivative always fall to the left and right of the second derivative maxima, which is located at d^2I_D/dV_{GS}^2 . **Figure 9** clearly illustrates this fact. Therefore, the third derivative technique is evidently incompatible with the broadly used second derivative method.

Figure 9 and **Figure 10** present the application of this TDM process to the 10-nm technology node test device in the linear and saturation regions, at drain voltages of 0.1 V and 0.9 V, respectively. It is clear from these figures that the TDM technique is extremely affected by tentative noisy data. Though investigational noise could be diminished by numerical flattening techniques or by fitting the semi-empiric models, the extracted V_{TH} value would still be irreconcilable with that extracted by the SD method.

Implementation of TDM on Test Device

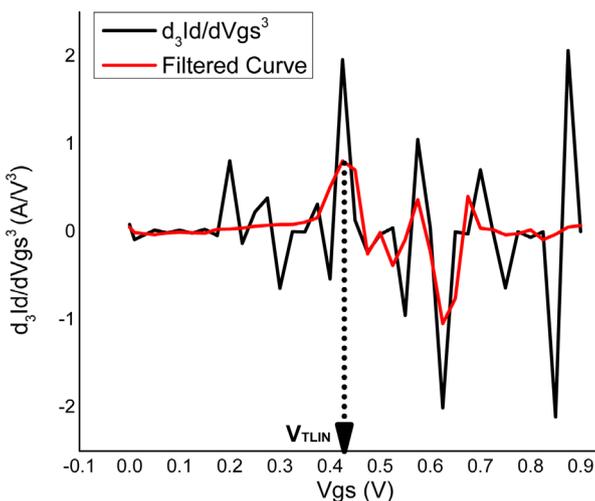


Figure 9. Extraction of V_{TLIN} using TDM for $V_{DS} = 0.1$ V.

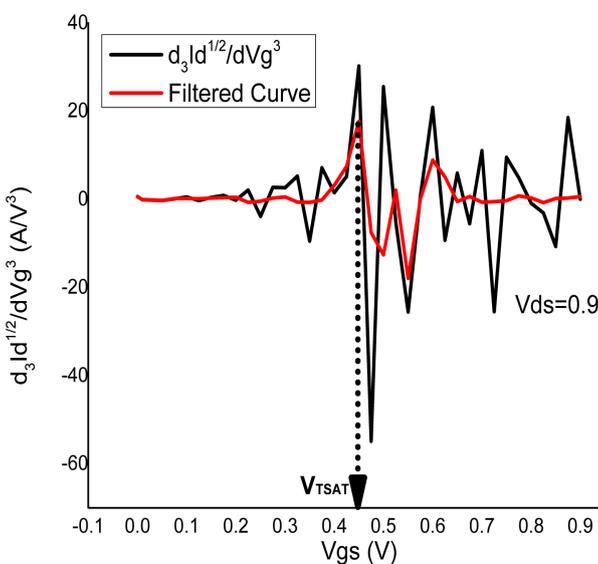


Figure 10. Extraction of V_{TSAT} using TDM for $V_{DS} = 0.9$ V.

The technique was implemented on the test device. The method was vastly affected by the investigational noise. Hence it was challenging to extract the threshold values. Special properties of smoothing and filtration of the curve were considered to extract the correct output. Even after high considerations, it was observed that V_{TLIN} value was lower than V_{TSAT} value which is commonly unusual.

The outcome of the result was as follows:

$$\begin{aligned} V_{\text{TLIN}} &= 0.43 \text{ V} \quad \text{at} \quad V_{\text{DS}} = 0.1 \text{ V} \\ V_{\text{TSAT}} &= 0.45 \text{ V} \quad \text{at} \quad V_{\text{DS}} = 0.9 \text{ V} . \end{aligned}$$

4.5. Ghibaudo Method/Current-to-Square-Root-of-Transconductance Ratio (CsrTR) Method

The CsrTR method formerly called as Ghibaudo Method (GM) was developed to dodge the extracted V_{TH} value dependence on mobility degradation and parasitic series resistance [25] [26] [27]. The ratio of the drain current to the square root of the transconductance, in the linear region, is given by Equation (5) as:

$$\text{GM} = I_{\text{D}}/\sqrt{g_{\text{m}}} = I_{\text{D}}/\sqrt{(dI_{\text{D}}/dV_{\text{GS}})} \Rightarrow \text{GM} \propto (V_{\text{GS}} - V_{\text{TH}}) \quad (5)$$

The GM technique, also occasionally called as “the modified Y function method”, has been freshly enhanced for application to contemporary devices using a more universal mobility degradation model.

The V_{TH} is extracted from the intercept of the GM versus V_{GS} linear fit. **Figure 11** shows the results of applying this method to the present test device in the linear region. As can be witnessed, it is not very clear in the method from where to linearly extrapolate to find the V_{GS} axis intercept. It does not evidently show the supposedly expected linear behavior. Therefore, the linear extrapolation shown in **Figure 11** is only a guess, amidst the evident non-linearity present.

Implementation of Ghibaudo Method (GM) on Test Device

The technique was implemented on the test device. Non-linearity in the curve caused difficulties in extrapolation process to estimate the required values. **Figure 12** shows the results of applying this method to the present test device in the saturation region.

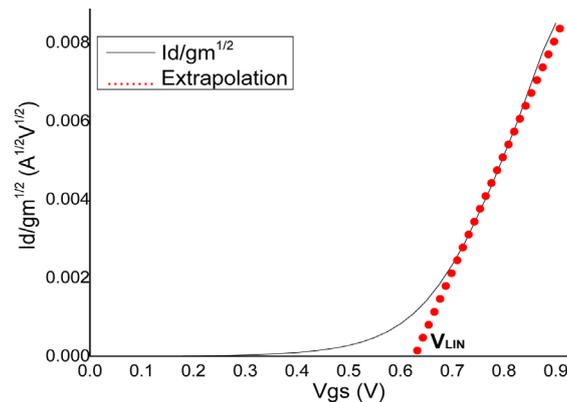


Figure 11. Extraction of V_{TLIN} using Ghibaudo Method for $V_{\text{DS}} = 0.1 \text{ V}$.

The outcome of the result was as follows:

$$V_{TLIN} = 0.61 \text{ V at } V_{DS} = 0.1 \text{ V}$$

$$V_{TSAT} = 0.49 \text{ V at } V_{DS} = 0.9 \text{ V}.$$

4.6. Transconductance to Current Ratio (TCR) Method

This method is based on calculating TCR as the ratio of transconductance to the drain current as described in Equation (6) [28] [29]:

$$TCR = g_m / I_D = (dI_D / dV_{GS}) / I_D = d \ln(I_D) / dV_{GS} \tag{6}$$

It states that the threshold voltage can be determined as the value of V_{GS} where TCR presents its maximum negative slope *i.e.* V_{GS} corresponding to the minimum value of curve $dTCR/dV_{GS}$. However, considering TCR by itself significantly increases random tentative noise, specifically in weak inversion.

Implementation of TCR Method on Test Device

The technique was implemented on the test device. The method was highly affected by the investigational noise as seen in **Figure 13** and **Figure 14** for extraction of V_{TLIN}

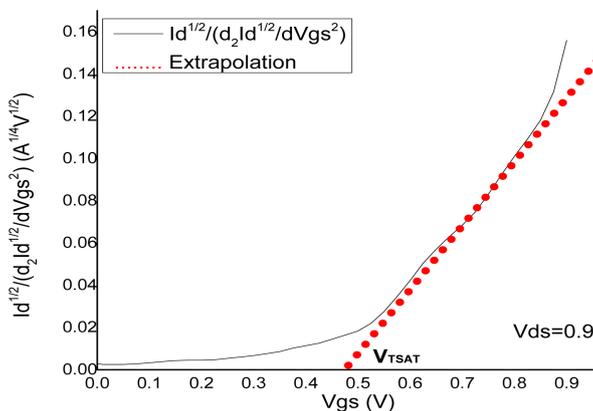


Figure 12. Extraction of V_{TSAT} using Ghibaudo method for $V_{DS} = 0.9 \text{ V}$.

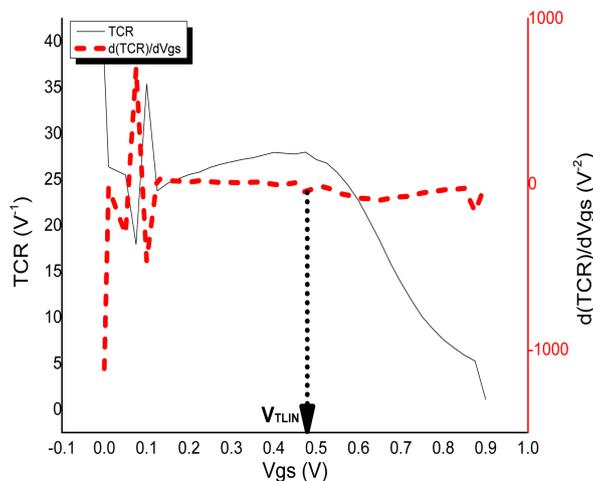


Figure 13. Extraction of V_{TLIN} using TCR for $V_{DS} = 0.1 \text{ V}$.

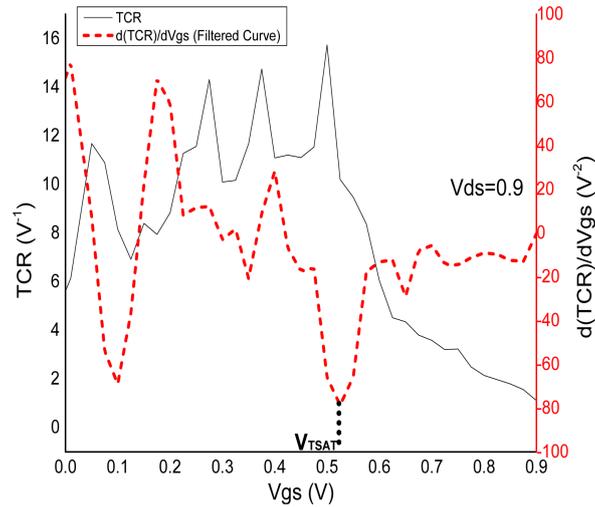


Figure 14. Extraction of V_{TSAT} using TCR for $V_{DS} = 0.9$ V.

and V_{TSAT} respectively. Hence it was challenging to extract the threshold values. Filtration and smoothening of the curve like properties were applied to extract the correct output. Even after high considerations, it was observed that V_{TLIN} value was lower than V_{TSAT} value which is generally unusual.

The outcome of the result was as follows:

$$V_{TLIN} = 0.49 \text{ V at } V_{DS} = 0.1 \text{ V}$$

$$V_{TSAT} = 0.51 \text{ V at } V_{DS} = 0.9 \text{ V .}$$

5. Integral of ID Based Methods

These methods use the integral of the drain current value in the extraction method of threshold voltage. Prevalent V_{TH} extraction methods using this technique are briefly discussed below [30] [31].

5.1. Transition Method

This TM technique was stimulated by the properties of the integral difference function $D(V,I)$, which had been formerly defined for two-terminal device as [32]:

$$D(V, I) = \int VdI - \int IdV = VI - 2 \int IdV \tag{7}$$

As shown in Equation (7), this function presents the advantageous features of eradicating the effect of any linear element (resistance) coupled in series with the device. To extract V_{TH} , the drain current is constantly measured from below the expected value of V_{TH} versus V_{GS} with a small constant drain voltage ($V_{DS} \approx 100$ mV). Subsequently, the succeeding function TM is numerically calculated from the measured data:

$$TM(V_{GS}, I_D) = D(V_{GS}, I_D) / I_D = (V_{GS} - V_{G0}) - 2 \int I_D dV_{GS} / I_D \tag{8}$$

where V_{G0} represents the lower limit of integration analogous to a gate voltage well below threshold in Equation (8). Usually chosen $V_{G0} = 0$. The logic of the method is based on the ideal case of a MOSFET, piecewise modelled as: $I_D = I_{LEAKAGE}$ for $V_{GS} < V_{TH}$ and

I_D is proportional to V_{GS} for $V_{GS} > V_{TH}$. Using the previous streamlining supposition, we observe that:

- 1) Function TM presents a discontinuity at V_{TH} ;
- 2) $TM = -V_{GS}$ for $V_{GS} < V_{TH}$; and
- 3) $TM = +V_{TH}$ for $V_{GS} > V_{TH}$.

Since for a real device such simplifying conventions are apparently not precisely true, function TM will present an extreme value due to the mobility degradation and its value will be close to V_{TH} .

A plot of TM versus V_{GS} or $\ln(I_D)$ should result in a straight line below threshold, where the current is dominated by diffusion and is principally exponential. As soon as $V_{GS} = V_{TH}$, the function TM should vitiate due to mobility degradation. The specified logic accords with the test device as shown in **Figure 15**. Hence the maximum of TM approaches the V_{TH} value of the device. The shape of the curve is swayed by the parasitic resistance and mobility degradation effects, but not significantly its maxima, lest those effects are exceedingly prominent. Hence, the parasitic series resistance consequence is not totally eradicated since a MOSFET is not a two-terminal device with node current as I_D and node voltage as V_{GS} . **Figure 16** represents the TM function output curve versus V_{GS} to extract V_{TSAT} for $V_{DS} = 0.9$ V.

Implementation of TM Process on Test Device

The technique was implemented on the test device. Smooth curves were obtained. Hence it was easy to extract the threshold values. The V_{TLIN} value and V_{TSAT} value can also be extracted through the TM versus I_D curve using the same procedure. On implementation of the mentioned logic, we got the same agreeing values of the threshold voltages.

The outcome of the result was as follows:

$$V_{TLIN} = 0.61 \text{ V at } V_{DS} = 0.1 \text{ V}$$

$$V_{TSAT} = 0.60 \text{ V at } V_{DS} = 0.9 \text{ V .}$$

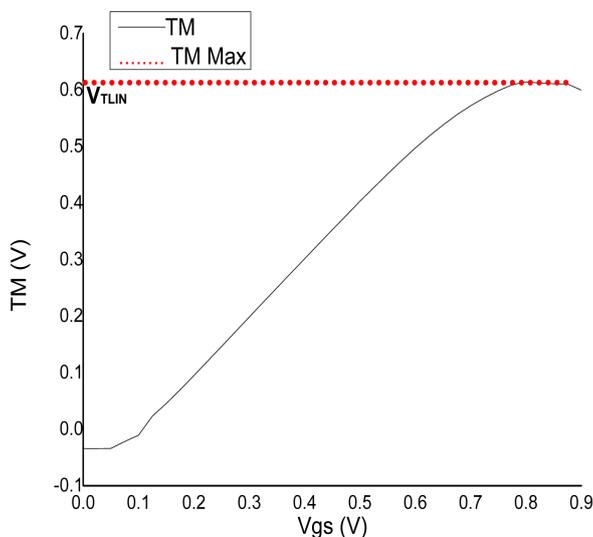


Figure 15. Extraction of V_{TLIN} using TM for $V_{DS} = 0.1$ V.

5.2. Normalized Mutual Integral Difference Method (NMID)

The NMID method was initially developed by He and co-workers in 2002 and it was also stimulated by the integral difference function NMID [31], but in this case normalized by product $I_D V_{GS}$ as shown in Equation (9):

$$\text{NMID}(V_{GS}, I_D) / (I_D V_{GS}) = 1 - 2 \int I_D dV_{GS} / (I_D V_{GS}) \quad (9)$$

Consequently, a plot of NMID versus V_{GS} will characterize a maxima at $V_{GS} = V_{TH}$. **Figure 17** exemplifies the claim of this method to the test device. Notice that the site of the maxima is autonomous of the constant term “1” which may be removed from Equation (11). A downside of this method is that the maximum of the curve is positioned in a wide region. Hence it becomes awkward to extract the analogous V_{GS} value.

Implementation of NMID Process on Test Device

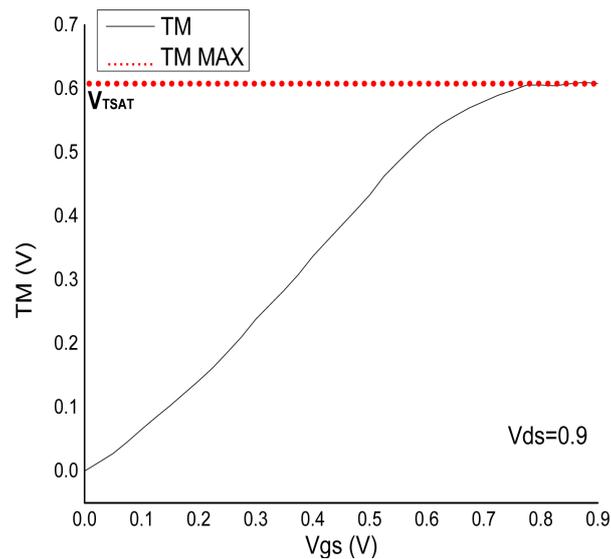


Figure 16. Extraction of V_{TSAT} using TM for $V_{DS} = 0.9$ V.

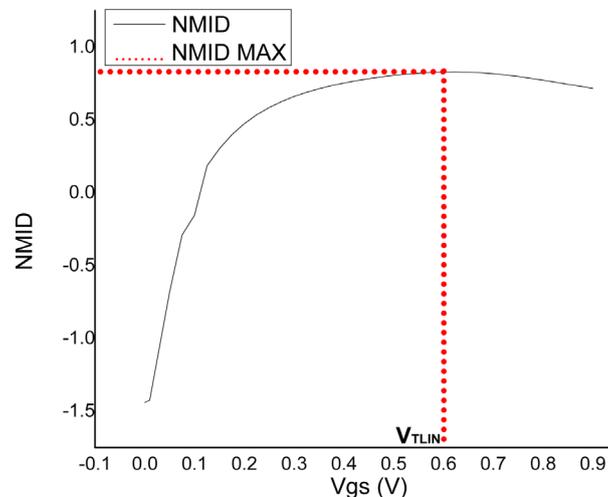


Figure 17. Extraction of V_{TLIN} using NMID for $V_{DS} = 0.1$ V.

The technique was implemented on the test device. Smooth curves were obtained. Flat curves of NMID to evaluate NMID max was challenging to extract the analogous threshold values. **Figure 18** represents the NMID function output curve versus V_{GS} to extract V_{TSAT} for $V_{DS} = 0.9$ V.

The outcome of the result was as follows:

$$V_{TLIN} = 0.6 \text{ V at } V_{DS} = 0.1 \text{ V}$$

$$V_{TSAT} = 0.56 \text{ V at } V_{DS} = 0.9 \text{ V}.$$

5.3. Normalized Reciprocal H Function (NRH) Method

The NRH method can also be labelled as “Improved NMID Method”. Eliminating the “1” term and the factor “2” from NMID Equation (11), and considering that $I_D \neq 0$ at $V_{GS} = 0$, yields a normalized version of the NRH function originally proposed in 2001 for extracting the threshold voltage of amorphous thin film MOSFETs, and later revised in 2010 to evaluate the sub-threshold slope of MOSFETs. Mathematically, the H function is represented as follows [33] [34]:

$$H(V_{GS}) = \int I_D dV_{GS} / V_{GS} (I_D - I_{D0}); \tag{10}$$

where I_{D0} is the drain current at $V_{GS} = 0$. Limit of the integral can be considered as 0 to V_{GS} in Equation (10). We propose that instead of using $H(V_{GS})$ function, its reciprocal $NRH(V_{GS})$ should be used to produce narrow maxima or minima:

$$NRH(Vg) = V_{GS} (I_D - I_{D0}) / (2 \int I_D dV_{GS}) \tag{11}$$

A factor of 2 is added to the denominator in Equation (11) to allow a simple graphical explanation of its meaning. The numerator divided by 2 is the area of a triangle with a width of V_{GS} and a height of $I_D - I_{D0}$. Then, NRH is the ratio of this triangle’s area divided by the area under the plot (the integral). **Figure 19** and **Figure 20** illustrate the application of this NRH method to the test device for the extraction of V_{TLIN} and V_{TSAT} respectively.

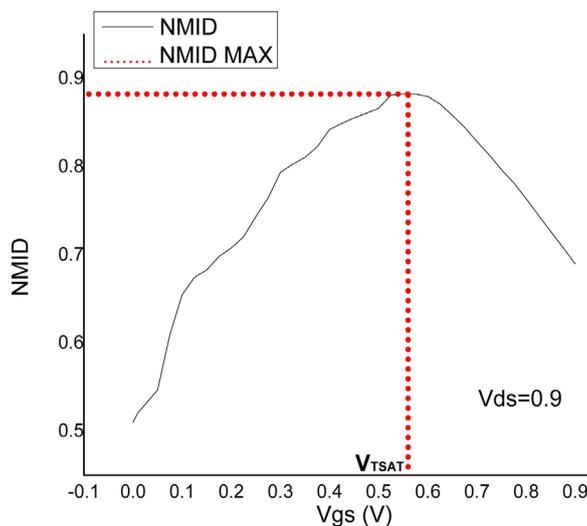


Figure 18. Extraction of V_{TSAT} using NMID for $V_{DS} = 0.9$ V.

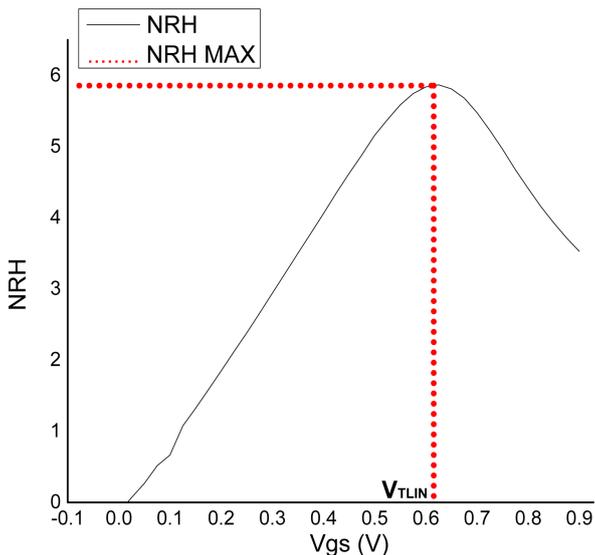


Figure 19. Extraction of V_{TLIN} using NRH for $V_{DS} = 0.1$ V.

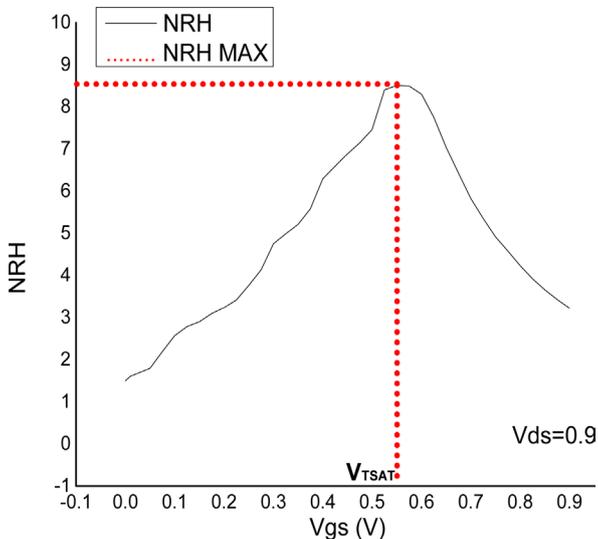


Figure 20. Extraction of V_{TSAT} using NRH for $V_{DS} = 0.9$ V.

Implementation of NRH Method on Test Device

The technique was implemented on the test device. Smooth curves were obtained. Flat curves of NRH to evaluate NRH max was challenging to extract the analogous threshold values.

The outcome of the result was as follows:

$$V_{TLIN} = 0.6 \text{ V at } V_{DS} = 0.1 \text{ V}$$

$$V_{TSAT} = 0.56 \text{ V at } V_{DS} = 0.9 \text{ V} .$$

5.4. Reciprocal H Function (RH) Method

In view of TCR, the differential value of I_D by itself expressively increases experimental noise, specifically in weak inversion, an analogous function for low gate bias. The plot

of dRH/dV_{GS} versus V_{GS} exemplifies the above statement as it can be clearly seen in **Figure 21** and **Figure 22**. The technique was proposed in 2010 based on the integration rather than differentiation to reduce unsolicited signal interference noise [33] [34]:

$$RH(V_{GS}) = (I_D - I_{D0}) / \int I_D dV_{GS} \tag{12}$$

where RH is the reciprocal of function H predefined in NRH method; I_{D0} is the drain current flow at $V_{GS} = 0$. Limits of the integral can be considered as 0 to V_{GS} . It is anticipated that the RH function could also be used to extract the threshold voltage. The V_{TH} can be extracted from the maximum negative gradient of the function RH *i.e.* $V_{GS} = V_{TH}$ analogous to the minimum value of curve dRH/dV_{GS} .

Implementation of RH Method on Test Device

The technique was implemented on the test device. The method was highly affected by the investigational noise. Hence it was challenging to extract the threshold values. As seen in **Figure 22** and **Figure 23**, distinct features like smoothing and filtration of the curve were considered to extract the correct output.

The outcome of the result was as follows:

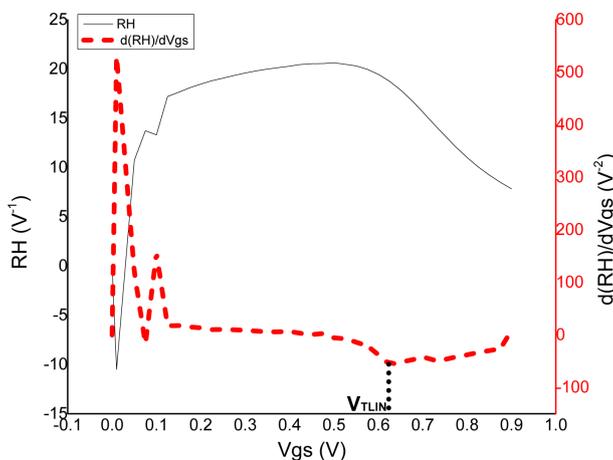


Figure 21. Extraction of V_{TLIN} using RH for $V_{DS} = 0.1$ V.

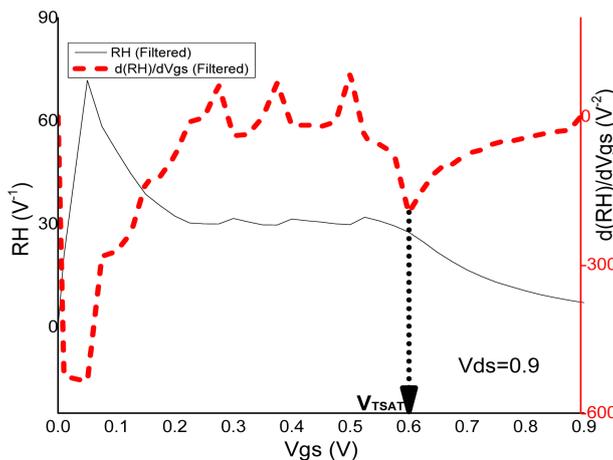


Figure 22. Extraction of V_{TSAT} using RH for $V_{DS} = 0.9$ V.

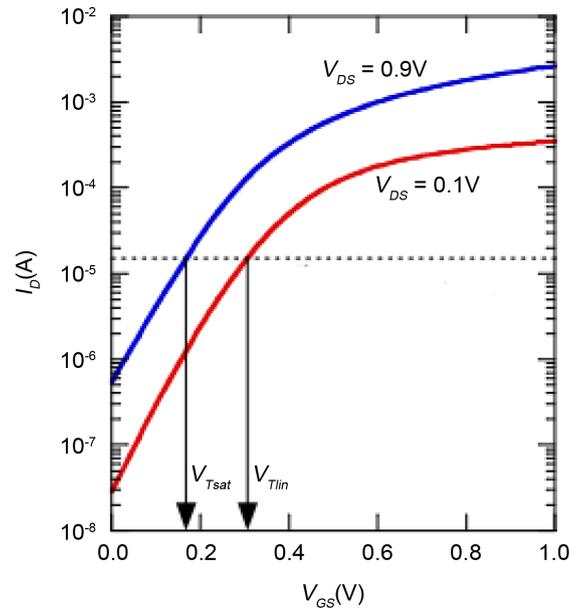


Figure 23. Implementation of HSPICE command on test device.

$$V_{TLIN} = 0.61 \text{ V at } V_{DS} = 0.1 \text{ V}$$

$$V_{TSAT} = 0.60 \text{ V at } V_{DS} = 0.9 \text{ V .}$$

6. Self-Extraction Methods

These methods use the self-extracting techniques and circuits to extract the value of threshold voltage. Couple of methods under this category are briefly discussed below.

6.1. HSPICE Command Extraction Method

A substantially enhanced HSPICE feature that extracts MOSFET threshold voltage (V_{TH}) based on the constant-current definition universally adopted by fabrication labs to measure, specify, and monitor V_{TH} . Introduced in the 2009.09 release, HSPICE simulations compute constant-current V_{TH} the exact same way V_{TH} is measured in the fab [35] [36].

For extracting V_{TH} , the “.OPTION IVTH” command is available. This .OPTION IVTH feature is supported for Levels 54 (BSIM4), 69 (PSP100), and 70 (BSIMSOI4) MOSFET models along with latest PTM nano-MOSFET models. It shows acceptable results. This command extracts V_{TH} using CCM and eliminates the use of $I_{DCRITICAL}$. LX142 model accessible in HSPICE, presents the output results as V_{TH} . Therefore, for short channel devices this process appears effectual in extracting V_{TH} and also shows compatibility with the existing transistor models.

The HSPICE Command “.OPTION IVTH” was implemented on the test device. LX142 model accessible in HSPICE, presents the output results as V_{TH} .

The outcome of the result was as follows:

$$V_{TLIN} = 0.30 \text{ V at } V_{DS} = 0.1 \text{ V}$$

$$V_{TSAT} = 0.19 \text{ V at } V_{DS} = 0.9 \text{ V}.$$

6.2. Automatic Threshold Voltage Extractor Circuit (ATEC) Method

This proposed ATEC method implements the most popular industrial extraction algorithm (LEM) of biasing a saturated MOSFET to the linear portion of its $\sqrt{I_D}$ versus V_{GS} characteristics and extrapolating the tangential line to V_{GS} axis [37] [38]. The circuit accomplishes both the tasks automatically in continuous time irrespective of dimensions and technology of device under test. A simple feedback loop utilizing a Differential Difference Amplifier (DDA) achieves auto biasing, while another DDA computes the extrapolated value. The circuit is valid for both PMOS and NMOS devices and is able to forecast the value of V_{TH} using the proposed logic. Conceptual Schematic of ATEC is shown in **Figure 24**.

Few other similar ATEC designs with different implementation logics are also proposed to extract the V_{TH} .

Implementation of ATEC Method on Test Device

The technique was implemented on the test device. The bulk driven 10 nm nano-NMOS model was used to simulate the circuit. The test device is made to work in linear region. Hence the outcome will be the threshold voltage in linear region (V_{TLIN}). The transient analysis of the circuit gave the following results as shown in **Figure 25**.

$$V_{TLIN} = 0.61 \text{ V for } V_{DD} = -V_{SS} = 0.9 \text{ V}.$$

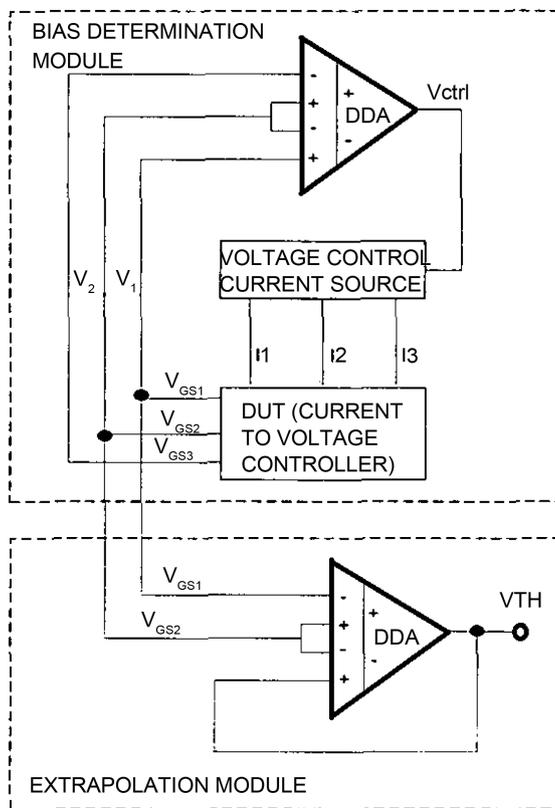


Figure 24. Conceptual schematic of ATEC method.

7. Deviation Based Extraction Methods

Under this grouping, the V_{TH} is extracted by determining either the deviation of the value or the difference between the measured values. Couple of methods using this logic are listed in this category and are briefly discussed below [39].

7.1. Match-Point (MP) Method

Match-Point method was proposed in 1990 by B. El-Kareh and co-workers. This scheme subjectively evaluates V_{TH} at the value of V_{GS} at which the exponential sub-threshold current semi-log extrapolation diverges by 5% from the measured I_D .

This MP method exaggerates the weak inversion region neglecting strong inversion. **Figure 26** and **Figure 27** present the application of this method to the linear region

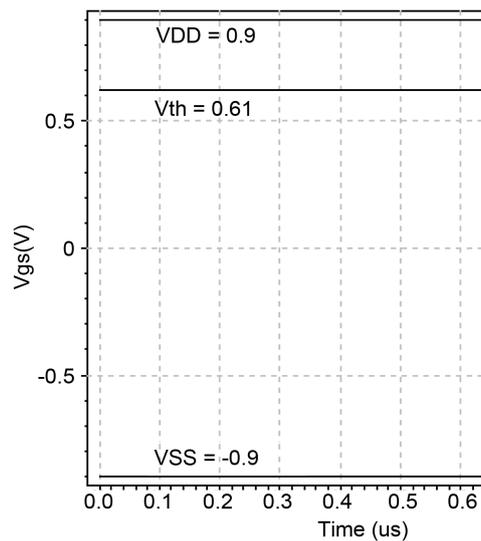


Figure 25. Extraction of V_{TH} using ATEC for $V_{DD} = -V_{SS} = 0.9$ V.

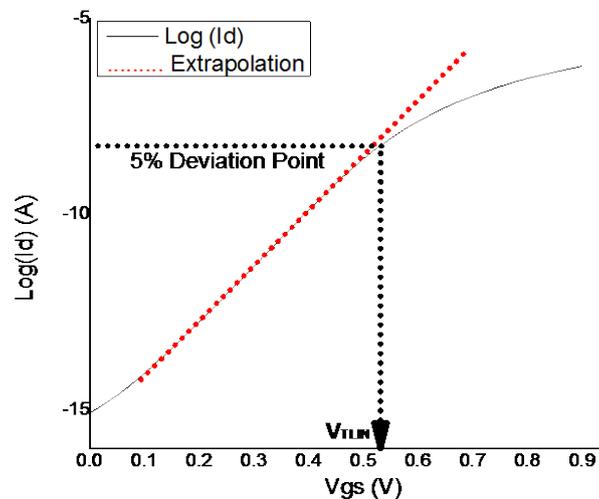


Figure 26. Extraction of V_{TLIN} using MP for $V_{DS} = 0.1$ V.

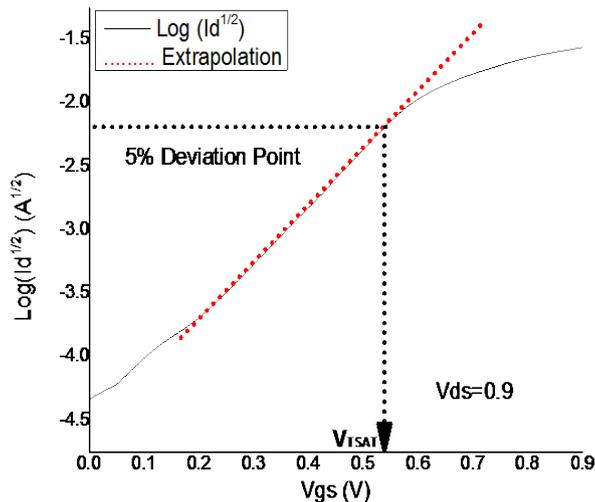


Figure 27. Extraction of V_{TSAT} using MP for $V_{DS} = 0.9$ V.

and saturation region our test device producing an apparent V_{TH} value V_{TLIN} of 0.51 V and V_{TSAT} of 0.52 V respectively. Of course, diverse values of V_{TH} could be arbitrarily achieved by defining the deviation of the extrapolation at threshold at other values different from 5%. The shape of the semi-log curve may be swayed by the presence of parasitic resistance and other SCEs. This method is seldom used as it is more laborious and time consuming.

Implementation of MP Method on Test Device

The technique was implemented on the test device. Generally Match Point method is used to calculate threshold Values by plotting I_D versus V_{GS} curve with low biased drain terminal. Hence outcome is V_{TLIN} . The results are extracted by using the semilog plot. We propose to calculate V_{TSAT} by plotting $\sqrt{I_D}$ versus V_{GS} and applying the same 5% deviation logic of Match point method. It was observed that V_{TLIN} value was lower than V_{TSAT} value which is generally unusual.

The outcome of the result was as follows:

$$V_{TLIN} = 0.51 \text{ V at } V_{DS} = 0.1 \text{ V}$$

$$V_{TSAT} = 0.52 \text{ V at } V_{DS} = 0.9 \text{ V .}$$

7.2. Vin-Vout Difference (VVD) Method

In this VVD method, a new interpretation of the threshold voltage is presented as [40]:

$$V_{TH} = V_{in} - V_{out} \tag{13}$$

The method is implemented by performing the transient analysis on the testing device. In other words, it states that V_{TH} can be extracted by the voltage difference between the constant V_G and V_S at the normalized current in the I_D - V_S curves. As seen in Figure 28, the circuitry of VVD and the extraction method is straightforward and can be easily applicable in measurement apparatus [27].

Implementation of VVD Method on Test Device

The technique was implemented on the test device. Figure 29 represents the transient

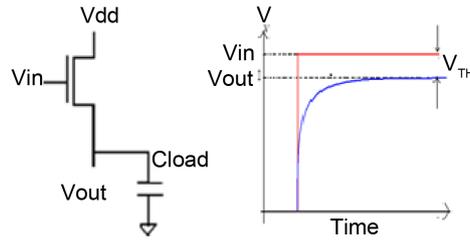


Figure 28. The proposed VVD circuit and the expected output to extract V_{TH} .

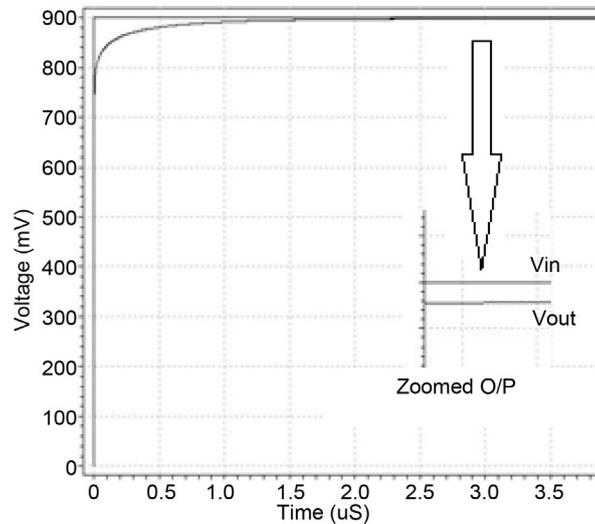


Figure 29. Transient analysis of VVD for $V_{in} = 0.9$ V.

results of the VVD circuit. The circuit was compiled and simulated using SPICE. The circuit was analysed using predictive technology model (PTM) at 10-nm, 16-nm, 22-nm, 32-nm, and 45-nm technology node. The input gate voltage was set as 0.9 V. The Vdd was given as constant DC supply of 0.9 V. The multiple values of Load Capacitances (Cload) were used for the testing purpose, however, the V_{TH} extraction results had negligible effect of the variations in the value. Transient analyses were performed on the compiled circuit to extract the threshold voltage value.

The outcome of the result was as follows:

$$V_{TSAT} = 0.003 \text{ V at } V_{IN} = 0.9 \text{ V and } V_{DD} = 0.9 \text{ V.}$$

The transient results gave the V_{out} value marginally equal to V_{in} , slightly a bit millivolts lower than V_{in} . Hence, as per the above mentioned logic of the referred extraction method, the calculated V_{TH} is a very small value in millivolts which was not in accord with other extraction method outcomes. The extracted threshold voltage value also seems to be unrealistic. Hence we can accomplish that the VVD extraction method is considerably ineffective at nano-meter technology node.

8. Hybrid Extraction (HEM) Methods

Under this category, the HEM process uses multiple recognized schemes to extract V_{TH}

and combines the advantage of each. One of the hybrid extraction methods is explained below [34].

This Hybrid extraction method overwhelms the constraints of above mentioned extraction techniques and compute V_{TH} for all values of V_{DS} . It syndicates both methods namely CCM and LEM mentioned beforehand to appropriately extract the V_{TH} . Additionally, this method is also unaffected by the arbitrary value of $I_{DCRITICAL}$. For valuation of V_{TH} using this method first the value of V_{TH} for low biased V_{DS} is attained using LEM (see Figure 30). Subsequently, $I_{DCRITICAL}$ is determined using CCM as mentioned above. Further, for higher value of V_{DS} , V_{TH} is defined as the gate voltage at I_D for pre-calculated $I_{DCRITICAL}$ value. However, the extracted value of V_{TH} is not constant as the dependence of g_m on other process parameters is not modelled accurately.

Implementation of Hybrid Extraction Method on Test Device

The HEM technique was implemented on the test device. V_{TLIN} was calculated using LEM for I_D versus V_{GS} graph with low biased V_{DS} , and correspondingly the $I_{DCRITICAL}$ was also evaluated. Furthermore, I_D versus V_{GS} graph is plotted with high biased V_{DS} . Implementing the CCM technique on the plot by using the pre-calculated $I_{DCRITICAL}$, we are able to calculate V_{TSAT} . Hence we are able to extract V_{TLIN} and V_{TSAT} using Hybrid extraction method as seen in Figure 30.

The outcome of the result was as follows:

$$V_{TLIN} = 0.67 \text{ V at } V_{DS} = 0.1 \text{ V}$$

$$V_{TSAT} = 0.55 \text{ V at } V_{DS} = 0.9 \text{ V .}$$

9. Compiled Simulation Results

All the predefined threshold voltage extraction methods were investigated and implemented at 10-nm Technology node and other sub 45-nm technology node. All the results are verified by extensive 2-D TCAD simulation and confirmed analytically. Various predictive technology models developed by the Nanoscale Integrations and Modeling (NIMO) Group at Arizona State University (ASU) were used to illustrate the characteristics of nano-MOSFETs. The models possess the competency to support short

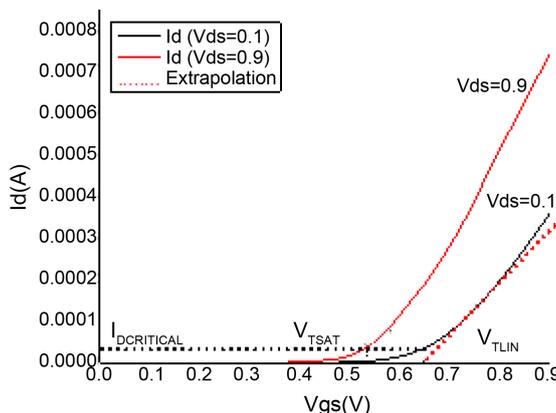


Figure 30. Extraction of V_{TLIN} and V_{TSAT} using hybrid method for $V_{DS} = 0.1 \text{ V}$ and $V_{DS} = 0.9 \text{ V}$.

channel effects, the gate leakage effects and various other second order effects to predict the realistic output. **Table 1** presents a comparative result of largely applied threshold extraction methods for bulk driven nano-MOSFETs various sub 45-nm technology nodes. The V_{TH} was analysed using predictive technology model (PTM) for bulk driven nano-mosfet at 10-nm, 16-nm, 22-nm, 32-nm and 45-nm technology node.

The results are tabulated in **Table 1**. Accuracy can be enhanced by considering more number of measured points.

10. Application of V_{TH} Extraction Methods to Implement Noise Analysis

Noise analysis of the Resistive load Inverter were performed using various V_{TH} extraction method values. Resistive load inverter is one of the most fundamental circuits of MOS family. It characterizes the basic operation of all static gates. With Load resistor (R_L) in series with driver NMOS transistor, it has one input connected to the gate of NMOS and one output port connected to the drain terminal of the NMOS as shown in **Figure 31**. The Inverter Threshold Voltage V_{TH} (inverter) is the value where output voltage is equal to input voltage.

Noise margin is the limit of noise that a circuit can endure without compromising the operation of circuit. It assures that logic "1" with finite noise added to it, is still recognized as logic "1" and not logic "0" and vice versa. It is principally the difference between

Table 1. V_{TH} extraction using defined methods for different technology node.

METHOD	10-nm TN		16-nm TN		22-nm TN		32-nm TN		45-nm TN	
	V_{TLIN}	V_{TSAT}								
CCM	0.355	0.104	0.463	0.369	0.479	0.425	0.440	0.396	0.433	0.403
DDEM	0.44	N.A	0.45	N.A	0.47	N.A	0.46	N.A	0.45	N.A
LEM	0.683	N.A	0.719	N.A	0.706	N.A	0.653	N.A	0.634	N.A
QEM	N.A	0.381	N.A	0.535	N.A	0.564	N.A	0.526	N.A	0.522
SDM	0.675	0.437	0.7	0.6	0.675	0.6	0.649	0.552	0.626	0.578
TDM	0.559	0.363	0.65	0.504	0.65	0.525	0.595	0.5	0.578	0.5
GM	0.59	0.51	0.645	0.575	0.645	0.56	0.6	0.525	0.6	0.5
TCRM	0.65	0.5	0.675	0.6	0.675	0.625	0.625	0.6	0.6	0.575
TM	0.645	0.5	0.65	0.575	0.675	0.575	0.625	0.525	0.6	0.513
NMID	0.625	0.65	0.625	0.65	0.625	0.65	0.6	0.625	0.575	0.6
NRHM	0.625	0.65	0.65	0.675	0.65	0.675	0.6	0.625	0.575	0.6
RHM	0.675	0.675	0.7	0.725	0.725	0.725	0.675	0.7	0.65	0.675
SPICE	0.30	0.19	0.34	0.23	0.42	0.37	0.43	0.38	0.43	0.40
ATEC	0.61	N.A	0.63	N.A	0.63	N.A	0.62	N.A	0.61	N.A
MPM	0.7	0.55	0.7	0.625	0.7	0.675	0.65	0.675	0.65	0.675
VVD	N.A	0.003								
HEM	0.67	0.55	0.675	0.6	0.67	0.61	0.61	0.56	0.58	0.56

signal and Noise value. Logically, the reference terms related Noise Margin analysis are described as below (Ref. **Figure 32**).

- V_{OH} : (Voltage Output High Value). $V_{OH} = V_{dd}$ because when the input voltage drops below V_{TH} of the inverter, no current flows. No current flow in turn means no voltage drop across the load resistor and $V_{OUT} = V_{dd} = V_{OH}$.
- V_{OL} : (Voltage Output Low Value). If the input is driven to $V_{OL} = V_{dd}$, then the driver NMOS transistor is "ON" and since $(V_{gs} - V_t) > V_{ds}$, it is operating in linear mode. The V_{OUT} will be at V_{OL} and the V_{IN} will be at V_{OH} .
- V_{IH} : (Voltage Input High Value). When $V_{IN} = V_{IH}$, the output is at V_{OL} and the NMOS is in the linear region.
- V_{IL} : (Voltage Input Low Value). To determine noise margin we need V_{IL} which is one of two points where we have unity gain. When input low, output high and NMOS in saturation.

10.1. Introduction

Considering the output characteristics of a resistive load inverter; the threshold voltage of the NMOS (V_{TH}) plays a significant role in determining the shape of the voltage transfer characteristic (V_{TC}) of a resistive load inverter. The V_{TH} appears as a critical parameter in expressions for V_{OL} , V_{IL} , and V_{IH} . V_{OH} is determined primarily by the power

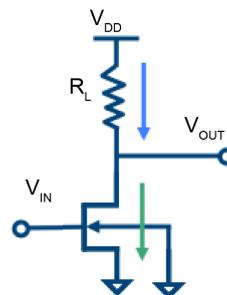


Figure 31. General circuit diagram of resistive load inverter.

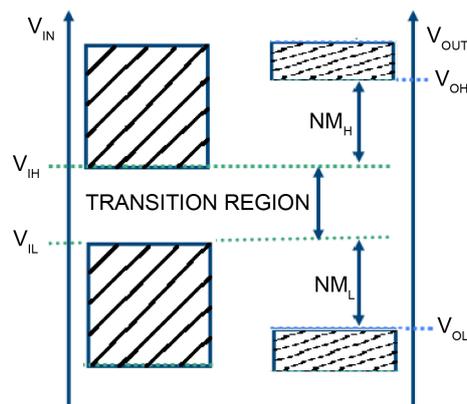


Figure 32. Representation of noise immunity and noise margins of resistive load inverter.

supply voltage V_{dd} . The adjustment of V_{OL} receives primarily attention than V_{IL} , V_{IH} . Larger V_{TH} results in smaller V_{OL} resulting in larger transition slope and higher voltage swing as it can be perceived through **Figure 33**.

10.2. Noise Margin Analysis of Inverter for Diverse Values of Driver NMOS Threshold (V_{TH})

Ideally, when input voltage is logic “1”, the output voltage is expected to be at logic “0”. Hence, V_{IH} is V_{dd} , and V_{OL} is 0 V as shown in **Figure 34**. Alternatively, when input voltage is logic “0”, output voltage is supposed to be at logic “1”. Hence, V_{IL} is 0 V, and V_{OH} is V_{dd} . Using the values, the Noise Margins for an ideal inverter could be defined as follows:

- NM_L (Noise Margin Low) = $V_{IL} - V_{OL} = 0 - 0 = 0$ V
- NM_H (Noise Margin High) = $V_{OH} - V_{IH} = V_{dd} - V_{dd} = 0$ V

Practically the situation is not identical. It is observed that due to number of secondary effects like voltage droop, ground bounce, internal resistances, practices, etc.; V_{OH} is slightly less than V_{dd} *i.e.* V'_{dd} , whereas V_{OL} is slightly higher than V_{ss} *i.e.* V'_{ss} as shown in **Figure 33**. Hence Noise margins for a practical circuit can be defined as follows:

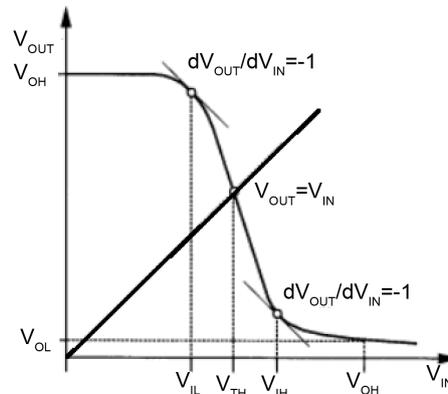


Figure 33. Typical VTC of a resistive load inverter.

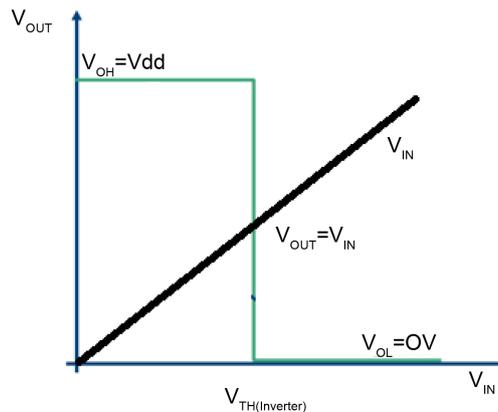


Figure 34. VTC of an ideal resistive load inverter.

- NM_L (Noise Margin Low) = $V_{IL} - V_{OL} = V_{ss} - V'_{ss} = \Delta V_{ss}$;
- NM_H (Noise Margin High) = $V_{OH} - V_{IH} = V'_{dd} - V_{dd} = \Delta V_{dd}$.

Hence, if input voltage (V_{IN}) lies somewhere between V_{OL} and V_{IL} , it would be detected as logic “0”, and would result in an output which is acceptable. Similarly, if input voltage (V_{IN}) lies between V_{IH} and V_{OH} , it would be detected as logic “1” and would result in an output which is acceptable.

10.3. Statistical Inference

Application of the extraction methods were implemented to calculate the Noise Immunity and Noise Margins for Resistive Load Inverter using 10-nm test device with Load Resistance $R_L = 100 \Omega$ and $V_{dd} = 1 V$. Referring to **Table 2**, we can infer number of facts and properties that can be extracted from noise margin analysis regarding various threshold extraction methods.

- We observe that with the increase in the Threshold voltage extraction value, the NM_H decreases and NM_L increases. For an Ideal Inverter, Noise Margins should be equal. Using QEM method for V_{TH} extraction, we obtain the most optimistic results ($NM_H \approx NM_L$) in this regards. (Ref. **Figure 35** and **Figure 36**).
- Using “.OPTION IVTH” command accessible in SPICE extraction method for V_{TH} extraction, we obtain the maximum output voltage swing *i.e.* $V_{OH} - V_{OL}$ for resistive load NMOS inverter (Ref. **Figure 37**).
- In the well-designed inverter, the Threshold value of the circuit ($V_{in} = V_{out}$) is nearly equal to $V_{dd}/2$. We obtain the flawless results in this regards using CCM extraction method (Ref. **Figure 38**).

Table 2. Noise immunity and noise margins for resistive load inverter using 10-nm test device.

METHOD	V_{TH}	NM_H	NM_L	$\Delta V_{out} (V_{OH}-V_{OL})$	$\Delta NM NM_H-NM_L $	$V_{TH}(Inverter) (V_{in} = V_{out})$
CCM	0.355	0.4325	0.3440	0.9687	0.0885	0.498
DDEM	0.44	0.3475	0.4242	0.9638	0.0767	0.572
LEM	0.683	0.1045	0.6364	0.9331	0.5319	0.779
QEM	0.381	0.4065	0.3687	0.9674	0.0378	0.521
SDM	0.675	0.1125	0.6303	0.935	0.5178	0.771
TDM	0.559	0.2285	0.5329	0.9536	0.3044	0.675
GM	0.59	0.1975	0.5602	0.9498	0.3627	0.701
TCRM	0.65	0.1375	0.6106	0.9403	0.4731	0.751
TM	0.645	0.1425	0.6066	0.9412	0.4641	0.746
NMID	0.625	0.1625	0.5900	0.9447	0.4275	0.73
NRHM	0.625	0.1625	0.5900	0.9447	0.4275	0.73
RHM	0.675	0.1125	0.6303	0.935	0.5178	0.771
SPICE	0.30	0.4875	0.2915	0.9712	0.196	0.449
ATEC	0.61	0.1775	0.5774	0.947	0.3999	0.718
MPM	0.7	0.0875	0.6489	0.9286	0.5614	0.793
HEM	0.67	0.1175	0.6265	0.9362	0.509	0.767

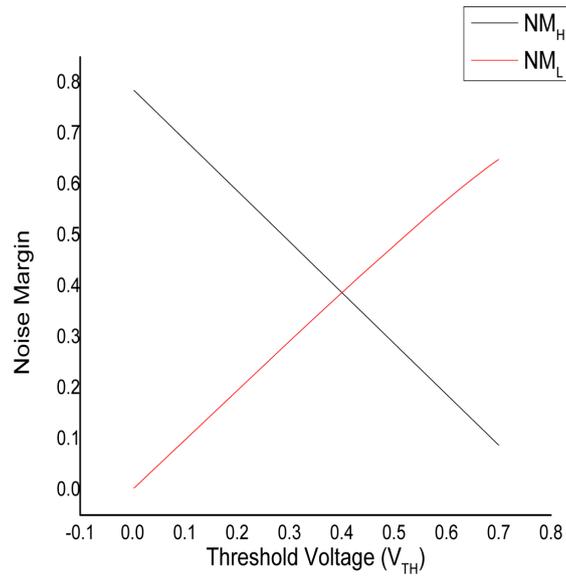


Figure 35. Noise margin variations vs. driver NMOS threshold values (V_{TH}).

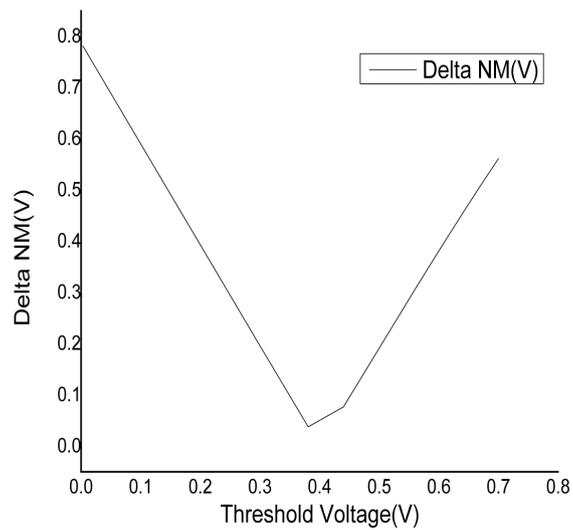


Figure 36. Plotting the $|NM_H - NM_L|$ vs. driver NMOS threshold voltage (V_{TH}).

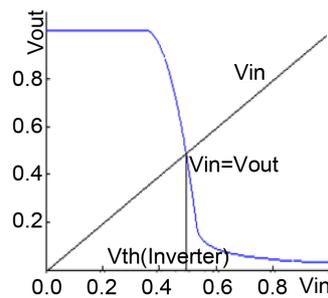


Figure 37. VTC of resistive load inverter vs. driver NMOS ($V_{TH} = 0.3 \text{ V}$) and $R_L = 100 \Omega$.

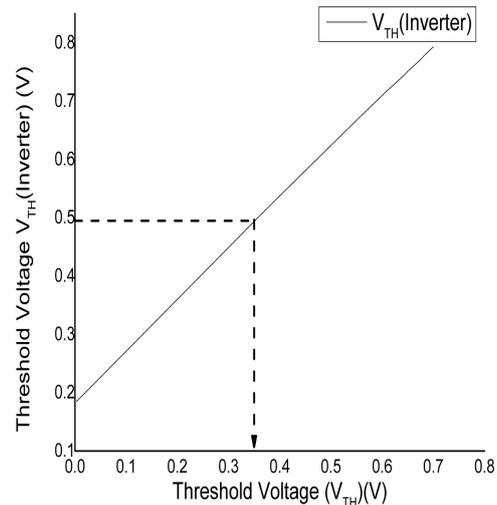


Figure 38. Inverter threshold $V_{TH}(\text{Inverter})$ vs. driver NMOS threshold voltage (V_{TH}).

- The slope of the output curve within the transition region describes the propagation delay properties of the circuit. The variation in the V_{TH} had a negligible effect on the slope of the curve resulting in nearly persistent switching characteristics for most of the extraction methods.

11. Conclusion

We presented, reviewed and critically compared several extraction methods currently used to determine the threshold voltage of bulk driven MOSFETs at 10-nm technology node and other various sub 45-nm technology nodes for precise evaluation of the respective method. The relative performance of all the methods was illustrated and compared under similar conditions by applying them to the test devices: bulk driven nano-MOSFETs with 10-nm technology node along with other various sub 45-nm technology nodes. We can perceive that the extracted threshold voltage largely depends on the method used for extraction specifically at nano-scale. The CCM has an ambiguous definition on the critical drain current (I_{D0}) contingent on technology being used. The LEM, QEM and TM outcomes are affected by extrinsic resistance effects, mobility degradation, Short Channel Effects and other second order present effects. SD, TD, GM, RH and TCRM are also widely affected by noise and are also not based on ideal threshold voltage definition condition. The MP is seldom used as 5% deviation value gives an ambiguous definition of threshold. The VVD extraction method is considerably ineffective at nano-meter technology node. In NMID and NRH, the correct calculation of maxima in wide ranges makes the extraction task much more difficult. We can also infer number of facts and properties from noise margin analysis performed using various threshold extraction methods. QEM provides the most optimistic balanced noise margin results. The maximum output voltage swing was observed using SPICE extraction method. CCM delivers the most appropriate results in calculating Threshold value of the circuit. The above listed features and properties of various extraction me-

thods can be helpful in merging the threshold voltage compact models at nano-level technology nodes.

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