

Current-Controlled CFTA Based Fractional Order Quadrature Oscillators

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Abstract

This paper presents a study of fractional order quadrature oscillators based on current-controlled current follower transconductance amplifiers (CCCFTA). The design realisation and performance of the fractional order quadrature oscillators have been presented. The quadrature oscillators are constructed using three fractional capacitors of orders $\alpha = 0.5$. The fractional capacitor is not available on the market or in the PSPICE program. Fortunately, the fractional capacitor can be realised by using the approximate method for the RC ladder network approximation. The oscillation frequency and oscillation condition can be electronically/orthogonally controlled via input bias currents. Due to high-output impedances, the proposed circuit enables easy cascading in current-mode (CM). The PSPICE simulation results are depicted, and the given results agree well with the anticipated theoretical outcomes.

Keywords

Fractional Order, Quadrature Oscillator, Current-Controlled Current Follower Transconductance Amplifier

1. Introduction

Fractional calculus, the branch of mathematics that addresses non-integer order differentiation and integration, is a field that is over 300 years old. Fractional calculus gained considerable attention in the late sixties because it provides a more accurate description of real objects, and many structures found in nature can be modelled by fractals [1]. Fractional calculus addresses the generalization of differentiation and integration of non-integer orders. The rapid growth of the application of fractional calculus to the fields of science and engineering is noteworthy. The integer-order models have been used for a long time, not because they were more accurate or better, but because of

their ability to solve fractional differential equations [2]. This issue has changed over the past few years as several methods of fractional derivative and integral approximation have been developed [3] [4] [5]; therefore, fractional calculus can be used to easily model a wide area of applications. Fractional calculus plays a major role in physics [6] [7], control systems [8] [9] [10], signal processing [11], and electrical engineering [12]-[17].

Traditional differentiation takes the form $(d^n/dt^n)f(t)$, where n is an integer; however, using fractional calculus, the value of n can be a non-integer order, such as 1.1, $\sqrt{2}$ or any other real or imaginary order. The Riemann-Liouville definition [18] [19] [20] of a fractional derivative, where $n-1 < \alpha < n$, is defined as:

$$\frac{d^\alpha}{dt^\alpha} f(t) \equiv D^\alpha f(t) = \frac{d^\alpha}{dt^\alpha} \left[\frac{1}{\Gamma(n-\alpha)} \int_0^t \frac{f(\tau)}{(t-\tau)^{\alpha-n+1}} d\tau \right], \quad (1)$$

and the definition of a fractional integral, where $0 < \alpha < 1$, is given as:

$$D^{-\alpha} f(t) = \frac{1}{\Gamma(\alpha)} \int_0^t \frac{f(\tau)}{(t-\tau)^{1-\alpha}} d\tau. \quad (2)$$

where $\Gamma(\cdot)$ is the gamma function. One of the most frequently used definitions for the general fractional derivatives is the Caputo definition, which can be expressed as follows [21]:

$$D_0^\alpha f(t) = \frac{1}{\Gamma(m-\alpha)} \int_{t_0}^t f^{(m)}(u)(t-u)^{m-\alpha-1} du. \quad (3)$$

where m is an integer, such that $(m-1) < \alpha < m$. The Laplace transform is a very useful tool in the design and analysis of electronic circuits, transforming the circuit from the time domain to the frequency domain. This transformation is particularly useful because it allows for the analysis of circuits using algebraic rather than differential equations. The Laplace transform of (3) under zero initial conditions is given by [16]:

$$\mathcal{L}\{D_0^\alpha f(t)\} = s^\alpha F(s). \quad (4)$$

where s^α is the fractional Laplacian operator. The use of the fractional Laplacian operator allows for the design and analysis of systems using concepts from fractional calculus without having to solve the difficult time domain representations.

During the past decades, the current-mode (CM) approach has become more popular in analogue integrated circuit design due to its advantages of providing a larger dynamic range, wider bandwidth, and lower power consumption over its voltage-mode counterparts [22]. Several active CM blocks are proposed for active filters, oscillators and immittance circuit design. The CM realization of oscillators and filters using the first generation of current conveyor (CCI), the second generation of current conveyor (CCII), and many other active blocks has been reported [23]-[28]. However, a large number of passive resistors are inevitably used in these circuits (except for the resistors that support linear capacitors), which are not suitable for monolithic integration [29]. In 2009, Herencsar *et al.* [30] introduced a modification of the CFTA, called the cur-

rent-controlled current follower transconductance amplifier (CCCFTA), in which the parasitic resistance at the input terminal is electronically tuned. The CCCFTA can be used as an active block in an analogue circuit design with a minimum number of resistors.

Sinusoidal oscillators are widely used in various applications, such as communication, instrumentation, measurement and signal processing. Particularly in communication systems, the sinusoidal oscillator is frequently used to generate the carrier signal for the modulation system [31] [32] [33] [34], such as AM, FM, and ASK. With the use of the fractional elements, the design equations of the well-known oscillators could be generalized from the tight integer order domain to the general fractional order domain.

In this paper, a study of a generalized fractional order CCCFTA-based oscillator circuit is introduced. The general CO and FO for this oscillator are derived with the use of the RC ladder network.

2. Fractional Capacitor

A realization using Carlson's method [15] was selected to model the fractional capacitors. The approximation of the fractional capacitors $(1/s)^{1/n}$ was conducted using a regular Newton process. The order of these approximations increases as the number of iterations in the Newton process increases. The function used in the regular Newton process for these approximations is:

$$F(x) = x \frac{(n-1)x^n + (n+1)(1/s)}{(n+1)x^n + (n-1)(1/s)} \quad (5)$$

where x is the previous iteration. Using this process to approximate a fractional capacitor when $n = 2$ or $\alpha = 0.5$, the initial assumption $x_0 = 1$ yields:

$$x_1 = \frac{s+3}{3s+1} \quad (6)$$

as the first iteration approximating $\sqrt{1/s}$. The second iteration approximating $\sqrt{1/s}$ is:

$$x_2 = \frac{s^4 + 36s^3 + 126s^2 + 84s + 9}{9s^4 + 84s^3 + 126s^2 + 36s + 1} \quad (7)$$

The magnitude response of this approximation is provided in **Figure 1**, which creates an approximation of the fractional capacitor centred around the angular frequency 1 rad/s. Using the approximation of (7), the fractional Laplacian operator can be physically realized using the RC ladder network shown in **Figure 2**. The impedance of this RC ladder network is:

$$Z_{in} = R_1 + \frac{1/C_1}{s + \frac{1}{R_2 C_1}} + \frac{1/C_2}{s + \frac{1}{R_3 C_2}} + \frac{1/C_3}{s + \frac{1}{R_4 C_3}} + \frac{1/C_4}{s + \frac{1}{R_5 C_4}} \quad (8)$$

The resistor and capacitor values for the RC ladder shown in **Figure 2** can be determined by equating the terms of (7) after a CFE of (8), which, after the CFE, becomes [35] [36] [37]:

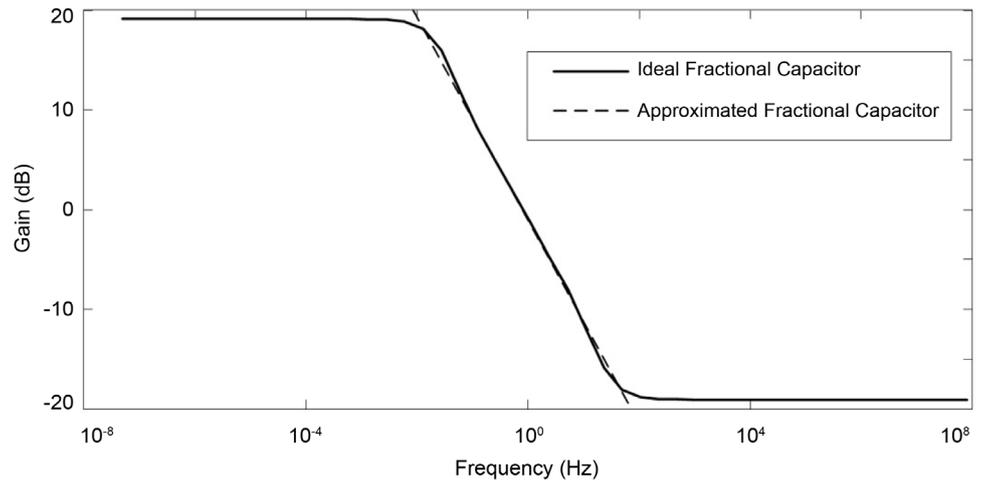


Figure 1. Magnitude response of the approximated fractional capacitor compared to the ideal fractional capacitor of impedance $Z(s) = 1/s^{0.5}$.

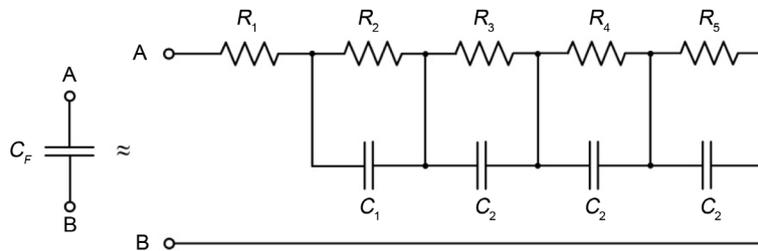


Figure 2. Approximated model for the fractional capacitor.

$$\frac{1}{s^{0.5}} \approx \frac{1}{9} + \frac{0.2291313787}{s + 0.03109120413} + \frac{0.2962962975}{s + 0.3333333333} + \frac{1.899696037}{s + 7.548632170} + \frac{0.5378392488}{s + 1.420276625} \tag{9}$$

Then an approximate CFE with any desired capacitance (C), which is centred around any angular frequency (ω_c), by applying magnitude and frequency scaling factors to the component values in the ladder realization. The resistor and capacitor values become:

$$R_s = Rk_m \tag{10}$$

$$C_s = \frac{C}{k_f k_m} \tag{11}$$

where R_s and C_s are the scaled resistor and capacitor values, respectively; R and C are the unscaled resistor and capacitor values, respectively; and $k_m = 1/C\omega_c^{1/n}$ is the frequency scaling factor.

The values of the resistors and capacitors used in the PSPICE simulations of the fractional order quadrature oscillators with the approximated fractional capacitors are provided in **Table 1**. The phase and magnitude response of the fabricated two-terminal FO capacitors are compared with the conventional capacitor, which is simulated using PSPICE and is shown in **Figure 3**. These values realize the approximated fractional capacitor of 40 pF with $\alpha = 0.5$ centred around a frequency of 1 MHz.

3. Description of the CCCFTA

The schematic symbol and the equivalent circuit of the current-controlled current follower transconductance amplifier (CCCFTA) [30] are shown in **Figure 4**. The properties

Table 1. Component values to realize approximated fractional capacitor of 40 pF using RC ladder.

Component	Values
R_1	1.107 MΩ
R_2	8.864 MΩ
R_3	73.499 MΩ
R_4	2.509 MΩ
R_5	3.77 MΩ
C_1	0.054 pF
C_2	0.069 pF
C_3	0.008 pF
C_4	0.029 pF

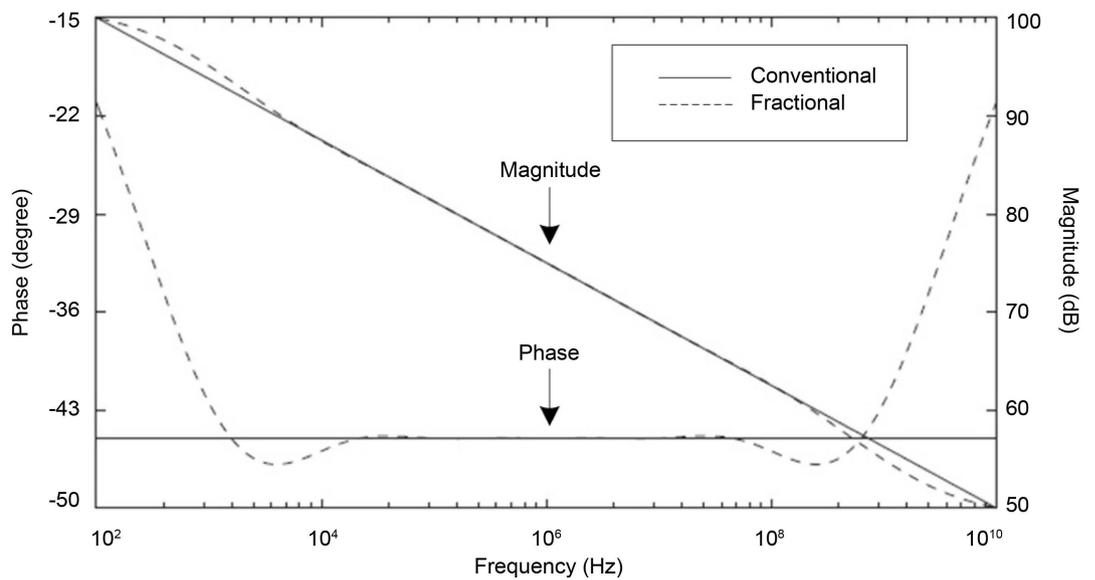


Figure 3. Phase and magnitude of the fractional capacitors compared with the conventional capacitor.

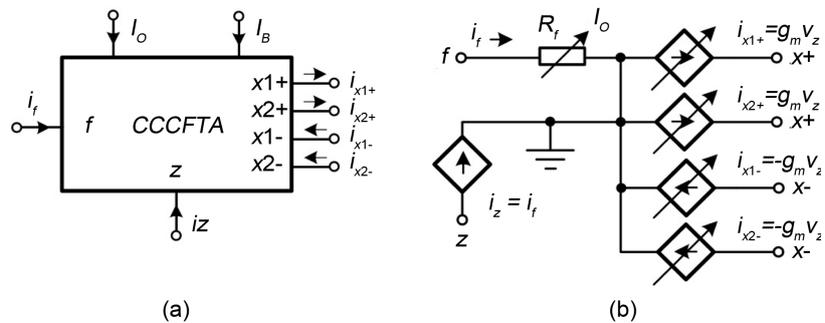


Figure 4. CCCFTA (a) schematic symbol and (b) equivalent circuit.

of the CCCFTA are similar to the conventional CFTA except that the input voltage of CCCFTA is not zero, and the CCCFTA has a finite input parasitic resistance R_f at the f input terminal, which can be controlled by the bias current I_o as shown below. The characteristics of the ideal CCCFTA are represented by the following hybrid matrix.

$$\begin{bmatrix} v_f \\ i_z \\ i_{x1+} \\ i_{x2+} \\ i_{x1-} \\ i_{x2-} \end{bmatrix} = \begin{bmatrix} R_f & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & +g_m \\ 0 & 0 & +g_m \\ 0 & 0 & -g_m \\ 0 & 0 & -g_m \end{bmatrix} \begin{bmatrix} i_f \\ 1 \\ v_z \end{bmatrix} \tag{12}$$

The CMOS 0.18 μm implementation based on the second generation current controlled conveyor (CCCII) with a grounded y terminal and a balanced output operational transconductance amplifier (BOTA) [38] is shown in Figure 5. The dimensions of the transistors are shown in Table 2. The DC power supply voltages are equal to ± 0.8 V. All transistors operate in the saturation region. For CMOS CCCFTA, the R_f and g_{mmi} are written as:

$$R_f = \frac{1}{g_{mm2} + g_{mm4}}, g_{mmi} = \sqrt{2I_o\mu_0C_{OX}(W/L)_i} \tag{13}$$

where g_{mmi} ($i = 2, 4$) are the transconductances of transistors M_2 and M_4 , forming the f stage. In (13), the current I_o is used to adjust the R_f ; μ_0 is the free electron mobility

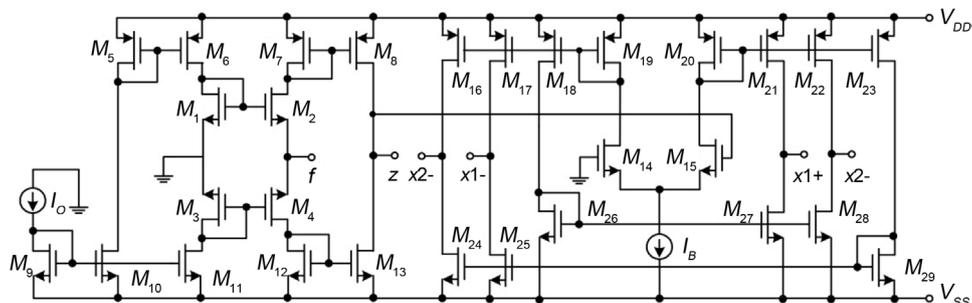


Figure 5. CMOS internal structure of CCCFTA.

Table 2. Scaling of MOS transistor dimensions.

Transistors	$W(\mu\text{m})/L(\mu\text{m})$
<i>NMOS</i>	
M_1, M_2	5/2
M_{14}, M_{15}	1.5/0.4
$M_{16} - M_{23}$	5/0.5
<i>PMOS</i>	
M_3, M_4	5/2
$M_5 - M_8$	5/0.18
$M_9 - M_{13}, M_{24} - M_{29}$	5/0.5

in the channel; C_{OX} is the gate oxide capacitance per unit area; and W and L are the channel width and length, respectively. Similarly, the transconductances g_m of CCCFTA can be given by:

$$g_m = \sqrt{I_B \mu_0 C_{OX} (W/L)}. \tag{14}$$

where the current I_B is used to control the transconductance g_m .

4. CCCFTA Based Fractional Order Quadrature Oscillators

The proposed fractional order quadrature oscillator is shown in **Figure 6**. Because the parasitic resistance of the f terminal of CCCFTA is used as an active resistor in this circuit, this fractional order quadrature oscillator only consists of two CCCFTAs and three fractional capacitors.

Using Equation (12), a routine analysis of the circuit yields the following characteristic equation:

$$s^{\alpha_1+\alpha_2+\alpha_3} R_{f1} C_{F1} C_{F2} C_{F3} + s^{\alpha_1+\alpha_2} C_{F1} C_{F2} + s^{\alpha_2} g_{m1} C_{F2} + g_{m1} g_{m2} = 0, \tag{15}$$

From Equation (15), the CO and FO can be expressed as:

$$C_{F2} = g_{m2} R_{f1} C_{F3}, \tag{16}$$

$$\omega_o = \sqrt{\frac{g_{m1}}{R_{f1} C_{F1} C_{F3}}}, \tag{17}$$

Moreover, because of the multiple-output CCCFTAs, the circuit can provide two inverted output currents, i_{out2} and i_{out4} . Thus, the relationship of all of the output currents can be expressed as:

$$\begin{aligned} i_{out1} &= -i_{out2} \\ i_{out3} &= -i_{out4} \end{aligned} \tag{18}$$

The circuit provides four phase quadrature outputs of equal magnitudes.

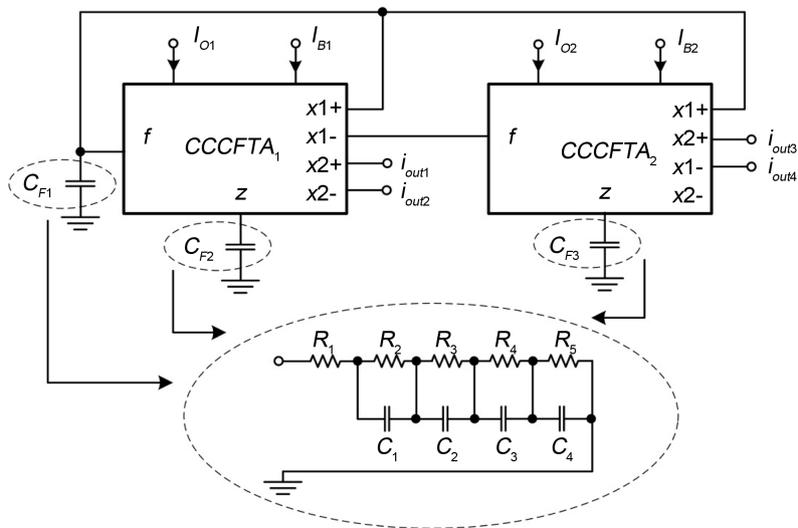


Figure 6. Proposed fractional order quadrature oscillator employing CCCFTAs.

5. Simulation Results

The CCCFTA is realized in **Figure 5**, and the performance of the proposed circuits is verified using PSPICE with a standard chartered 0.18 μm TSMC CMOS process. The bias currents of CCCFTA₁ and CCCFTA₂ are $I_{O1} = I_{O2} = 300 \mu\text{A}$ and $I_{B1} = I_{B2} = 1 \text{mA}$, respectively. Some cases are chosen to be simulated to show the reliability of the proposed design.

For case 1 ($\alpha_1 = \alpha_2 = \alpha_3 = 1$), the simulation parameters chosen are $C_{F1} = C_{F2} = C_{F3} = 40 \text{pF}$. **Figure 7** is the simulated quadrature outputs i_{out1} , i_{out2} , i_{out3} and i_{out4} at steady state. From the simulation results, the oscillation frequency of 3.50 MHz is obtained, which agrees well with the theory, as expected.

For case 2 ($\alpha_1 = \alpha_2 = 1$, and $\alpha_3 = 0.5$), the simulation parameters chosen are $C_{F1} = C_{F2} = C_{F3} = 40 \text{pF}$, and the frequency of the oscillation equals 35.50 MHz. **Figure 8** is the simulated quadrature outputs i_{out1} , i_{out2} , i_{out3} and i_{out4} at steady state.

For case 3 ($\alpha_1 = \alpha_2 = \alpha_3 = 0.5$), the simulation parameters chosen are $C_{F1} = C_{F2} = C_{F3} =$

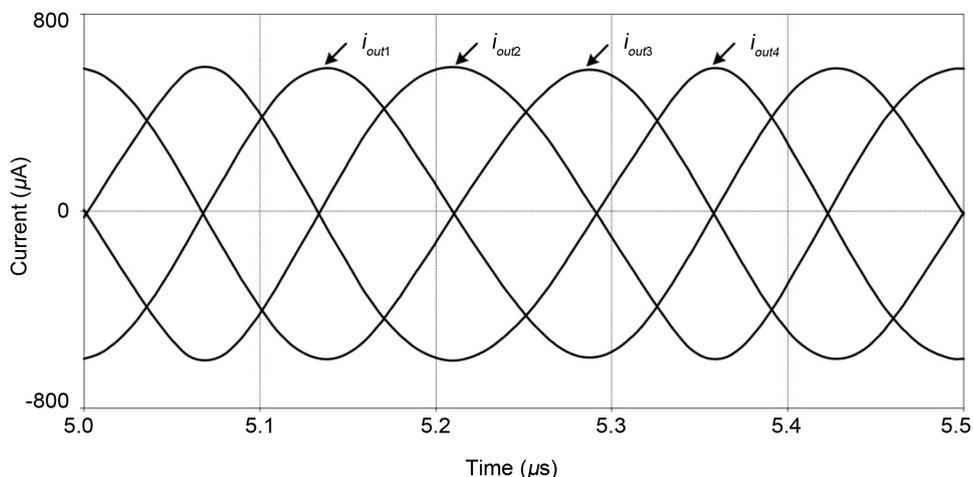


Figure 7. i_{out1} , i_{out2} , i_{out3} , and i_{out4} at steady state.

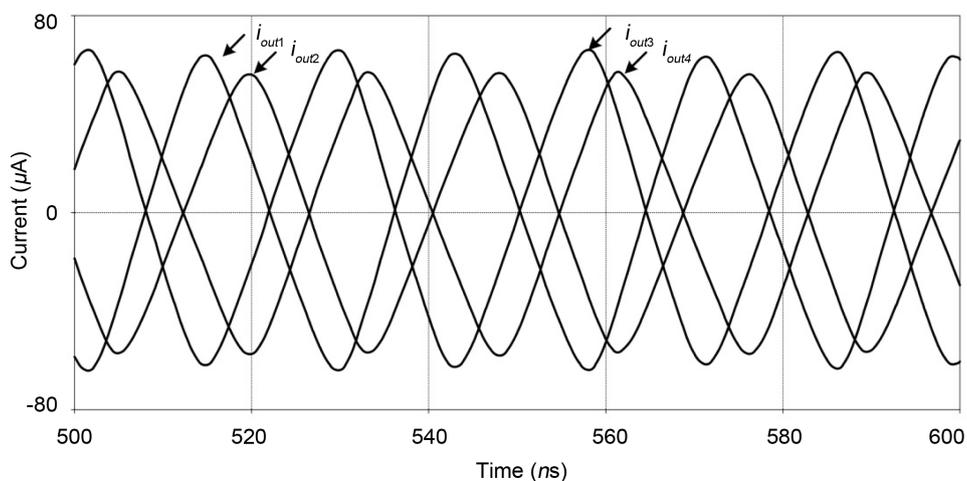


Figure 8. i_{out1} , i_{out2} , i_{out3} , and i_{out4} at steady state.

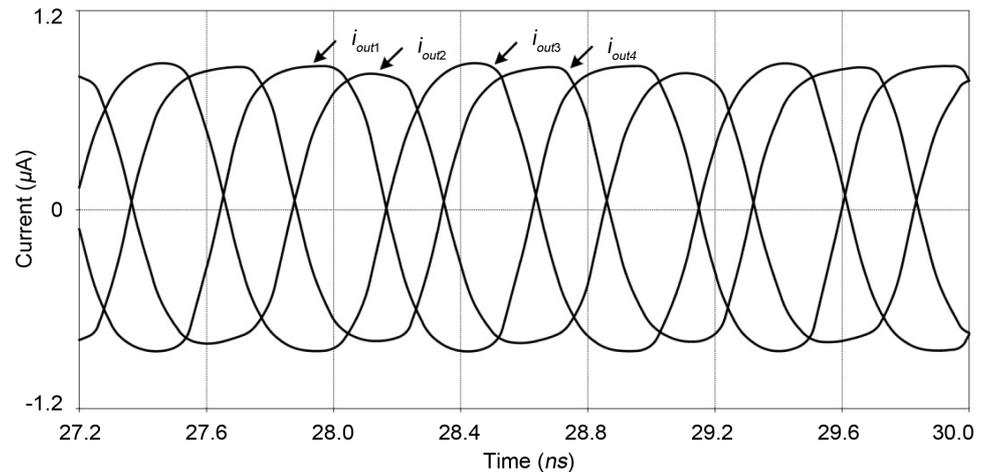


Figure 9. i_{out1} , i_{out2} , i_{out3} , and i_{out4} at steady state.

Table 3. The performance comparison table.

Case	Frequency	Phase difference
$\alpha_1 = \alpha_2 = \alpha_3 = 1$	3.50 MHz	90.00°
$\alpha_1 = \alpha_2 = 1$, and $\alpha_3 = 0.5$	35.50 MHz	99.21°
$\alpha_1 = \alpha_2 = \alpha_3 = 0.5$	1.02 GHz	123.13°

40 pF, and the frequency of the oscillation equals 1.02 GHz. **Figure 9** is the simulated quadrature outputs i_{out1} , i_{out2} , i_{out3} and i_{out4} at steady state.

In each case, the experimental result is compared with the simulated results obtained through PSPICE. In the latter case, the fractional orders capacitors are approximated using the RC ladder networks as shown in **Figure 2**. The parameters of the fractional order quadrature oscillator for the simulation are divided into three cases in **Table 3**. **Table 3** shows that the phase also increases with an increase in the order. It also shows the relationship between the frequency and the phase, which is an advantage that the fractional order can provide, such as a design for a specific phase.

6. Conclusion

This study presented the design of a fractional order CCCFTA-based four-phase sinusoidal oscillator. The proposed circuit consists of two CCCFTAs and three fractional order capacitors. The oscillation frequency and oscillation condition can be electronically/orthogonally controlled via input bias currents. The fractional order parameter gives extra degree of freedom to the design, and it increases the flexibility of the design and adds more fundamentals. PSPICE simulations are included to verify the theoretical analysis. Simulated and theoretical results are in close agreement.

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