

Ride through Strategy for a Three-Level Dual Z-Source Inverter Using TRIAC

A. Nazar Ali¹, Dr. R. Jeyabharath²

¹K. Ramakrishnan College of Technology, Trichy, Tamilnadu, India

²K.S.R Institute for Engineering and Technology, Namakkal, Tamilnadu, India

Email: krcthodeee@gmail.com

How to cite this paper: Nazar Ali, A. and Jeyabharath, Dr.R. (2016) Ride through Strategy for a Three-Level Dual Z-Source Inverter Using TRIAC. *Circuits and Systems*, 7, 3911-3921.

<http://dx.doi.org/10.4236/cs.2016.711326>

Received: April 7, 2016

Accepted: May 1, 2016

Published: September 30, 2016

Copyright © 2016 by authors and Scientific Research Publishing Inc. This work is licensed under the Creative Commons Attribution International License (CC BY 4.0).

<http://creativecommons.org/licenses/by/4.0/>



Open Access

Abstract

A new ride through strategy is introduced in a three-level dual Z-source inverter, for isolation under semiconductor switching failure condition. Here the output will have no significant decrease in the amplitude and quality. Instead of diodes, the triacs are added to the inverter source ends, as it can perform a bidirectional power transfer also it can operate well in both low and high voltage operating conditions. The faulted part can be isolated by simply altering the firing pulses for turning on/off the triacs using the carrier based SPWM technique and resulting in a boosting output with zero common mode voltage. Consequently, it forms a common floating point or null point with a zero common mode voltage. It is experimentally verified by using MATLAB, and digital oscilloscope.

Keywords

Common Mode Voltage, Fault Compensation, Three-Level Inverter, Sinusoidal Pulse Width Modulation, Z-Source Inverter

1. Introduction

The conventional converters have many blockades, such as high distortion, losses with a variation at the amplitude of the output during faulty conditions. To overcome the limitations and problems of the traditional converters, an impedance-source (or impedance-fed) power converter (that can be abbreviated as ZSC) is introduced. **Figure 1** depicts the general structure of ride through strategy introduced in the dual ZSI. The ZSI is a special impedance network (or circuit) that connects the voltage source converter and current converter, main circuit to the power source, load, or another converter, for providing special features that cannot be seen in the conventional converters [1] [2].

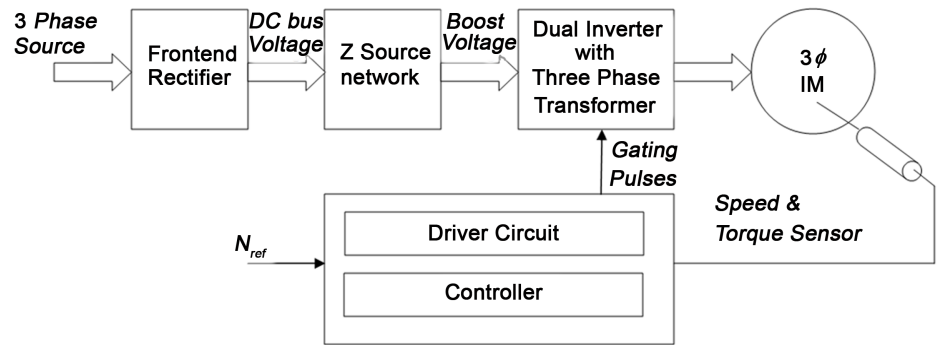


Figure 1. Proposed block diagram.

Contemporarily, three-level inverters are extensively used for industrial applications due to their many inherent advantages including a lower electromagnetic interference (EMI), better waveform quality and lower semiconductor stress which are achieved by an appropriate series-connection of multiple static switches. Despite this popularity, a possible complication associated with three-level inverters is higher risk of experiencing semiconductor switching failure (both open and short circuit). As more switches are used for the inverter construction the switching failure is inevitable [3] [4].

For enhancing the inverter ride-through capability, many fault-tolerant schemes have been proposed with some solutions focusing on the timely replacement of faulty switches using extra pre-installed switches and others focusing on the appropriate selection of switching states that can give rise to a lower waveform distortion. This paper proposed three-level Z-source inverters with ride through capability [5]-[9], unlike other traditional three-level inverter where ride through is not supported.

Here in this manuscript all three-level Z-source inverters can ride-through semiconductor failure smoothly with their output-waveform quality and amplitude kept nearly unchanged. These performance improvements are achieved by performing slight reconfiguration of the inverter state sequences and gating arrangements with no additional hardware requirements as shown in **Figure 1**.

There are many types of ZSI, which have been used for different applications. The few are explained here for the fault tolerant strategy. They are, Z-source neutral point clamped inverter with two dc sources, Z-source neutral point clamped inverter with single dc sources, Z-source DC-linked cascaded inverter, Dual Z-source inverter with two dc sources, Dual Z-source inverter with single dc sources [10]-[12]. But the schemes for detecting faults are not topologically dependent, meaning that existing detection schemes can also be used for new inverter topologies with only minor modifications.

Compared with the other types of inverter it is palpable that the dual source inverter is mostly used, because of its less common mode voltage and it can also be completely eliminated using ride through strategy. The dual-inverter topologies are that the switches are functionally identical with no distinction like inner and outer switch classifications found. The same technique has been used for identifying open-circuit switches in three-level inverter in [9] with some extra logics added to distinguish the

four switches per phase. Other more advanced techniques are proposed in [10] for diagnosing faults in a multilevel inverter that are referred for this paper. With the earlier belief in view, this paper presents a detailed study of a fault ride-through scheme with slight modifications in **Figure 2**.

Additionally, for cases where the dual Z-source inverters are used and configured to operate with reduced common mode switching [13], the simple reconfiguration of the inverter gating signals would allow the inverters to continue operating with less common-mode voltage.

2. Proposed Dual ZSI Using TRIAC

The dual Z-source inverters can be supplied by either two isolated dc sources or a single source. In spite of their drawbacks including the control complexity in the existing method a new technique is implemented with slight modifications in **Figure 3**. Both inverters are tuned to operate with zero common-mode voltage by simply restricting their switching states (by the omitting the dead time delay, which is an inherent feature of all Z-source inverters). Generally there are two categories for reducing the CMV they are using hardware devices like isolation transformer, filters, zero sequencing impedance and control strategy using software includes SVPWM schemes, sine PWM scheme etc. Here the dual-inverter topology triacs connected in series with the inverters controlled by SPWM technique is introduced.

As triac is a bidirectional device it can conduct in both directions. The ride-through technique for dual Z-source inverters can simply be performed by considering the open and short-circuit failure of any single switch which leads to common mode voltage. The term common mode voltage is defined as an undesirable electric signal which is generated by the power electronic switching circuits having same amplitude and frequency to

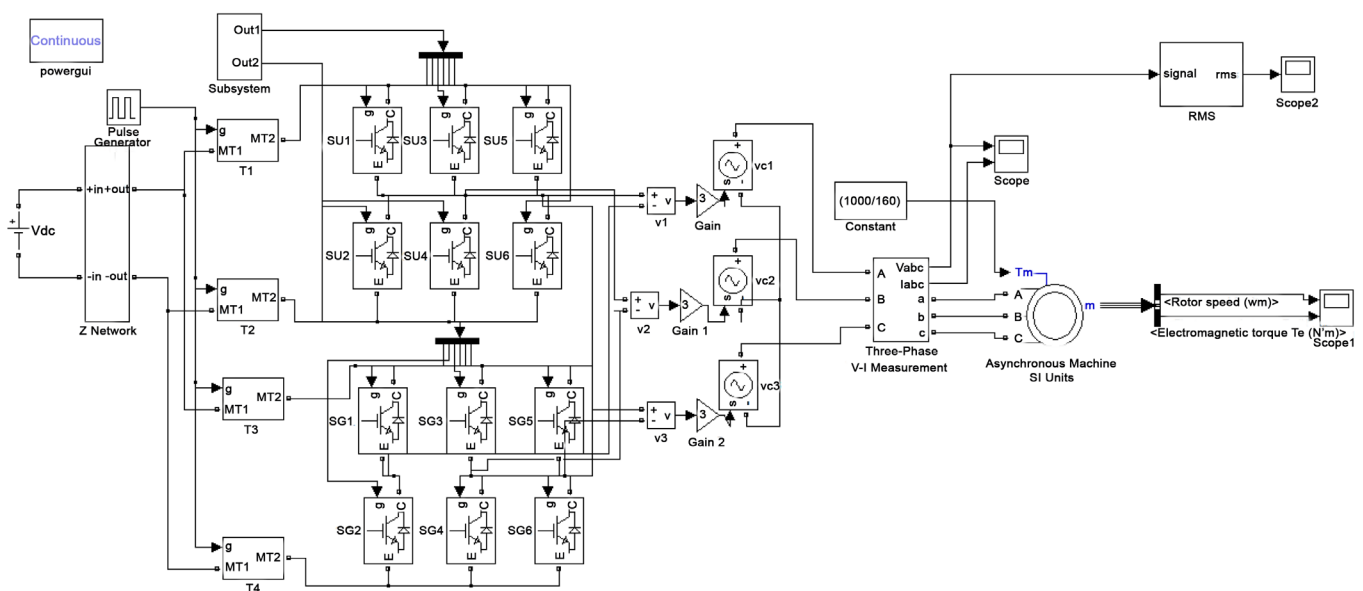


Figure 2. Proposed dual Z-source inverter using TRIACs.

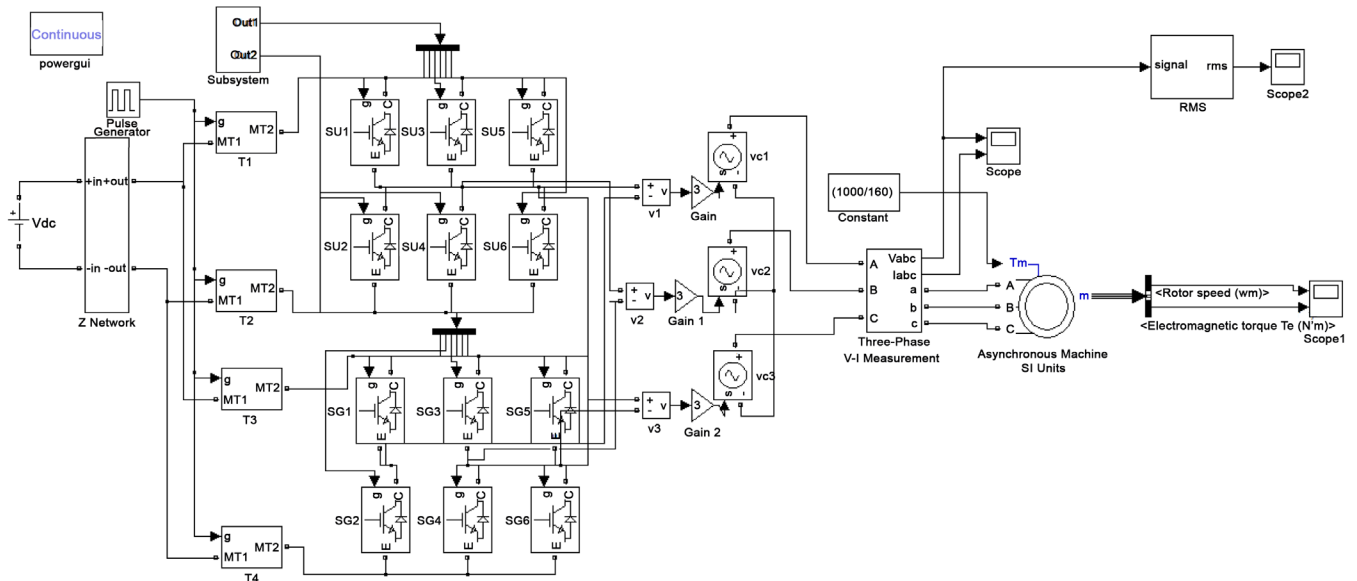


Figure 3. Circuit of dual ZSI under normal condition.

that of the reference signal. This interferes with the control and other electronic equipments. Hence leads to EMI, high shaft voltage. When this voltage exceeds the breakdown voltage results in large bearing current, and causes premature failure of the motor bearing, induces leakage current, false tripping of relays etc. Hence it is a great issue which exists only in motor forming a crisis in the system.

Hence, during switching failure the inverter simply generates two level output without altering its shoot-through duration for compensating the voltage dip. This method turns all the zero states into shoot through state thus minimizing the voltage stress across the switches. Where S_a , S_b , and S_c represent the switching functions of inverter U in two-level mode and V_i is its dc-link voltage. The proposed scheme is likely to work under most operating conditions except for cases whereby two switches and their accompanied anti-parallel diodes in a phase leg in either of the inverter U or G fail, open-circuit simultaneously.

Assuming that a fault occurred in inverter G, the failed terminal $V_x(y)$ ($x = a, b$, or c , and $y = U$ or G) becomes isolated, by forcing it to null state $[000]$ or $[111]$ by turning off the lower triacs, the aroused floating point will be symmetrical which can no longer be formed for common-mode voltage elimination and that no current can now flow in the faulted phase. In addition, for the case where two isolated sources can be used, it is noted that the output terminals of the lower inverter G are now constantly shorted to form a floating point on the primary side of the transformer.

The generated common-mode voltage at the secondary terminals of the transformer is derived, whose value is zero. This extra feature and the symmetrical structure of the dual inverter allow it to ride-through virtually all types of semiconductor failure with negligible disturbances incurred on its output-voltage amplitude, waveform quality, and common mode elimination capability, which, to date, cannot be achieved by other three-level Z-source inverters. In the erstwhile methods zero common mode voltage

cannot be retained if a single dc source is used in the inverter. This proposed technique can be explained through two modes of operations.

They are,

Mode 1: Pre-fault condition

Mode 2: Faulted condition

2.1. Mode-1

This is a pre-fault condition, here the inverter undergoes normal inverter in **Figure 4**. This has two conduction angle 120° & 180° . In 180° conduction three switches will be turned ON at a time (*i.e.*) 123, 234, 345, 456, 561, 612. During 120° conduction two switches remain ON at any instant of time. The ZSI operates as active or non shoot through state. In non-shoot through state the input diode is ON, V_{ac} source, inductor transfer energy to load, capacitor charges hence the voltage is boosted.

Switching frequency (F) = $1/T$

= $1/0.0002$

= 5 kHz

Duty cycle = 0

2.2. Mode-2

In mode II, a fault is introduced in any one of the inverter either the upper or lower inverter in **Figure 5**. If the fault occurs in the upper inverter the switch1 and triac1 will turn-off. The switches 4, 6 & 2, will conduct by the inductive boosting of Z-source network through triac 2. It forms floating star point in the upper inverter. Here the ZSI undergoes shoot through state, where the switch is reversed biased and the input is isolated from the load and the capacitors discharge energy to the inductor and load when the inverter operates in active state. Hence provides a boosting operation.

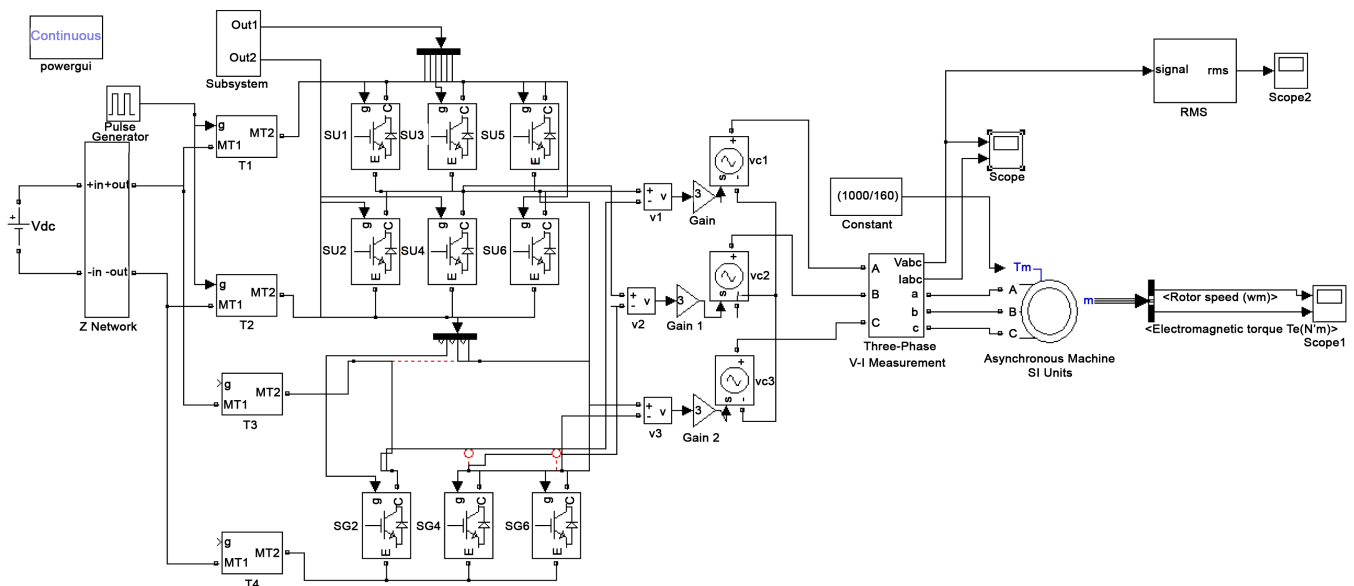


Figure 4. Circuit of dual ZSI under faulted condition.

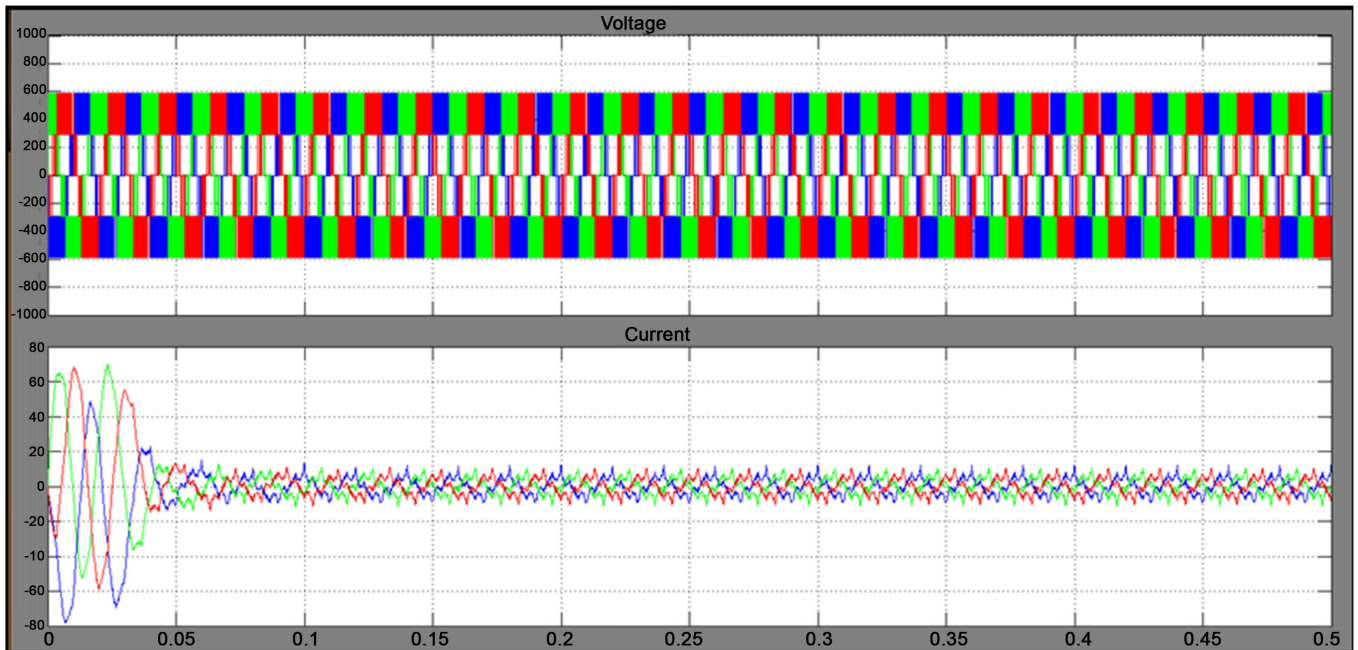


Figure 5. Proposed system simulation output of dual ZSI voltage and current.

During this shoot through operation two switches of same leg conducts simultaneously without any failure. A carrier based PWM technique is used, in which the carrier wave is compared with the reference signals ensures boosting output voltage, reduced CMV by eliminating the dead time delay. Hence during fault condition the inverter is operated without any interruption.

Switching frequency = 5 kHz

Duty cycle = 0.33

3. Simulation and Hardware Results

The proposed fault-tolerant strategies were initially verified in mat lab simulation with the Z-source network parameters chosen as $C = 2200 \mu\text{F}$ and $L = 5 \text{ mH}$ and the switching frequency set to 5 kHz. In common, all tested inverters were powered from single dc sources with set to 40 V, which was subsequently boosted to $\approx 100 \text{ V}$ for powering the rear-end inverter circuitry during various fault conditions set to occur at $t = 40 \text{ ms}$. Before fault occurrence, the pre-fault control parameters are set to $M = 1$ and $T_0/T = 0$, and immediately upon sensing the fault, the control parameters are returned to $M = 0.67$ and $T_0/T = 0.33$ is needed for producing enough voltage boosting to keep the three-phase ac output currents unchanged. Hence the Phase and line voltage is of about 230 V during normal and faulted condition.

The Z-source inverter is specially suited for fuel cell applications. Unique features include buck-boost inversion by single power-conversion stage, improved reliability, strong EMI immunity, and low EMI. The Z-source technology can be applied to the entire spectrum of power conversion. To have a new power conversion technology, a new Z-source inverter is proposed which has the capacity to solve the above problems and

unique feature includes,

- It can boost the output voltage by introducing shoot through operation mode, which is forbidden in traditional voltage source inverters.
- With this unique feature, the Z-source inverter provides a cheaper, simpler, single stage approach for applications of fuel cell.

Thus, the Z-source inverter system can minimize stress and increase the output power greatly. The simulated results obtained with the same pre- and post-fault parameters of $M = 1$ and $T_0/T = 0$. Since the faulted circuitry is still being powered by the two separate dc sources, instead of one as in the first case (**Figures 6-9**).

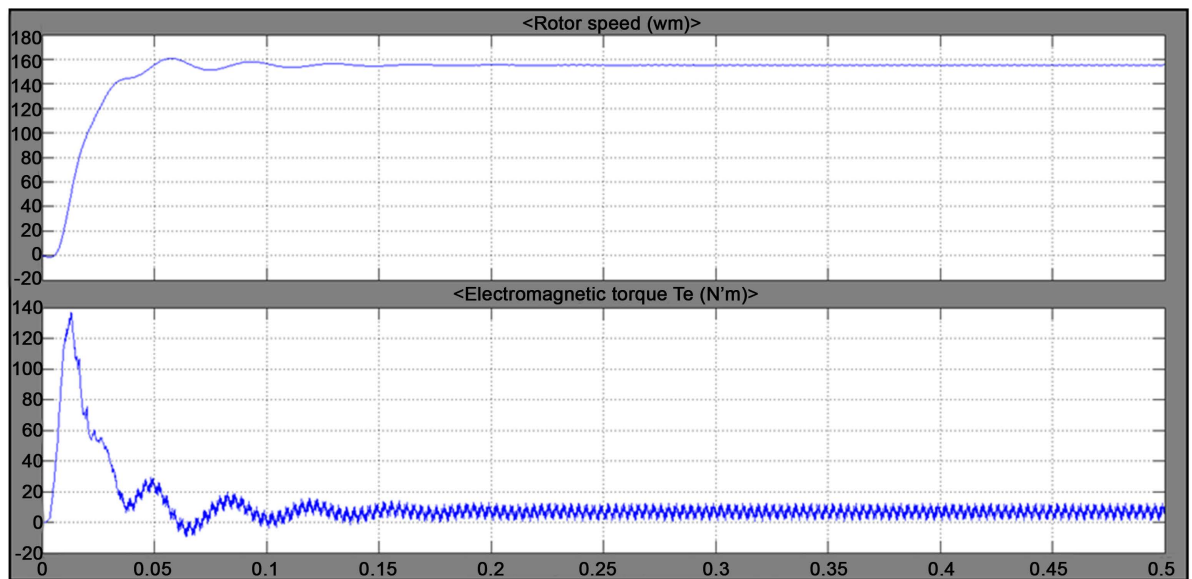


Figure 6. Proposed system simulation output for three phase induction motor load speed and torque.

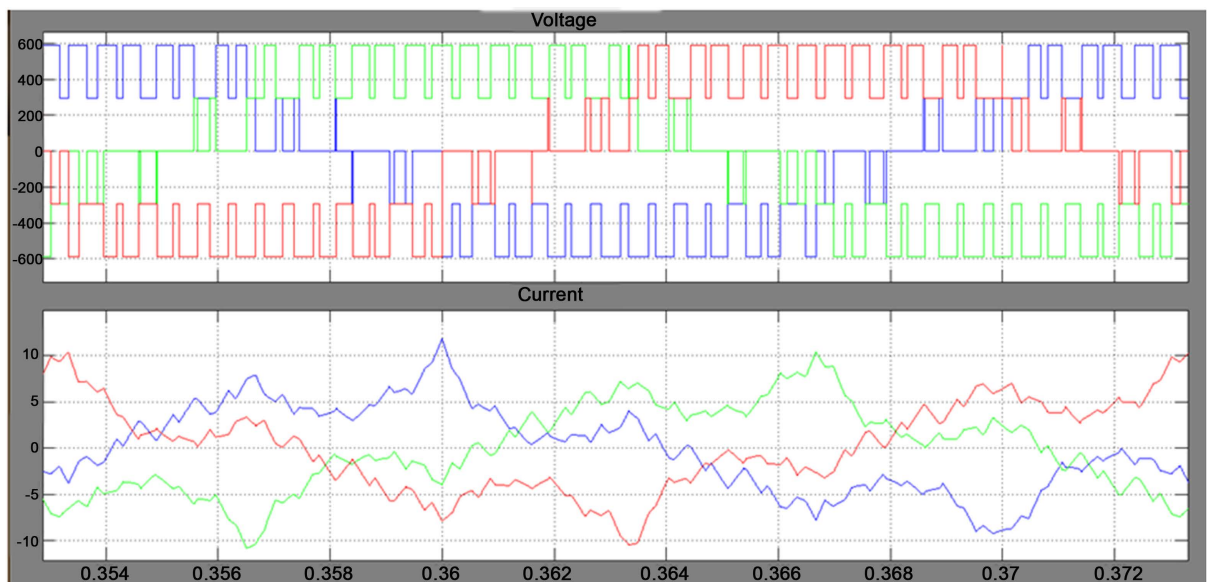


Figure 7. Simulation output of dual ZSI under fault condition voltage and current.

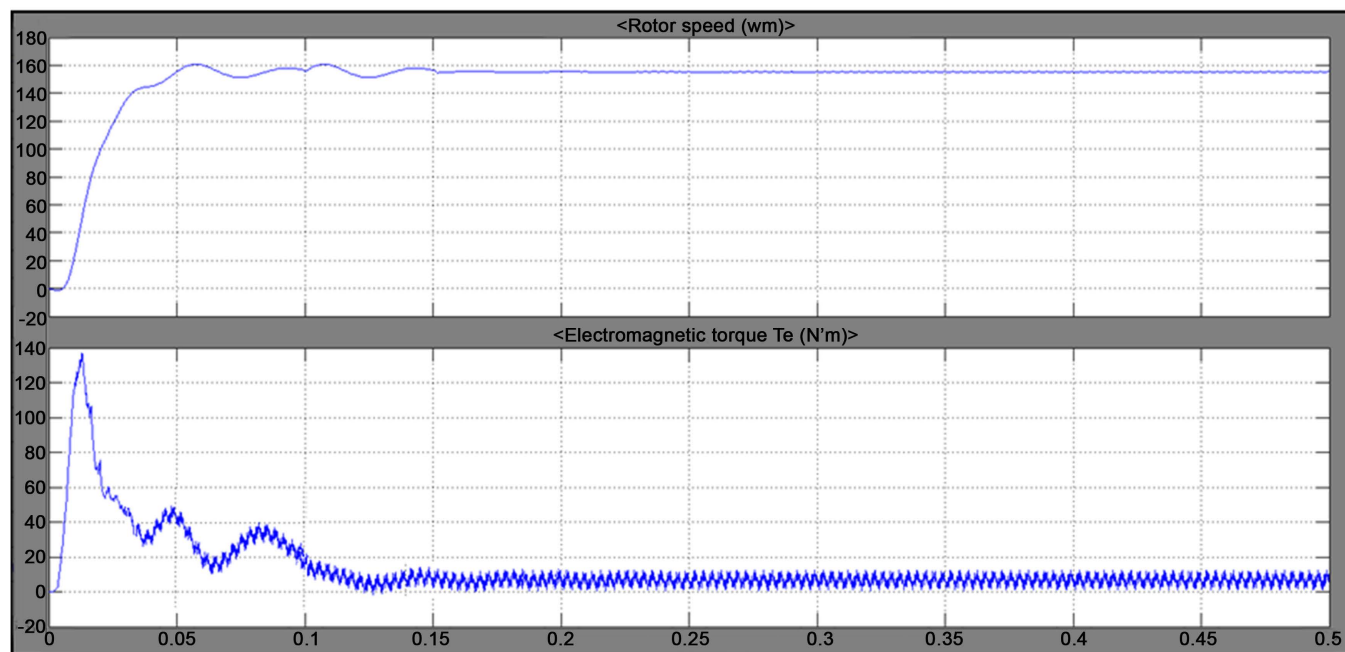


Figure 8. Simulation output of dual ZSI under fault condition speed and torque.

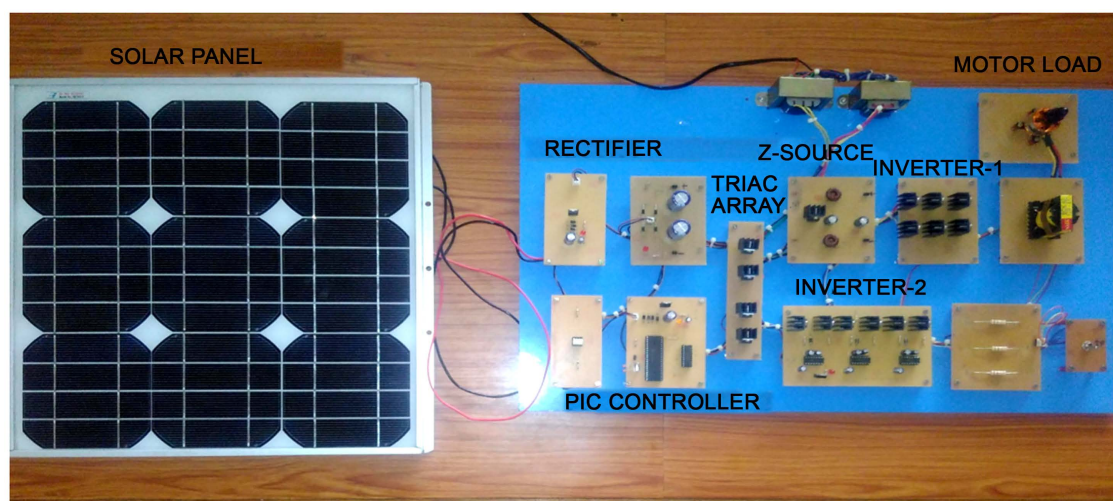


Figure 9. Proposed hardware image.

However, it causes shoot through duty ratio to vary in each cycle, thus increasing the ripple content in inductor current. When the output frequency is low, the inductor ripple becomes significant and a large inductor is required. This method achieves maximum boosting output while keeping shoot through duty ratio as constant all the time, thus reduces ripple content in inductor current.

The **Figure 9** shows the hardware image of the dual ZSI using triacs. The components are enumerated in **Table 1** and **Table 2** with their specifications. The **Figure 10** and **Figure 11** show the output of the hardware under normal and faulty condition which are displayed using the digital oscilloscope.

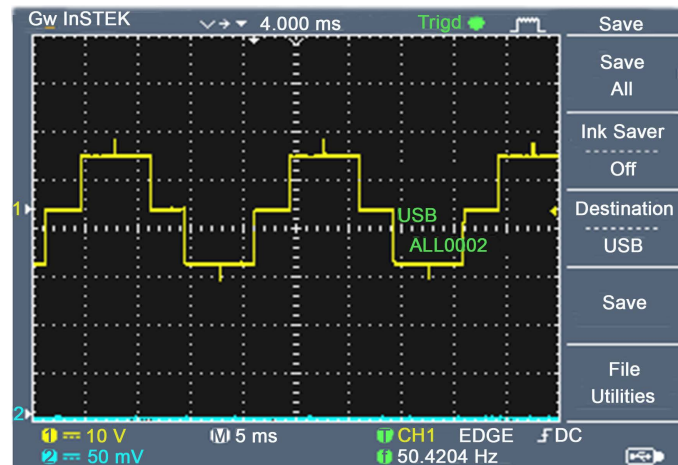


Figure 10. Hardware output during normal condition.

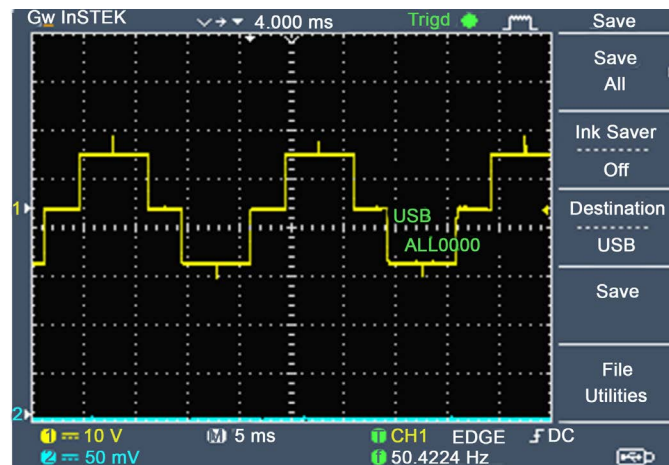


Figure 11. Hardware output during fault condition.

Table 1. Components and its voltage rating.

S. No	Component	Input Voltage
1	Step down transformer (bridge rectifier input)	230/15 V, AC
2	Step down transformer (capacitor bank input)	230/10 V, AC
3	Bridge rectifier	15 V, AC
4	DC input	10 V, AC
5	Opto-isolator	12 V, AC
6	PIC	5 V, DC
7	Z-source network	
8	TRIACS	
9	Inverter1	20 V, DC
10	Inverter2	
11	Gate driver	12 V, AC
12	Resistive load	10 ohms
13	SPDT switch	-
14	Isolation transformer	-
15	BLDC motor	48 V

Table 2. Components and its specifications.

S. No	Components	Specifications
1	PIC	16F877A
2	Buffer	74LS244A
3	Gate driver	IRS2110
4	Opto-Isolator	TLP250
5	Triac	BT136
6	Diode	IN2007
7	Mosfet	IRF840
8	Resistor	10 ohms , 22 ohms
9	Capacitor	2200 micro farad, 10 micro farad
10	Inductor	20 micro henry

4. Conclusion

In this project a new ride through strategy for Dual ZSI using triac is analyzed and the output has been simulated using MATLAB software. Its feasibility is checked with the simulated results of the conventional method. The fault condition is detected within one fourth of the fundamental cycle. This concept improves the ride-through ability of the dual Z-source inverters supplied by either a single dc source or two isolated dc sources with added triacs, with an advantage of maximum output, fewer ripple content and zero common mode voltage; hence helps the inverter to operate without any interruption. The future scope of this Impedance Source Inverter is that, by obtaining the parameter control of the motor this can be implemented in speed control methods and can be achieved by using micro controller as a feedback between output and the input.

References

- [1] Peng, F.Z. (2003) Z-Source Inverter. *IEEE Transactions on Industry Applications*, **39**, 504-510. <http://dx.doi.org/10.1109/TIA.2003.808920>
- [2] Ribeiro, R.L.A., Jacobina, C.B., da Silva, E.R.C. and Lima, A.M.N. (2001) A Fault Tolerant Induction Motor Drive System by Using a Compensation Strategy on the PWM-VSI Topology. 2001 *IEEE 32nd Annual Power Electronics Specialists Conference*, Vancouver, 17-21 June 2001, 1191-1196. <http://dx.doi.org/10.1109/PESC.2001.954281>
- [3] Beltrao de Rossiter Correa, M., Brandao Jacobina, C., Cabral da Silva, E.R. and Nogueira Lima, A.M. (2001) An Induction Motor Drive System with Improved Fault Tolerance. *IEEE Transactions on Industry Applications*, **37**, 873-879. <http://dx.doi.org/10.1109/28.924770>
- [4] Li, S. and Xu, L. (2006) Strategies of Fault Tolerant Operation for Three-Level PWM Inverters. *IEEE Transactions on Power Electronics*, **21**, 933-940. <http://dx.doi.org/10.1109/TPEL.2006.876867>
- [5] Richardeau, F., Baudesson, P. and Meynard, T.A. (2002) Failures-Tolerance and Remedial Strategies of a PWM Multicell Inverter. *IEEE Transactions on Power Electronics*, **17**, 905-912. <http://dx.doi.org/10.1109/TPEL.2002.805588>
- [6] Chen, A., Hu, L., Chen, L.F., Deng, Y. and He, X.N. (2005) A Multilevel Converter Topolo-

- gy with Fault-Tolerant Ability. *IEEE Transactions on Power Electronics*, **20**, 405-415. <http://dx.doi.org/10.1109/TPEL.2004.842983>
- [7] Chokhawala, R.S., Catt, J. and Kiraly, L. (1995) A Discussion on IGBT Short Circuit Behavior and Fault Protection Schemes. *IEEE Transactions on Industry Applications*, **31**, 256-263. <http://dx.doi.org/10.1109/28.370271>
- [8] Peugeot, R., Courtine, S. and Rognon, J.-P. (1998) Fault Detection and Isolation on a PWM Inverter by Knowledge-Based Model. *IEEE Transactions on Industry Applications*, **34**, 1318-1326. <http://dx.doi.org/10.1109/28.739017>
- [9] de Araujo Ribeiro, R.L., Jacobina, C.B., da Silva E.R.C. and Lima, A.M.N. (2003) Fault Detection of Open-Switch Damage in Voltage-Fed PWM Motor Drive Systems. *IEEE Transactions on Power Electronics*, **18**, 587-593. <http://dx.doi.org/10.1109/TPEL.2003.809351>
- [10] da Silva, E.R., Lima, W.S., de Oliveira, A.S., Jacobina, C.B. and Razik, H. (2006) Detection and Compensation of Switch Faults in a Three Level Inverter. *IEEE Annual Power Electronics Specialists Conference*, July 2006, 1-7. <http://dx.doi.org/10.1109/PESC.2006.1711955>
- [11] Khomfoi, S. and Tolbert, L.M. (2007) Fault Diagnosis and Reconfiguration for Multilevel Inverter Drive Using AI-Based Techniques. *IEEE Transactions on Industrial Electronics*, **54**, 2954-2968. <http://dx.doi.org/10.1109/TIE.2007.906994>
- [12] Loh, P.C., Gao, F., Blaabjerg, F., Feng, S.Y. and Soon, K.N. (2007) Pulsewidth-Modulated Z-Source Neutral-Point-Clamped Inverter. *IEEE Transactions on Industry Applications*, **43**, 1295-1308. <http://dx.doi.org/10.1109/TIA.2007.904422>
- [13] Loh, P.C., Gao, F. and Blaabjerg, F. (2008) Topological and Modulation Design of Three-Level Z-Source Inverters. *IEEE Transactions on Power Electronics*, **23**, 2268-2277. <http://dx.doi.org/10.1109/TPEL.2008.2002452>



Scientific Research Publishing

Submit or recommend next manuscript to SCIRP and we will provide best service for you:

Accepting pre-submission inquiries through Email, Facebook, LinkedIn, Twitter, etc.

A wide selection of journals (inclusive of 9 subjects, more than 200 journals)

Providing 24-hour high-quality service

User-friendly online submission system

Fair and swift peer-review system

Efficient typesetting and proofreading procedure

Display of the result of downloads and visits, as well as the number of cited articles

Maximum dissemination of your research work

Submit your manuscript at: <http://papersubmission.scirp.org/>

Or contact cs@scirp.org