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Reduction of THD in Thirteen-Level Hybrid PV Inverter with Less Number of Switches

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Abstract

Multilevel inverter (MLI) is one of the most efficient power converters which are especially suited for high power applications with reduced harmonics. MLI not only achieves high output power and is also used in renewable energy sources such as photovoltaic, wind and fuel cells. Among various topologies of MLI, this paper mainly focuses on cascaded MLI with three unequal DC sources called asymmetric cascaded MLI which reduces the number of power switches. Various modulation techniques are also reviewed in literature [1]. In this paper we focus on sinusoidal (or) multicarrier pulse width modulation (SPWM) which improves the output voltage at lower modulation index for obtaining lower Total Harmonic Distortion (THD) level. The gating signal for the 13-level hybrid inverter using SPWM technique is generated using Field Programmable Gate Array (FPGA) processor. The proposed modulation technique results in reduced percentage of THD, but lower order harmonics are not eliminated. So a new technique called Selective Harmonic Elimination (SHE) is also implemented in order to reduce the lower order harmonics. The optimum switching angles are determined for obtaining minimum THD. The performance evaluation of the proposed PWM inverter is verified using an experimental model of 13-level cascaded hybrid MLI and compared with MATLAB/SIMULINK model.

Keywords

Asymmetric Cascaded Multi Level Inverter (ACMLI), Total Harmonic Distortion (THD), Sinusoidal Pulse Width Modulation (SPWM), Field Programmable Gate Array (FPGA), Selective Harmonic Elimination (SHE)

1. Introduction

In recent years multilevel inverter [2] plays an important role and attracts more attention in the conversion of

medium power applications. It is simple in construction, better-quality in performance and produces lesser harmonics. Also it has lower switching losses, high dv/dt rating and reduced switching stresses and harmonics. The three commercial topologies of multilevel voltage source inverters are (i) the Neutral Point Clamped (NPC) or diode clamped multilevel inverter (DCMLI), (ii) flying capacitor multilevel inverter (FCMLI), and (iii) cascaded H-bridge (CHB) multilevel inverter. Unlike DCMLI and FCMLI the CMLI does not require voltage clamping diodes and voltage balancing capacitors. This paper focuses particularly on cascaded hybrid multilevel inverter [2]-[5] which requires independent DC sources *i.e.* for "n" number of DC sources the number of levels obtained will be (2n + 1). In view of DC source, the CHB multilevel inverter is further divided into two topologies namely symmetric and asymmetric inverters. The values of all the voltage sources are equal in symmetric topology. In symmetric topology if the number of output voltage levels is increased, it results in rapid increase in number of switching devices. So in order to increase the number of output voltage levels with less number of switching devices the different value of DC sources are selected which is named as asymmetric topology [6] [7]. Among these two topologies, asymmetric cascaded MLI is explained in this paper and it requires three unequal DC sources to produce thirteen-level output. This new topology has been proposed to obtain 13-level output with minimum number of switches. In addition to that the THD are reduced and specified harmonics are eliminated using selective harmonic elimination technique (SHE PWM).

2. Asymmetric Cascaded Multilevel Inverter (ACMLI)

Normally a CMLI requires "n" dc sources for (2n + 1) level. But it is difficult to use separate DC sources for many applications since it requires many long cables and could lead to voltage imbalance among the DC sources.

Figure 1 represents CMLI consisting of two H-bridges. Each H-bridge is provided with separate different values of dc source as V_{dc} for bridge 1 and $V_{dc}/2$ for bridge 2. The output of H-bridge 1 is denoted as $V_1(t)$ and another one as $V_2(t)$. Hence output phase voltage is given by $V_0(t) = V_1(t) + V_2(t)$.

If the number of levels is increased it results in increase in number of H-bridges.

In general the output phase voltage is given by

$$V_0(t) = V_1(t) + V_2(t) + \cdots + V_N(t) \tag{1}$$

It can also be determined from the individual cells switching states.

It is represented as

$$V_0(t) = \sum_{j=1}^{N} (\mu_j - 1) V_{dc,j}, \quad \mu_j = 0,1 \tag{2}$$

The maximum output voltage

$$V_0 Max = N V_{dc} \tag{3}$$

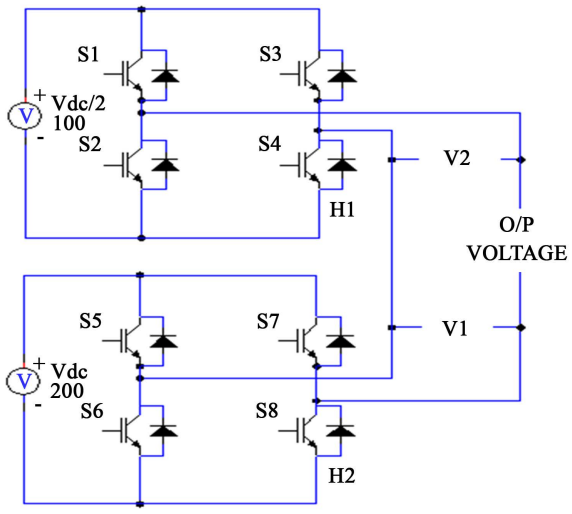

Figure 1. CMLI with unequal dc sources.

By closing and opening of the switches alternatively the output of H1 is obtained as $V_1(t)$ which is equal to $+V_{dc}$, 0, $-V_{dc}$ and for bridge 2 is $V_2(t)$ which is equal to $+V_{dc}/2$, 0, $-V_{dc}/2$.

Hence $V_0(t)$ gives the value of $-3/2V_{dc}$, $-V_{dc}$, $-1/2V_{dc}$, 0, $+1/2V_{dc}$, $+V_{dc}$, $+3/2V_{dc}$ for the above CMLI. **Figure 2** shows an 11 level inverter output $V_0(t)$ gives a value of $-5/2V_{dc}$, $-3/2V_{dc}$, $-V_{dc}$, $-1/2V_{dc}$, 0, $+1/2V_{dc}$, $+V_{dc}$, $+3/2V_{dc}$, $+5/2V_{dc}$.

The major advantages of ACMLI are

- Less Number of dc sources;
- Low switching losses;
- Output switching frequencies are low;
- Cost and complexity are reduced ;
- Reduced harmonics level;
- Increased output efficiency.

3. Modulation Methods for ACMLI

The three main modulation techniques: Fundamental frequency switching, space vector modulation (SVM), sinusoidal (or) multi carrier PWM (SPWM). In frequency switching modulation, initially the switching angles are calculated and then it is transferred to the digital system. This technique will eliminate the lower order harmonics to reduce distortion in output voltage. SVM is used to obtain the commutation state for the switches. If the number of levels in the inverter is increased this method becomes more complex. In SPWM it has several carrier signals keeping only one modulating signal. The carrier signals are triangular one and have same frequency and peak to peak amplitude so that the bands they occupy are contiguous *i.e.* one carrier signal will have a contact with other signal. The modulating signal is pure sinusoidal and at every instant each carrier signal is compared with modulating signal. In each comparison if the modulating signal is greater than the carrier signal it gives one or otherwise zero. The results are added to give the voltage level, which is required at the output terminal of the inverter. SPWM is further categorized in to 2 groups namely carrier disposition (CD) and phase disposition (PD) method. To sample the reference waveform in CD method, the number of carrier signals is displaced by contiguous increment in amplitude of the reference waveform. Similarly the multi carrier phase is shifted in case of PD method. The phase disposition method is implemented here in this paper as it gives least THD.

4. Proposed Model of Single Phase ACMLI

4.1. Circuit Description

Since explained in the earlier methods of CMLIs, it is necessary to implement a new design to overcome the

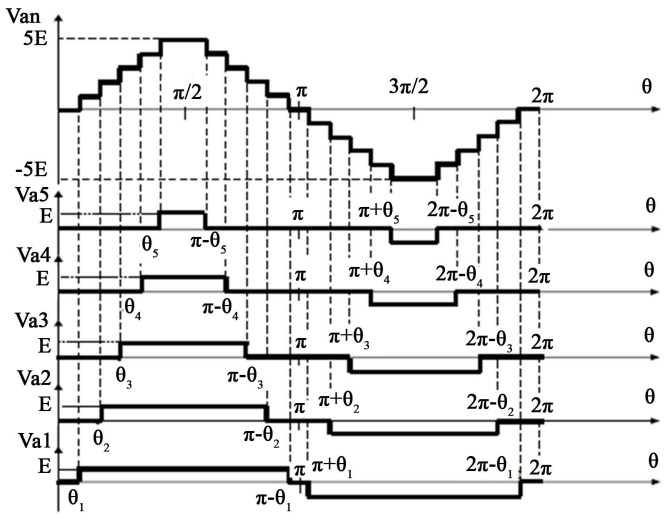

Figure 2. A cascaded 11 level inverter output.

disadvantages of the other methods. So a new design of topology is required to form an asymmetric inverter as shown in **Figure 3**. Here there are 3 DC sources connected with seven switches which include an H-bridge inverter. All IGBT switches are connected as shown in the **Figure 3** in order to form a hybrid cascaded inverter. The hardware model of the proposed inverter is also described here.

The new topology comprises a Spartan 3E FPGA processor with a control of modulation index level to form various levels of inverter. The basic operation of FPGA processor is explained in chapter 6. Three Flywheel diodes are used to prevent the back emf from triggering and other circuits in the proposed model. By using FPGA the gating signal for 13-level inverter is generated for employing the SPWM technique. The hardware prototype model is also shown in **Figure 4** and the internal blocks of the FPGA implementation technique is also shown in **Figure 5**.

4.2. Generation of Gating Pulses Using FPGA

To produce a 13-level output the proposed modulation technique carries six carrier signals with one modulating signal. The carrier waveform for the proposed system is shown in **Figure 6**. The switching states and voltage levels of the proposed inverter are shown in **Table 1**.

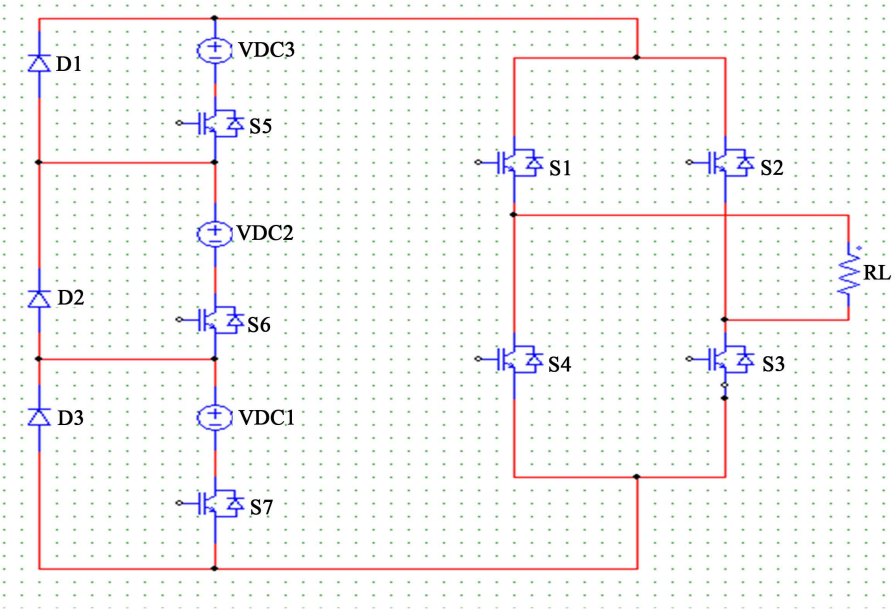

Figure 3. Proposed circuit model for 13-level ACMLI.

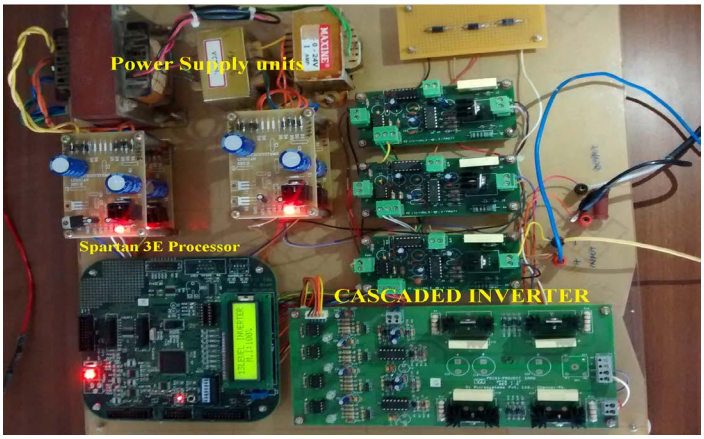

Figure 4. Prototype model of FPGA SPARTAN 3E processor.

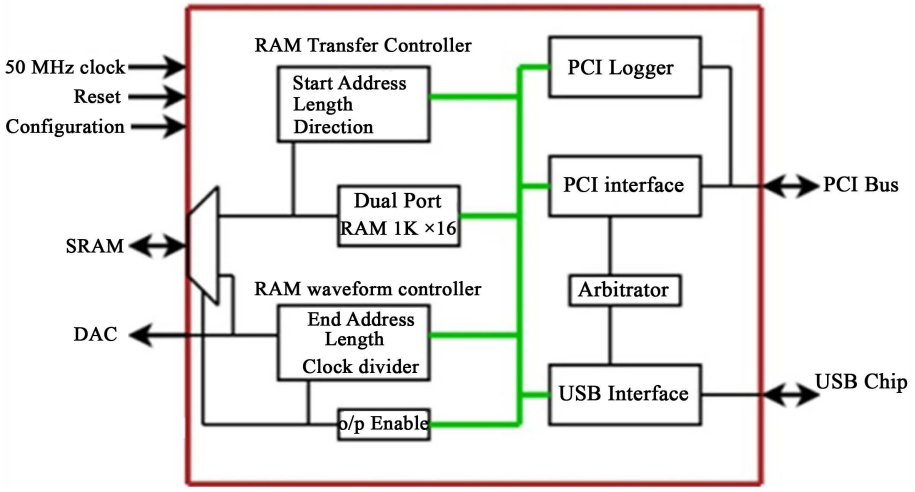

Figure 5. Internal blocks of FPGA implementation.

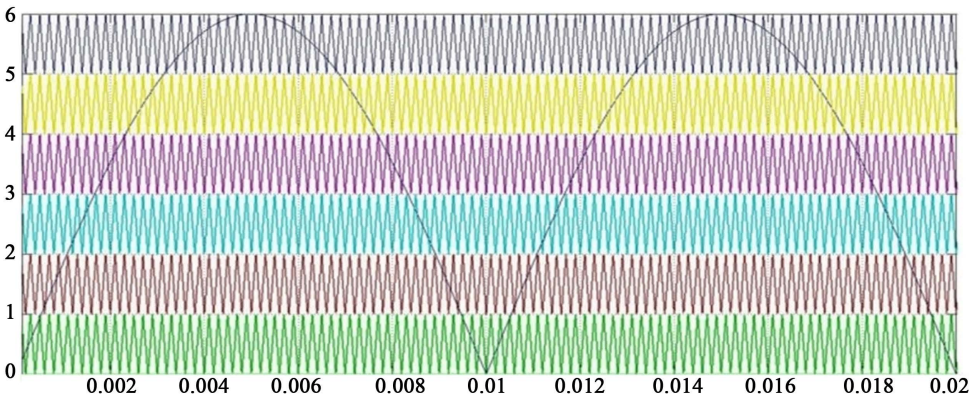

Figure 6. Carrier waveform for SPWM technique.

Table 1. Switching states and voltage levels of 13-level inverter.

S5	S6	S7	S1	S2	S3	S4	Output voltage V_d
0	0	1	1	0	1	0	$+V_d$
0	1	1	1	0	1	0	$+V_d/6$
0	1	1	1	0	1	0	$+V_d/3$
1	0	0	1	0	1	0	$+3V_d/6$
1	0	1	1	0	1	0	$+2V_d/3$
1	1	1	1	0	1	0	$+4V_d/5$
0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	$-V_d$
0	1	1	0	1	0	1	$-V_d/6$
0	1	1	0	1	0	1	$-V_d/3$
1	0	0	0	1	0	1	$-3V_d/6$
1	0	1	0	1	0	1	$-2V_d/3$
1	1	1	0	1	0	1	$-4V_d/5$

4.3. Matlab/Simulink Model

The simulation model for a 13-level inverter with R load is shown in **Figure 7**. By using MATLAB/SIMULINK the proposed 13-level inverter is simulated by using Insulated Gate Bipolar Transistor (IGBT) switches. Here only 7 switches are used to produce 13-level output along with 3 feedback diodes. The staircase output and the FFT analysis for THD% is shown in **Figure 8**. The model is verified using RL load and its corresponding FFT analysis is shown in **Figure 9**. The staircase output voltage and current waveform of 13-level inverter thus obtained is shown in **Figure 10**. From the obtained result the THD for R load is 9.29% at 1500 Hz frequency for 126.6 V. Similarly with LC filter the THD is 1.09% for 129.5 V. We also observed from the simulation result

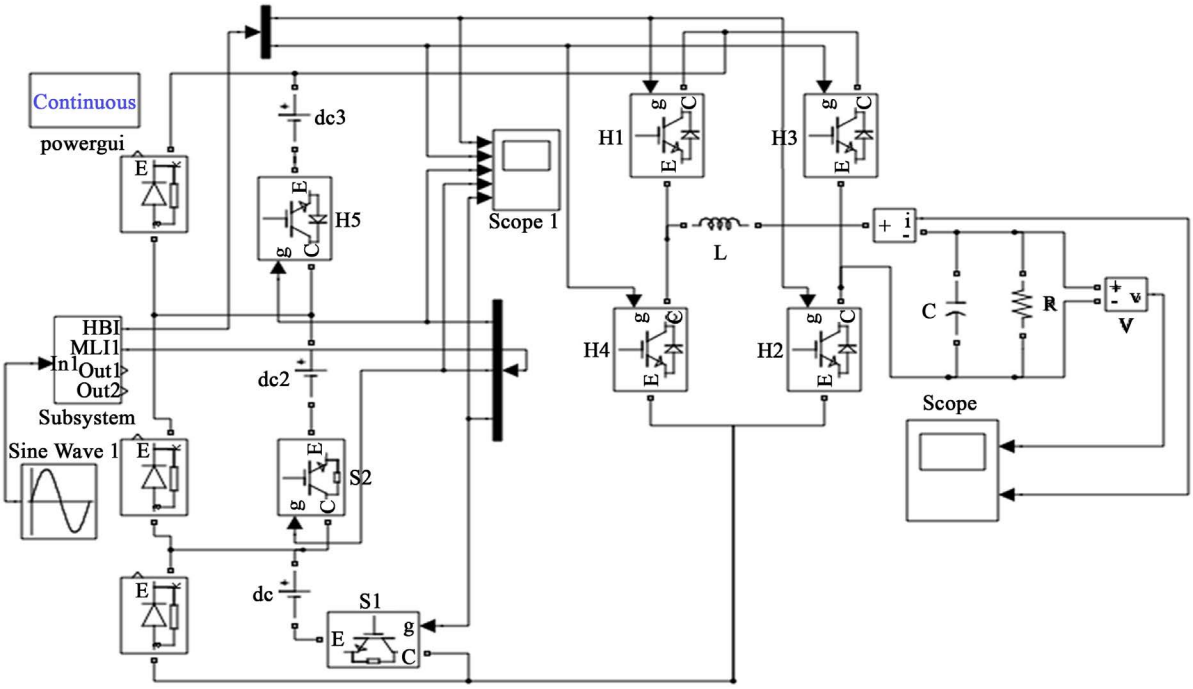

Figure 7. Circuit diagram with RL load for 13-level inverter.

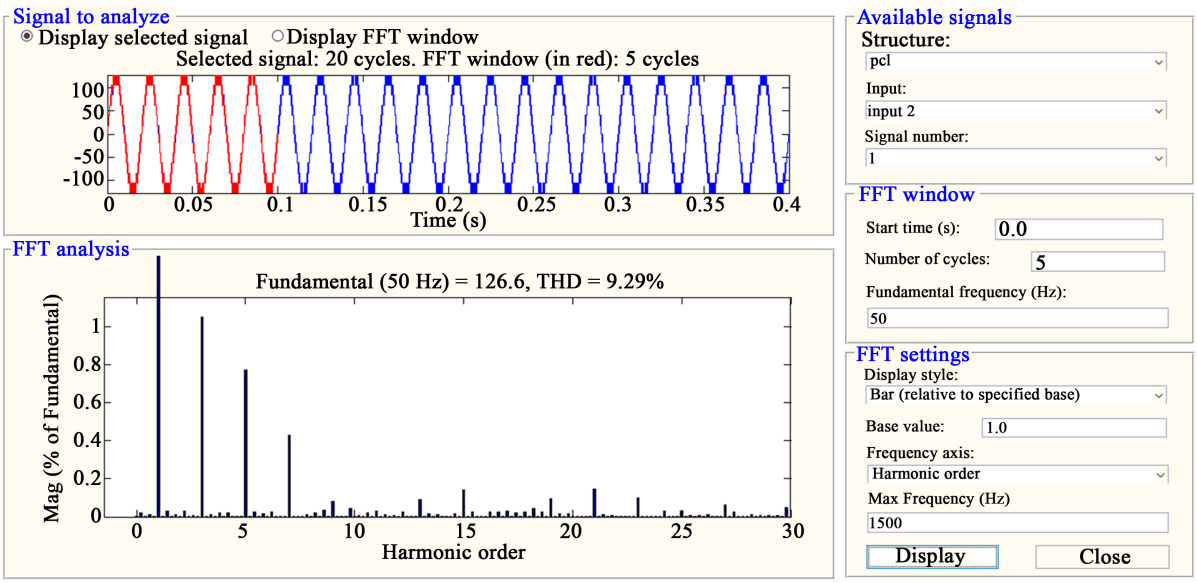

Figure 8. FFT analysis for 13-level inverter with R load.

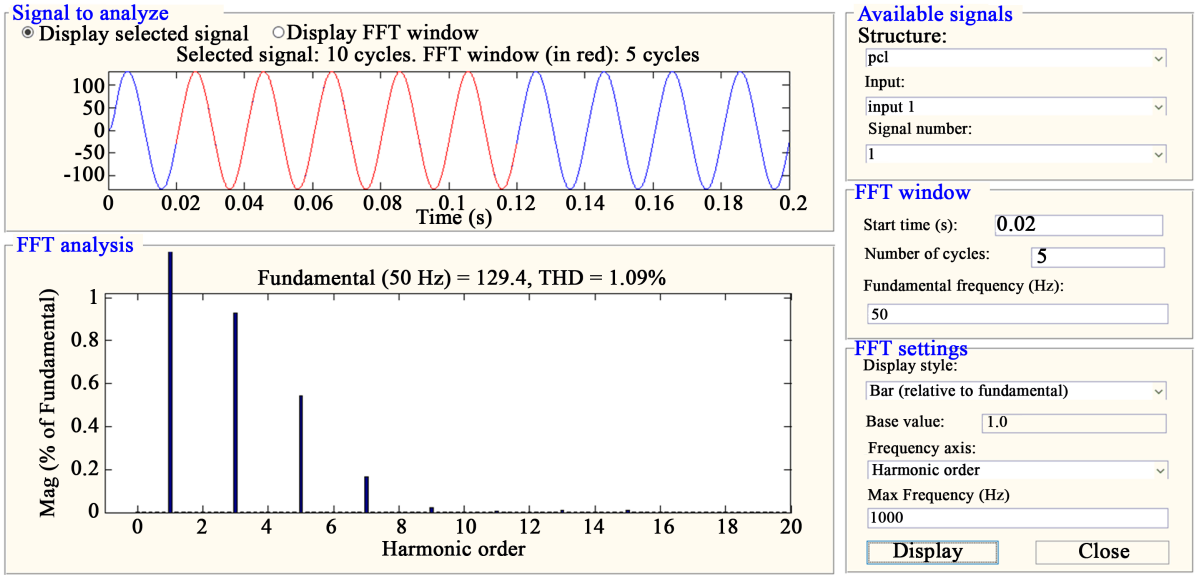

Figure 9. FFT analysis for 13- level inverter with RL load.

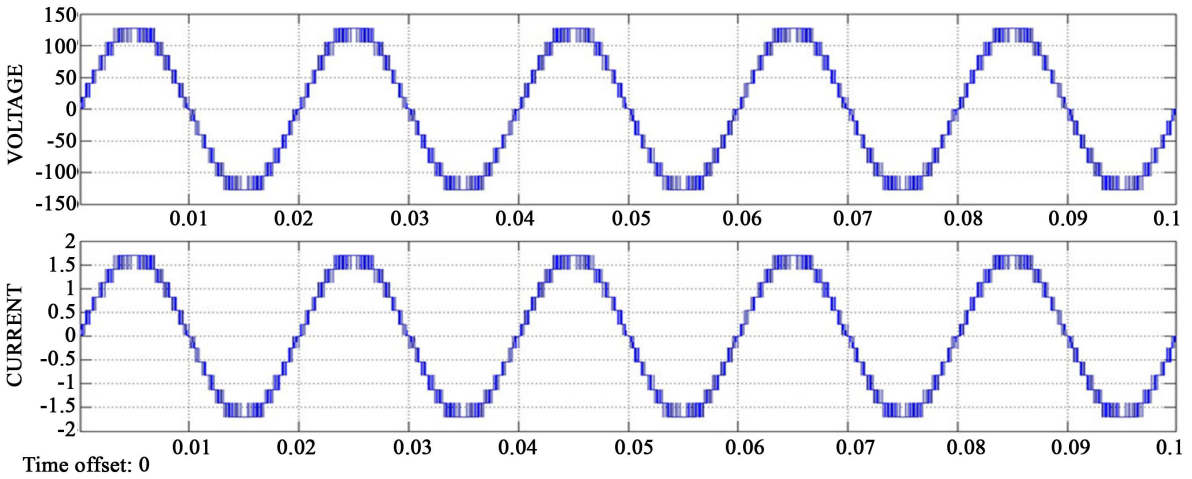

Figure 10. Output voltage and current waveform.

that the odd harmonics of 3rd, 5th, 7th, and 9th harmonic levels are most dominant. Hence a new method of SHEPWM is suggested for minimizing such kind of odd harmonics.

5. Selective Harmonic Elimination (SHE)

SHE is commonly adopted in medium and high power inverter applications where the switching frequency is low enough to minimize the switching losses. The effectiveness of this method is fully depends on switching angles. So, for determining the optimum switching angles several algorithms have been developed. Usually it is done using optimization techniques such as Newton Raphson method [8]-[11], Genetic algorithm (GA) and Particle swarm optimization (PSO). The digital implementation of SHE equations involves two steps.

1) The switching angles are too calculated through a set of non-linear and transcendental equations.
2) The determined switching angles are to be stored in look up table (LUT) for real time applications.

In order to implement this in real time power electronic applications [12], software based devices like microcontrollers, microprocessors and DSPs are preferred by design engineers. The programs are usually written in C or assembly languages. But the sampling rate and speed are limited because the programs are executed line by line and not simultaneously. These limitations are resolved by using FPGA. It is a digital hardware-based device

and it has become popular in prototype model for multilevel inverters due to their speed and flexibility.

In this paper for finding the values of switching angles the Newton Raphson method has been implemented which has a set of solutions to reduce the lower order harmonics. The main advantages of this SHE is to obtain lower order harmonics at the output side. If the inverter wants to supply AC power to an AC load with constant frequency a filter is usually installed in its output side. In this method when the lower order harmonics are eliminated the output will have only higher order harmonics and it should be attenuated by the filter. Hence the cut-off frequency will be increased which will results in filter size.

Solution for SHE Modulation

The output for 13-level inverter and the Fourier series can be expressed as

$$V_{inv}(\omega t) = a_0 + \sum_{n=1}^{\infty}\left[a_n \cos(\omega t) + b_n \sin(\omega t)\right] \tag{4}$$

The actual waveform consists of sine terms only.

The even harmonics are absent thus a_0 and a_n will be zero.

Thus the above equation is reduced to

$$V_{inv}(\omega t) = \sum_{n=1}^{\infty} b_n \sin(\omega t) \tag{5}$$

where

$$V_{inv}(\omega t) = \frac{2V_{dc}}{n\pi}\sum_{n=1,3,5}^{\infty}\left[\cos(\theta_1) + \cdots + \cos(\theta_6)\sin(\omega t)\right] \tag{6}$$

From the above equation the fundamental output equation can be expressed as

$$b_1 = \frac{2V_{dc}}{\pi}\left[\cos(\theta_1) + \cdots + \cos(\theta_6)\right] = V_1 \tag{7}$$

As shown in **Figure 2** the switching angles must satisfy the following condition:

$$0 < \theta_1 < \theta_2 < \cdots < \theta_6 < \frac{\pi}{2}$$

The modulation index is given by

$$M = \frac{\pi V_1}{2sV_{dc}} \quad (0 \le M \le 1) \tag{8}$$

As explained earlier, the main objective of this paper is to generate the output with the ability to eliminate the 3rd, 5th, 7th, 9th and 11th order harmonics. So in order to obtain the switching angles the following transcendental equations are solved.

$$\begin{aligned}
&\cos(\theta_1) + \cos(\theta_2) + \cdots + \cos(\theta_6) = 6M\\
&\cos(3\theta_1) + \cos(3\theta_2) + \cdots + \cos(3\theta_6) = 0\\
&\cos(5\theta_1) + \cos(5\theta_2) + \cdots + \cos(5\theta_6) = 0\\
&\cos(7\theta_1) + \cos(7\theta_2) + \cdots + \cos(7\theta_6) = 0\\
&\cos(11\theta_1) + \cos(11\theta_2) + \cdots + \cos(11\theta_6) = 0
\end{aligned} \tag{9}$$

Since it is difficult to solve the above equations analytically a different approach called Newton Raphson method is implemented to find the switching angles. The switching angles are then examined for their corresponding THD and is given by

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \tag{10}$$

where V_n is the rms value of the nth harmonic component and V_1 is the rms value of the fundamental component. The FFT analysis of 13-level inverter with R load for Mi = 0.97 using SHE technique is shown in **Figure 11**. The output obtained by using SHE equations is explained as follows. By using SHE technique the 3rd, 5th, 7th, and 9th harmonics are minimized by varying the modulation index from 0 to 1. For the modulation index 0.85,

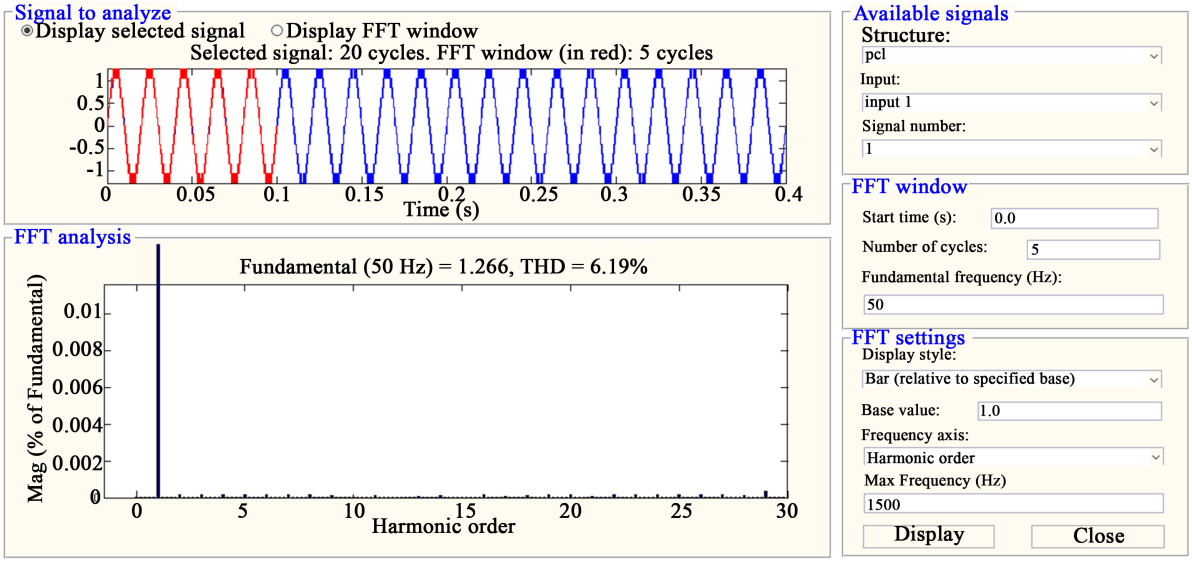

Figure 11. FFT analysis of 13-level inverter with R load for Mi = 0.97 using SHE technique.

the switching angles are 0.62, 23.10, 44.42, 54.37 and 63.57 the THD is 8.59%. If the modulation index is 0.97 the various switching angles are 4.82, 12.69, 23.32, 24.46, 37.27 and THD is around 6.19% which highly satisfies the IEEE 519-1992 harmonic guidelines. Thus if the modulation index has been increased the % THD would be reduced.

6. Experimental Results

The simulated output result using MATLAB/ SIMULINK model is verified with an experimental prototype hybrid cascaded multilevel inverter. The experimental setup of the proposed 13-level hybrid cascaded multilevel inverter model is shown in **Figure 12**. The model consists of switching pattern generation unit, power supply, driver circuit, user interface and 13-level output. A 6V dc source is given to the model to produce carrier wave signal. It is fed to FPGA processor to produce gating signals. The gate driver circuit is used to produce high power buffer stage between PWM control and gates of power switching device like IGBT. An opto-isolator (6N137) is used to isolate the control circuit from the power circuit.

The output result of the experimental setup is shown in **Figure 13** and **Figure 14** for the modulation index of Mi = 0.85 and Mi = 0.97 respectively.

The PWM waveform is produced by a ramping signal with a consistent level of DC source. The FPGA is designed specially by considering the needs of cost sensitive and high volume of electronic applications. The Spartan-3E processor has increased amount of logic per I/O then the earlier version and so the cost per logic cell is reduced. Hence the performance of the system is improved. Spartan-3E is ideally suited for wider range of consumer electronics including home networking, digital television, display/ projection and broadband access. The experimental results are compared with the matlab output and found that both the results are almost equal in amplitude and the level of THD which could meet the IEEE 519-1992 harmonic guidelines. The simulation result thus obtained by RL type load is ac current near sinusoidal output with p.f of 0.9 and THD is 1.09% which is shown in **Figure 15**. The FFT analysis for 13-level inverter with RL load is also shown in **Figure 9**. The value of R = 100 Ω, L = 0.7 mH and C = 6.8 μF.

7. Conclusion

The proposed topology of 13-level ACHMLI is experimentally verified with the satisfied results of MATLAB/ SIMULINK model. This topology is also simulated by using SHEPWM technique for minimizing the most dominant odd harmonics. The ratio (1:2:4) of the DC source voltage and the firing angle computation has performed to obtain a minimum THD value of the load voltage and current. Here the realization of the modulation index is also observed for maintaining the AC output voltage by varying the modulation index between $0 < m \leq 1$.

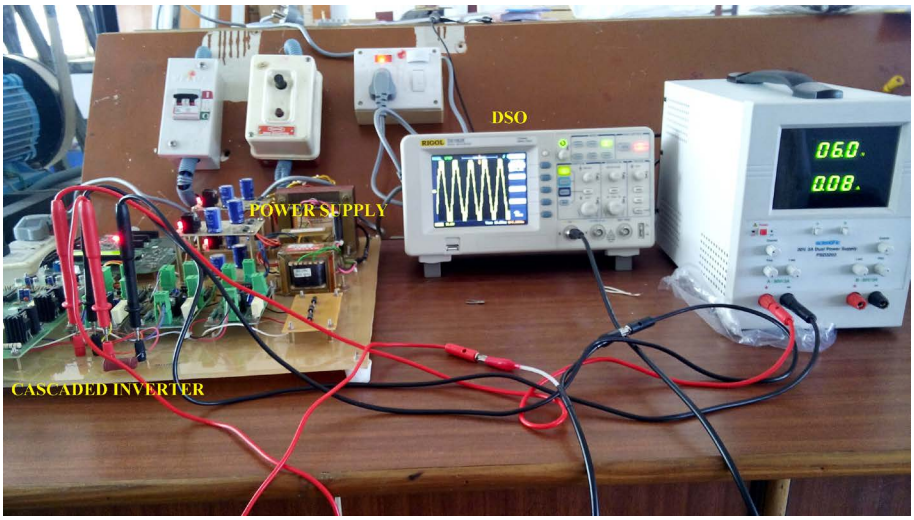

Figure 12. Experimental setup of proposed 13-level inverter.

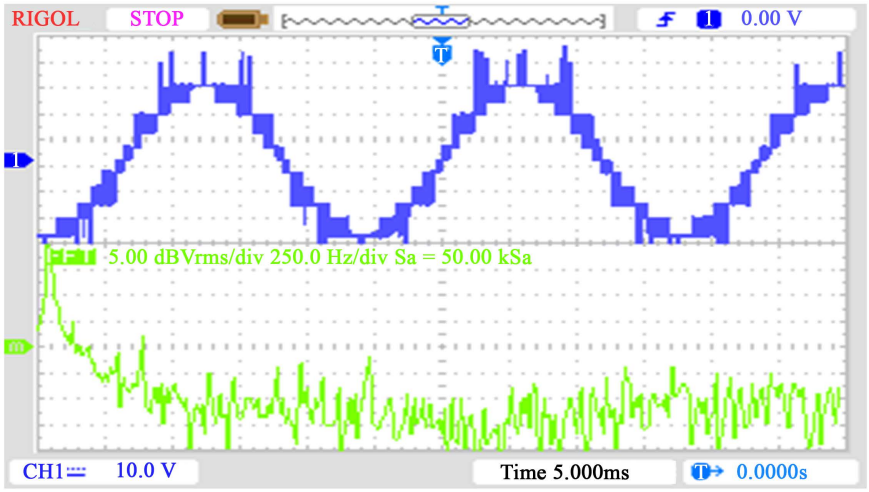

Figure 13. Hardware output of staircase waveform of proposed 13-level inverter for Mi = 0.85.

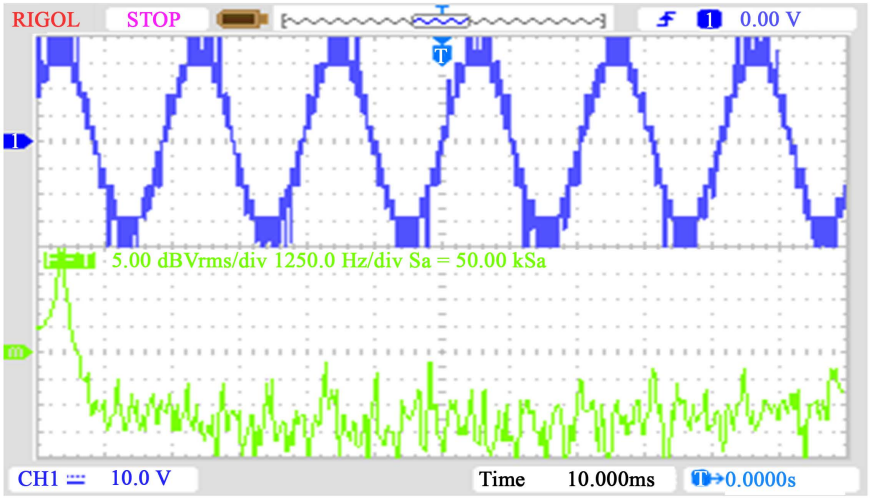

Figure 14. Hardware output of staircase waveform of proposed 13-level inverter for Mi = 0.97.

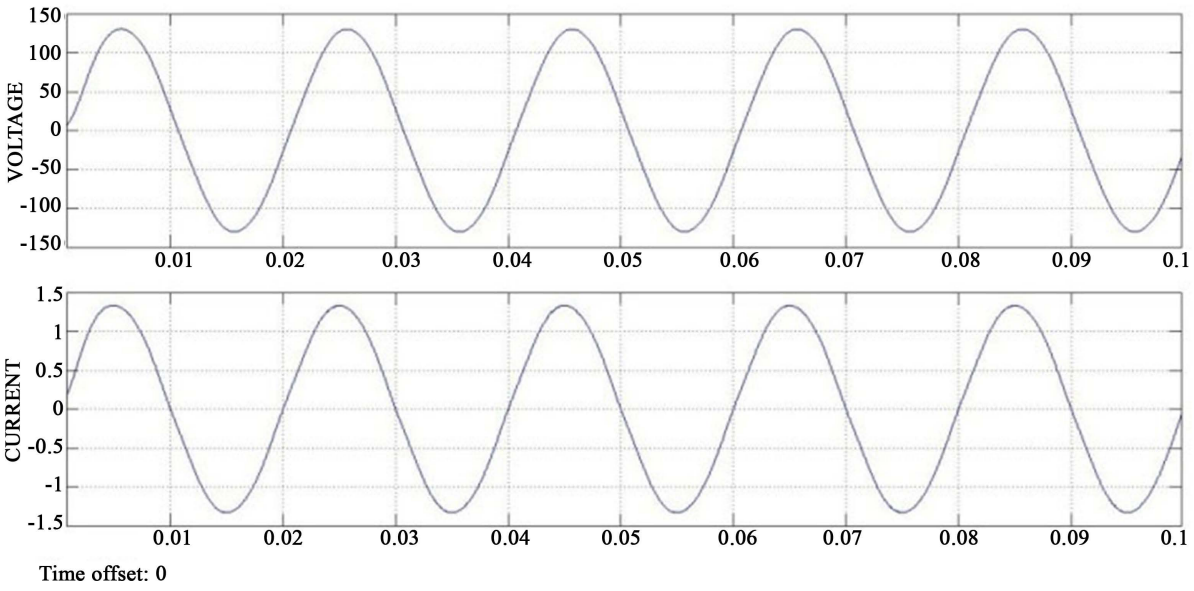

Figure 15. Simulation result for voltage and current obtained by RL type load.

This method shows that there is no power flow from load to any of the inverter cell. Hence the regeneration of power is avoided during the normal operating condition. From the above analysis by the comparison of output results, it is realized that the proposed model resulted lower THD level which could meet the IEEE 519-1992 standard. Also this can be used for any non-linear loads and solar photovoltaic application etc. Further the investigation is extended for PV applications by minimizing the switching losses with suitable DC converter and to find out the most suitable method for optimizing the lowest THD level.

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