

# An Improved Hybrid Space Vector PWM Technique for IM Drives

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## Abstract

In this paper, an improved hybrid space vector pulse width modulation (HSVPWM) technique is proposed for IM (induction motor) drives. The basic principle involved in the proposed random pulse width modulation (RPWM) cuddled SVPWM is amalgamating the pre-calculated switching timings for various sections of hexagonal space vector boundary and the random selection of carrier between two triangular signals, in order to disband acoustic switching noise spectrum with improved fundamental component. The arbitrary selection between triangular carriers, which is decided by digital signal states (Low or High) of the linear feedback shift register (LFSR) based pseudo random binary sequence (PRBS) generator. The SVPWM offers a control degree of freedom in terms of positioning of vectors inside every sampling interval and hence it has six possible variants of the voltage vectors arrangements in each sector. The developed HSVPWM is thoroughly analyzed in using the MATLAB® based simulation for all SVPWM variants. From the simulation and experimental results viz. harmonic spectrum, harmonic spread factor (HSF), total harmonic distortion (THD) etc., and the superiority of the proposed scheme such as better utilization of DC bus and the randomization of the harmonic power are evidenced. For the practical implementation, Xilinx XC3S500E FPGA device has been used.

## Keywords

Harmonic Spread Factor, Hybrid Space Vector Pulse Width Modulation, Pseudo Random Binary Sequence, Random Pulse Width Modulation

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## 1. Introduction

The main aim of any modulation technique employed in voltage source inverters (VSIs) is to obtain variable

output having a maximum fundamental component with minimum distortion. In a sinusoidal pulse width modulation (SPWM), a sinusoidal reference signal at desired output frequency is compared with a triangular waveform to generate the required duty cycles. The drawback of this technique is that it generates a fundamental term with limited amplitude, a significant amount of undesired carrier frequency harmonics and increased switching losses [1] whereas the advantage is being larger dead band between the fundamental and the first dominant harmonics. These high switching frequency schemes ease the filtering effort but a low frequency switching scheme which inherently suppresses the lower order harmonics can offer reduced switching losses.

Space vector pulse width modulation (SVPWM) is a method of pre-calculation of switching the timing instants for various sections of target output which has options in terms of positioning the active vectors inside every sampling interval [2] [3]. The SVPWM claims reduced distortion and enhanced the fundamental component when compared with the SPWM. The space vector theory, which involves rotating reference and hexagonal boundary (and triangular sectors) offers a control degree of freedom in selecting in active vectors and null vectors [4] [5]. The performance of the SVPWM technique is considerably influenced by selection of null vectors and their positioning [6]. These multiple options in selecting the null vectors and forming a combined sequence with active vectors render six different space vector patterns [7] [8]. Due to the deterministic PWM/SVPWM switching of the inverters, the motor generates an unpleasant acoustic switching noise and a mechanical vibration [9] and the best way to reduce the audible switching noise radiated from the induction motor is to increase the switching frequency up to 20 kHz. By using such method, noise problem can be solved, on the other hand it increases the switching losses of the inverter [10].

Random PWM (RPWM) methods have attracted attention from 1987 as a solution to the above problem. In a typical RPWM, the duty cycle is computed by comparing the sinusoidal reference wave with the randomly composed triangular carrier using two triangular waves each of the same has fixed frequency, but of opposite the phase [11]. These undeterministic PWM methods spread the harmonic power as demanded by modern drives and their influential variation in fundamental term and THD are negligible. More numbers of RPWM schemes have been investigated, which differ in how the randomness is incorporated in the carrier signal. A pseudo random triangular carrier modulation method and its harmonic spread effect have been discussed [11]. In addition, Chaos-based PWM strategies have also been discussed, whereas it utilizes a chaotic changing switching frequency to spread the harmonics continuously to a wideband area, so that the peak harmonics could be reduced greatly [12].

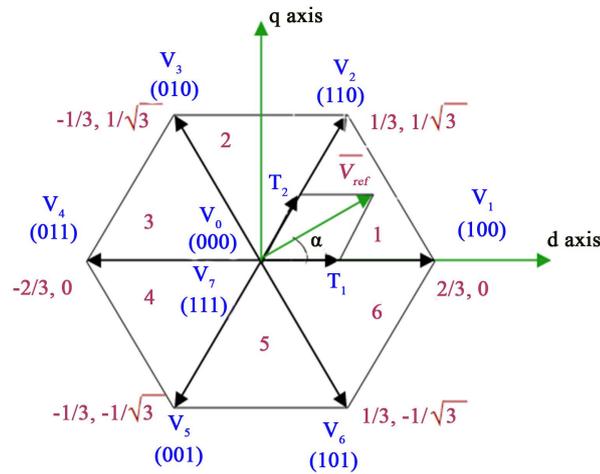
A discontinuous PWM method has exhibited better performance with higher modulation range which is mandatory for high power applications [13]. Field programmable Gate Arrays (FPGAs) have become one of the most popular implementation media for digital circuits, and their preamble in 1984. The key to success of FPGAs is their programmability which allows any circuit to be instantly composed out by appropriate programming [14]. Even though the SVPWM patterns offer the major requirements of the drives and conceptually suite with modern speed control methods, clustering of harmonics around a specific frequency is objectionable. RPWM methods performs well in terms of secondary issues like spreading the harmonic power etc. while the primary issues related parameters like improved fundamental, reduced THD and higher dead band separation for harmonics are not appreciable. In this paper, a modified SVPWM strategy is developed by using FPGA which performs similar to conventional SVPWM in primary issues but with improved secondary issues like harmonic spreading effect.

## 2. Space Vector Modulation Switching Patterns

Space vector pulse width modulation is a digital PWM method, in which, the duty cycles of gating pulses are pre-calculated for every sections of target output cycle [5] [6]. At any instant in a particular sector, two vectors need to be participated in variable timing intervals to establish the target vector as indicated in **Figure 1**. The effective switching instants are calculated as follows.

$$T_1 = \frac{\sqrt{3}}{V_{dc}} \times \left( T_z \times V_{ref} \times \left( \sin\left(\frac{n\pi}{3}\right) \times \cos \alpha - \cos\left(\frac{n\pi}{3}\right) \times \sin \alpha \right) \right) \quad (1)$$

$$T_2 = \frac{\sqrt{3}}{V_{dc}} \times \left( T_z \times V_{ref} \times \left( \cos\left(\frac{(n-1)\pi}{3}\right) \times \sin \alpha - \cos \alpha \times \sin\left(\frac{(n-1)\pi}{3}\right) \right) \right) \quad (2)$$



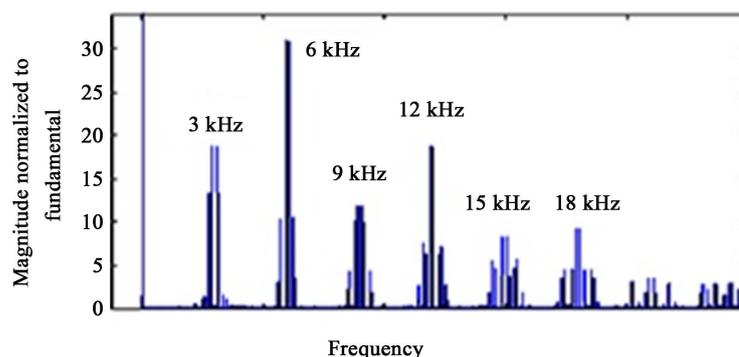
**Figure 1.** Principle of SVPWM.

where,  $T_1$ ,  $T_2$  and  $T_0$  are computed switching instants for the lagging, leading and zero switching vectors, “ $n$ ” is the sector number (Sectors 1 to 6),  $T_s$  is sampling time,  $f_c$  is switching frequency and  $\alpha$  is the instantaneous phase angle of  $V_{ref}$  ( $0^\circ \leq \alpha \leq 360^\circ$ ). The freedom in space vector modulation (SVM) is the choice of formulating the switching patterns [6]. The basic idea behind the any SVM pattern is the average voltage resulted in a sampling interval is same, but if the contributing vectors are switched for their computed times ( $T_1$  and  $T_2$ ) with appropriate null vector and the sequence. In contrary, the different patterns not only offer merits like unit transition, reduced switching losses, ease of implementation etc. but also performance differences in terms of fundamental component value and THD. The clues of the patterns’ variation are detailed below.

The choice of the zero vectors—(i) contribution of  $V_7$  (111) or  $V_0$  (000) or both for pattern formation, (ii) sequencing of the vectors (clockwise reference vector rotation and anti-clockwise reference vector rotation) and arrangement of leading, lagging and null vectors, (iii) and splitting of the duty cycles of the vectors without introducing additional commutations. Based on the above clues, six patterns are formulated. It is worth noting that according to the theory of SVM, the reference vector is contributed just by active vectors, not by null vectors. The involvement of null vectors may facilitate the digital implementation and also helps in solving few practical circuit complications. Avoidance of the null vectors may create a problem in inverter bridges that use isolation circuits such as bootstrap. The reason is that the lower leg of the inverter is switched on or off for extended periods of time. Pattern I: An unique switching pattern is followed for each sector and can be summarized as  $V_0$  (000),  $V_1$  (100),  $V_2$  (110),  $V_7$  (111),  $V_7$  (111),  $V_2$  (110),  $V_1$  (100),  $V_0$  (000) for sector 1. Where,  $V_1$  and  $V_2$  ( $V_1 + 60^\circ$ ) are the forming (contributing) vectors in the sector 1. For the consecutive sector (Sector 2) the respective contributing vectors,  $V_2$  and  $V_3$  are used in place of  $V_1$  and  $V_2$ . Pattern II: This pattern is similar to pattern I, but only the null vector  $V_0$  is involved in all sectors along with two active vectors. Pattern III: This pattern is similar to pattern II, but the null vector  $V_7$  is engaged instead of  $V_0$ . Pattern IV: This pattern has two different vector sequences for odd numbered (1, 3, 5) and even numbered (2, 4, 6) sectors. With the contribution of vectors, odd sectors and even sectors use  $V_7$  and  $V_0$  as null vectors respectively. Pattern V: In this pattern, the null vector assignment is swapped while comparing to the pattern IV. That is,  $V_0$  is considered for odd sectors and  $V_7$  for even sectors. Pattern VI: This pattern is similar to pattern II, but the assignment of active vectors  $V_1$  and  $V_2$  are swapped.

### 3. Problem Formulation

The PWM techniques can be broadly classified as deterministic PWM schemes and non-deterministic PWM schemes. The conventional PWM schemes viz. SPWM, SVPWM, selective harmonic elimination PWM (SHEPWM) etc. are examples for deterministic PWM schemes. The RPWM schemes are non-deterministic PWM schemes. The deterministic PWM schemes are operated at constant switching frequency in a modern drive system [1]-[5]. In any deterministic PWM with carrier frequency,  $f_c$  (say 1.5 kHz), the harmonic spectrum possesses the clustered harmonics at its multiples ( $2f_c$ ,  $4f_c$ ,  $6f_c$  etc.) as shown in **Figure 2**.



**Figure 2.** Output voltage harmonic spectrum of SPWM.

The acoustic noise emitted by the motor is very annoying under this condition since the majority harmonics comes within the audible range (20 Hz - 20 kHz). These clustered harmonic spectra will produce acoustic noise, electromagnetic interference (EMI), mechanical vibration and hence paves a possibility of physical damage to the rotor. The best way to reduce the audible switching noise is radiated from the induction motor is to increase the PWM switching frequency up to 18 kHz. Such a method can solve the noise problem but increases the switching loss of the inverter [12]. In general, the 1 - 10 kHz range is the region of the greatest annoyance for human listeners. Unfortunately, this range may coincide with the switching frequency of the VSI quite often. Hence it is important that the acoustic noise radiated from the induction motor, with a frequency below 10 kHz should be reduced. In recently, to overcome this problem, a new host of techniques called RPWM has been proposed. The basic requirement of applications, which demands acoustic noise and vibration free working in harmonic spectrum involving more number of harmonics none having dominant magnitude (say > 5% of fundamental) rather than the spectrum of less number of dominant harmonics. This feature is otherwise known as spreading of harmonic power. RPWM methods contribute to dispersing of harmonics with same (range of) switching frequency as that of deterministic PWM methods. The RPWM technique is operating at variable switching frequency. By selecting the carrier triangle wave in a random manner, the above said problems are mitigated as understood from [Figure 3](#).

All the previous attempts in changing the reference wave were towards the fundamental enhancement and THD reduction. The reformation of harmonic spectrum like spreading the harmonic power must be done through carrier modification/randomization. The recent solution for above said problems is RPWM, where switching frequency is selected within the audible range (hence reduced switching losses) with an intelligent randomness so that no objectionable audio noise is produced.

#### 4. Proposed Hybrid Scheme

An ingenious PWM schemes, which amalgamates the features of SVPWM and RPWM is the need of any modern ac drive system. Conceptually the SVM suggests six different references (analog equivalent) for the better most of THD and the enhanced fundamental. It does not offer any guidance on carrier selection and suggests the usage of conventional triangular carrier. Opportunely, the randomness addition in the RPWM is in carrier wave and restricted within the carrier cycle. This paves the way to amalgamate the random carrier with the SVPWM irrespective of the pattern preference.

The implementation accuracy of any computation intensive PWM largely depends on the implementation platform and the algorithm used. The proposed hybrid SVPWM (HSVPWM) adds both timing computation and carrier randomness to its complexity, and demands great care in implementation. The implementation of the HSVPWM is done with the help of an architecture as shown in [Figure 4](#). The HSVPWM architecture consists of three functional blocks namely, SVM reference generator block, carrier generation and selection block, and pulse generation block. The SVM reference generator block has the timing equations and a reference position in incremental mechanism. For every incremental position the instants of active and null vectors are computed and used for forming three-phase references. In the carrier generation and selection block, normal triangular carrier (+fc) and inverted triangular carrier of same frequency (-fc) are given as input to the 2:1 multiplexer. Choice of triangle called winning triangle depends up on the output of the LFSR based 8 bit random bit generator. The

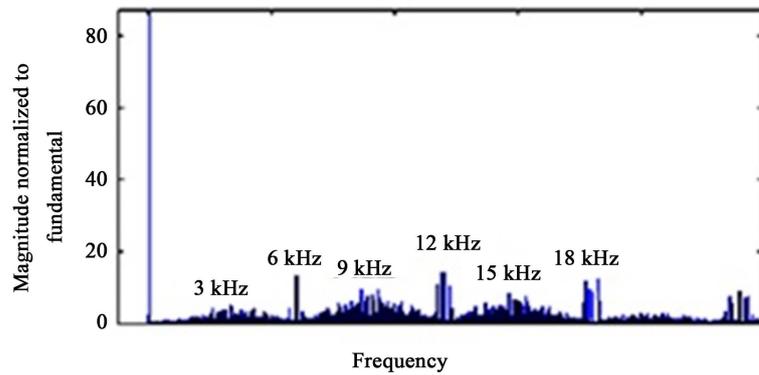


Figure 3. Output voltage harmonic spectrum of RPWM.

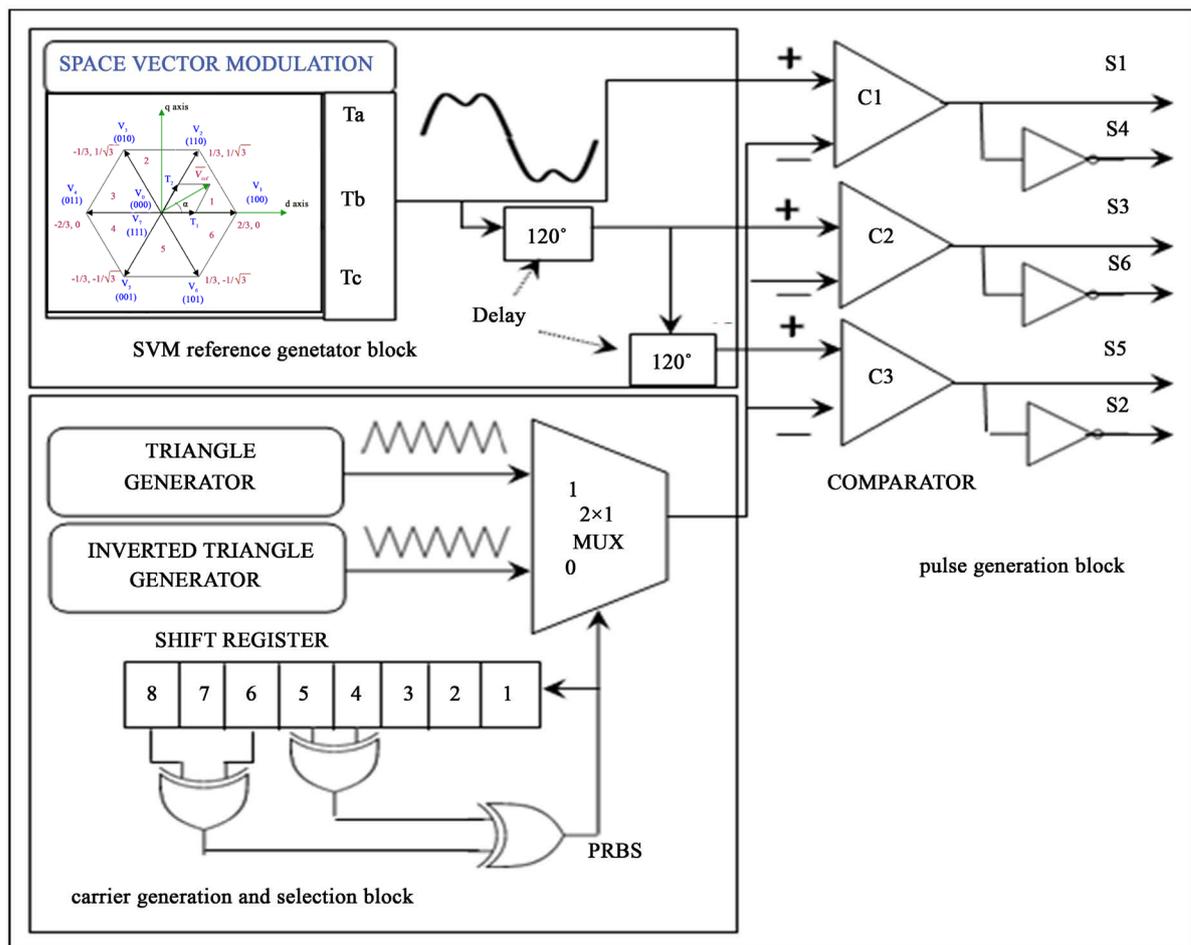


Figure 4. Proposed HSVPWM method.

pulse generation block compares the references with the randomized carrier and generates the pulses for the six switches of VSI. In case the output is “1” then the winning triangle is +fc triangle otherwise the winning triangle is -fc triangle as shown in Figure 5. This characteristic makes more continuous distribution.

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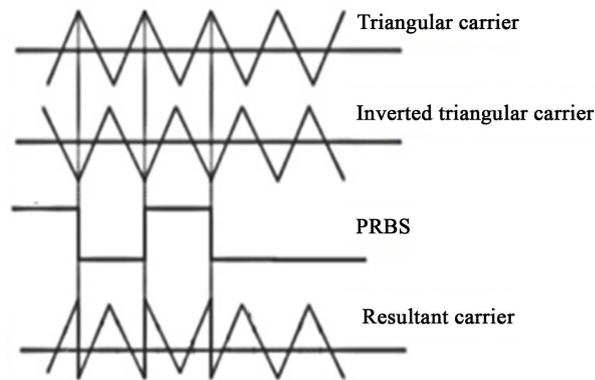


Figure 5. Generation of random triangular carrier.

“1” then the winning triangle is  $+f_c$  triangle otherwise the winning triangle is  $-f_c$  triangle as shown in Figure 5. This characteristic makes more continuous distribution.

## 5. Discussion of Simulation Results

A simulation study is carried out using MATLAB 7.9b software with ode23tb solver. Conventional simulation study for the kind of calculation involves understanding the various waveforms, harmonic study (fundamental and other harmonics) and THD along with spectrum. Another performance parameter harmonic spread factor is a simple quality indicator would be useful for evaluating the harmonic spread effect of the random PWM scheme. The factor is named as harmonic spread factor (HSF) and uses the concept of statistical deviation. The HSF [10] [11] is defined as follows:

$$\text{HSF} = \sqrt{\frac{1}{N-1} \sum_{j>1}^N (H_j - H_0)^2} \quad (3)$$

$$H_0 = \sum_{j>1}^N (H_j) / (N-1) \quad (4)$$

where, “ $H_j$ ” is amplitude of  $j$ th harmonics, “ $H_0$ ” is average value of all “ $N - 1$ ” harmonics. The HSF quantifies the harmonic spectra spread effect of any PWM scheme and it should be small. For ideal flat spectra of white noise, the HSF would be zero. A theoretical comparison of line to line voltage performance indices are presented in for dc bus voltage  $V_{dc} = 415$  V, fundamental frequency  $f_1 = 50$  Hz and average switching frequency  $f_c = 1.5$  kHz with the inverter feeding a 0.75 kW, 415 V, 50 Hz, three-phase squirrel cage induction motor. The switches are considered to be ideal. The simulation results of the harmonic spectra for pattern I of HSVPWM ( $M_a = 0.8$ ) is given in Figure 6.

The performance parameters (fundamental voltage, THD and HSF) are carried out by using FFT window in MATLAB simulation tool with one cycle of line to line voltage. Table 1 and Table 2 show that all the performance assessment of RPWM and all the patterns of SVPWM, HSVPWM. From the assessment, SVPWM pattern I contributed well while compared with the other patterns. But pattern II of the SVPWM has given very low fundamental because of poor dc bus utilization. Usually, randomness effects of the SVPWM patterns are low when compared with the superimposed RPWM which is mainly designed to disperse the predominant harmonics. From the view of HSF, the performance of SVPWM pattern I is good above the linear modulation; But RPWM is better where the modulation index range is in between 0.2 to 0.8. From the table, fundamental component of the RPWM is low when compared with the SVPWM pattern I for all the levels of modulation indices, But while comparing other patterns, RPWM has given reasonably good results for higher linear modulation indices ( $M_a = 0.8$  to 1.0). The SVPWM higher order patterns (3, 4, 5 and 6) have performed similarly not better than the pattern I and not lesser than the pattern II. Figure 7 and Figure 8 show the convenient three dimensional graphical representation of the fundamental and THD of all the methods. From the representation, while increasing the modulation indices, fundamental component also increases and the value of THD decreases.

Figure 9 shows fruitful three dimensional graphical line representation of the significant HSF for all the methods. After the progress of the HSVPWM patterns, the fundamental value and the THD of the HSVPWM patterns

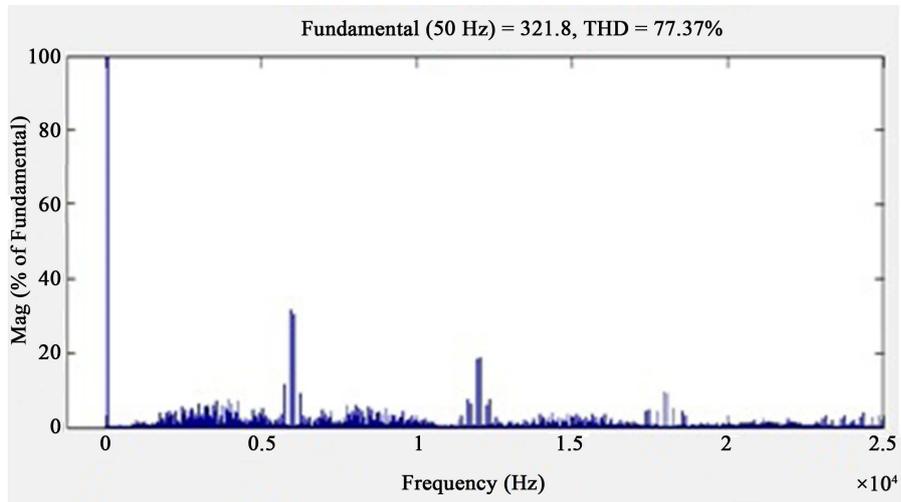


Figure 6. Line voltage spectra of HSPWM.

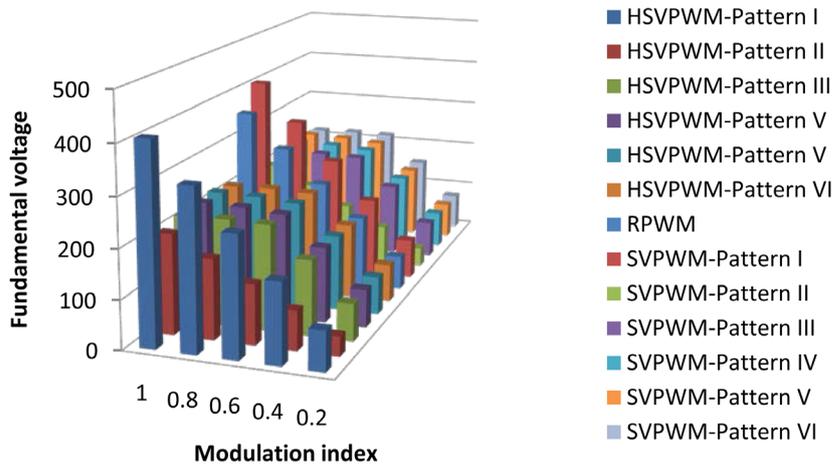


Figure 7. Fundamental assessment.

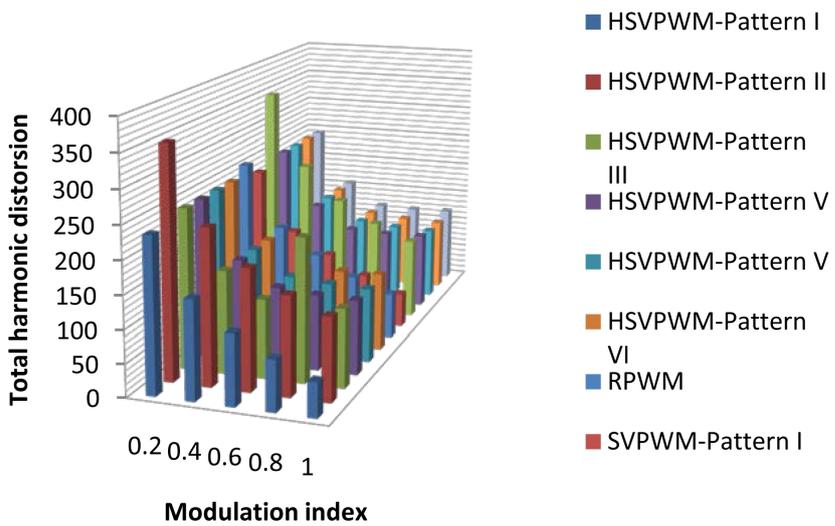


Figure 8. THD assessment.

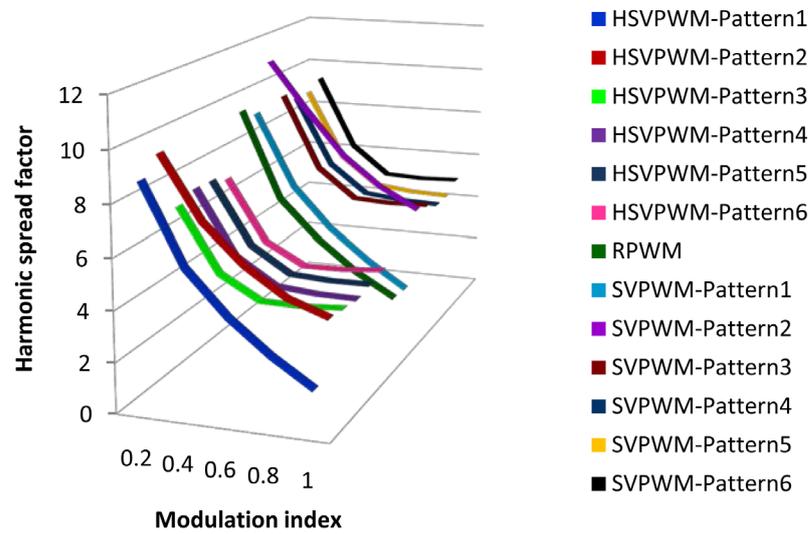


Figure 9. HSF assessment.

Table 1. Fundamental and THD assessment of SVPWM, RPWM and HSPWM.

M <sub>a</sub>	SVPWM patterns						RPWM	HSPWM patterns					
	I	II	III	IV	V	VI		I	II	III	IV	V	VI
<b>Fundamental voltage</b>													
0.2	81.94	40.44	76.46	76.8	76.27	76.65	69.54	81.73	40.36	76.47	76.84	76.41	76.6
0.4	163.7	81.25	154.2	153.8	153.5	153.6	146.4	163.5	81.25	153.7	154	153.8	154
0.6	245.5	122	215.6	215.2	214.6	215.8	214.1	245.2	122.1	215.9	214	214.9	215.3
0.8	325.9	163.3	218.1	220.8	220	217.4	284.4	327.8	163.3	218.1	220.6	220.8	217.6
1	406.5	203	216	222.5	222.5	215.9	355.3	408.3	204.1	216.4	222.24	222.6	215.7
<b>THD</b>													
0.2	234.47	351.2	244.44	244.17	244.74	243.85	258.62	235.0	351.8	244.64	244.26	244.45	244.27
0.4	144.24	236	155.79	156.19	156.61	156.4	161.6	149.4	236.3	156.29	156.14	156.39	155.94
0.6	106.85	182.97	119.4	119.65	120.06	119.62	122.25	107.0	183.1	119.42	119.84	119.7	119.73
0.8	77.73	149.58	117.35	114.49	114.9	117.75	91.79	77.37	149.7	217.43	114.63	114.69	117.79
1	52.84	125	118.83	112.8	112.8	119.25	70.18	52.72	125.9	118.89	112.94	113.01	119.27

Table 2. HSF assessment of SVPWM, RPWM and HSPWM.

M <sub>a</sub>	SVPWM patterns						RPWM	HSPWM patterns					
	I	II	III	IV	V	VI		I	II	III	IV	V	VI
<b>HSF</b>													
0.2	9.12	11.09	9.30	8.90	8.90	9.27	9.52	8.79	9.46	7.06	7.36	7.31	7.01
0.4	6.09	9.06	6.16	5.99	6.00	6.18	5.93	5.68	6.98	4.53	4.77	4.78	4.50
0.6	4.38	7.19	4.92	4.77	4.79	4.93	4.34	3.99	5.47	3.62	3.74	3.76	3.64
0.8	3.12	5.95	4.83	4.59	4.60	4.85	3.10	2.70	4.39	3.59	3.60	3.66	3.66
1	2.07	5.08	4.89	4.53	4.54	4.91	2.15	1.65	3.83	3.70	3.57	3.68	3.81

in all the modulation indices are almost equal to SVPWM patterns. But amazingly the HSF of the HSPWM patterns (except pattern II) are superimposed when compared to the existing SVPWM and RPWM schemes. For higher linear modulation indices ( $M_a = 0.8$  to  $1.0$ ), HSPWM pattern I has given a higher harmonic spreading effects (less HSF) when compared with the other HSPWM patterns. But for lesser than  $0.8$  modulation indices the pattern I is less performing while comparing with the higher order HSPWM patterns (3 to 6).

The superlative values of performance indices are underlined in **Table 1** and **Table 2**. The improvements of the HSPWM are clearly depicted in **Table 1** and **Table 2**. By comparing the simulation results, the proposed HSPWM not only afford the better performance in terms of fundamental voltage and THD than conventional SVPWM and RPWM, but also provide less harmonic spread factor which results in reduced acoustic noise. In comparison, **Table 3** shows that the percentage of improvement of the HSPWM (pattern I) is better than the SVPWM (pattern I) and RPWM. For modulation index  $1.0$  HSF improvement of the HSPWM  $20.29\%$  more than the SVPWM and  $23.26\%$  is better than the RPWM

Fundamental improvement of HSPWM  $0.44\%$  is more than the SVPWM and  $28.44\%$  more than the RPWM for modulation index  $1.0$ . In HSPWM,  $0.23\%$  of the THD has been decreased when compared with SVPWM and  $24.88\%$  decreased when compared with RPWM for the modulation index  $1.0$ . **Table 4** represents, noticeable dominating harmonic orders affecting the performance of the inverter fed drives system. The clustered of harmonics at its multiples ( $2fc =$  order  $62, 58$  and  $56$ ) are existing in the harmonic spectrum of the SVPWM and RPWM ( $2fc =$  order  $60$ ), whereas these are having less than  $5\%$  of the magnitude in HSPWM.

## 6. Discussion on FPGA Synthesis Results

The recent developments in the field of VLSI made FPGAs as one of the major components in high performance processors especially in the area of power conversion utilities [14]. The VHDL has been used to design the proposed

**Table 3.** Percentage of improvement of HSVM.

$M_a$	% of improvement HSVM (pattern I) over SVM(pattern I)			% of improvement HSVM (pattern I) over RPWM		
	Fundamental	THD	HSF	Fundamental	THD	HSF
0.2	-0.26%	-0.24%	3.62%	17.53%	9.12%	7.67%
0.4	-0.12%	-3.58%	6.73%	11.68%	7.55%	4.22%
0.6	-0.12%	-0.21%	8.90%	14.53%	12.42%	8.06%
0.8	0.58%	0.46%	13.46%	15.26%	15.71%	12.90%
1	0.44%	0.23%	20.29%	14.92%	24.88%	23.26%

**Table 4.** Dominating harmonic order and their magnitude.

Dominating harmonics for $M_a = 0.8$					
SVPWM(pattern I)		RPWM		HSPWM(pattern I)	
D-H-O	magnitude (% of Fundamental)	D-H-O	magnitude (% of Fundamental)	D-H-O	magnitude (% of Fundamental)
119	30.93	121	40.01	119	31.35
121	30.83	119	38.16	121	30.28
62	18.69	241	13.84	241	18.79
239	18.69	239	12.6	239	18.25
58	18.63	245	10.63	115	11.51
241	18.56	60	10.48	359	9.36
56	13.19	167	9.82	361	9.03

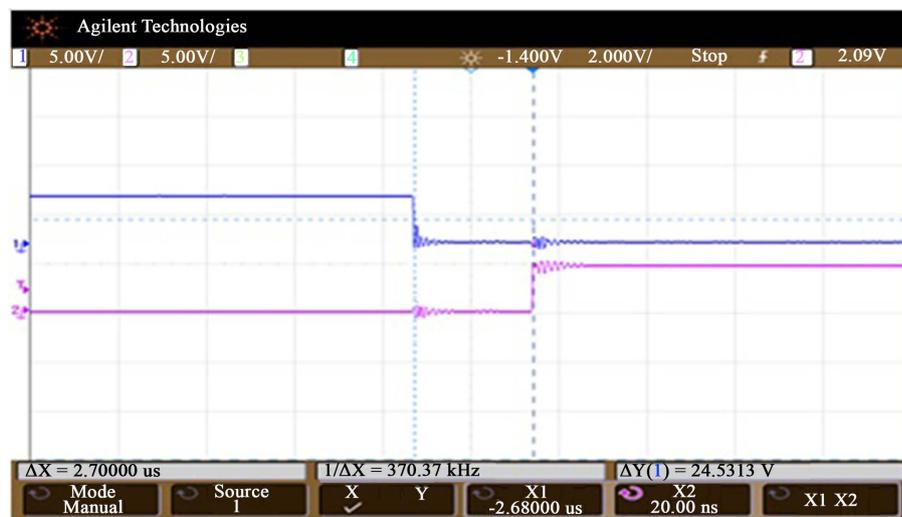
method and the synthesis results have been acquired from Xilinx project navigator tool. The XC3S500E-5fg320, 90 nm low cost FPGA device is used for real time exploitation. A 50 MHz board clock has been used for sequential circuit design. In this work, 16% of look up tables are utilized. 15% DSP based 18x18 multipliers are used for development of carrier and reference waves. A Xilinx power estimator tool is used to estimate the power analysis. In this scheme, dissipation of the static power is 78 mW and the Dynamic power is 32 mW. Total power dissipated by FPGA device is 110 mW. This power analysis has been taken for typical process with commercial grade, ambient temperature is 25°C and Vccint voltage is 1.2 V.

## 7. Experimental Results

To validate the analysis and simulations in the previous sections, a laboratory experimental setup has been assembled as shown in **Figure 10**. The set-up consists of a 0.75 kW, 415 V, 50 Hz three-phase squirrel cage induction machine fed from a 2 kW intelligent power module based IGBT inverter. Spartan3E- XC3S500E FPGA is used as the controller platform. A dead time of 2.7  $\mu$  seconds is inserted between the switches of the same inverter leg in order to ensure smooth transition of the switching states of the inverter shown in **Figure 11**. In both the conventional and proposed schemes, the tests are carried out with the 50 Hz fundamental frequency of the inverter voltage. **Figure 12** represents the Yokogawa precision power analyzer window for measuring the line to line voltage and line current of the proposed HSVPWM scheme. In comparing the simulation results with experimental results clearly depicts that both results are very similar, and harmonic spectra spread effect is most excellent in the hybrid scheme as shown in **Figure 13**.



**Figure 10.** Experimental hardware setup.



**Figure 11.** Dead time measurement by Yokogawa precision power analyser.

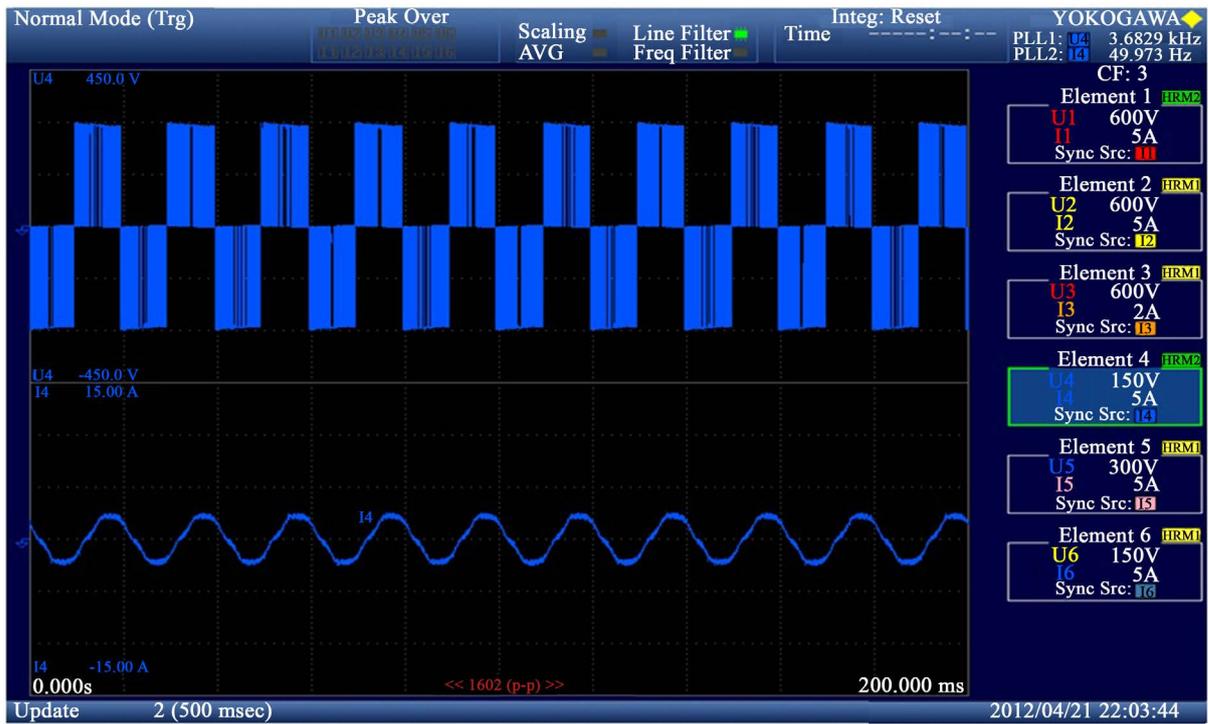


Figure 12. Experimental results of the line-line voltage and line current with  $M_a = 0.8$  for HSPWM.

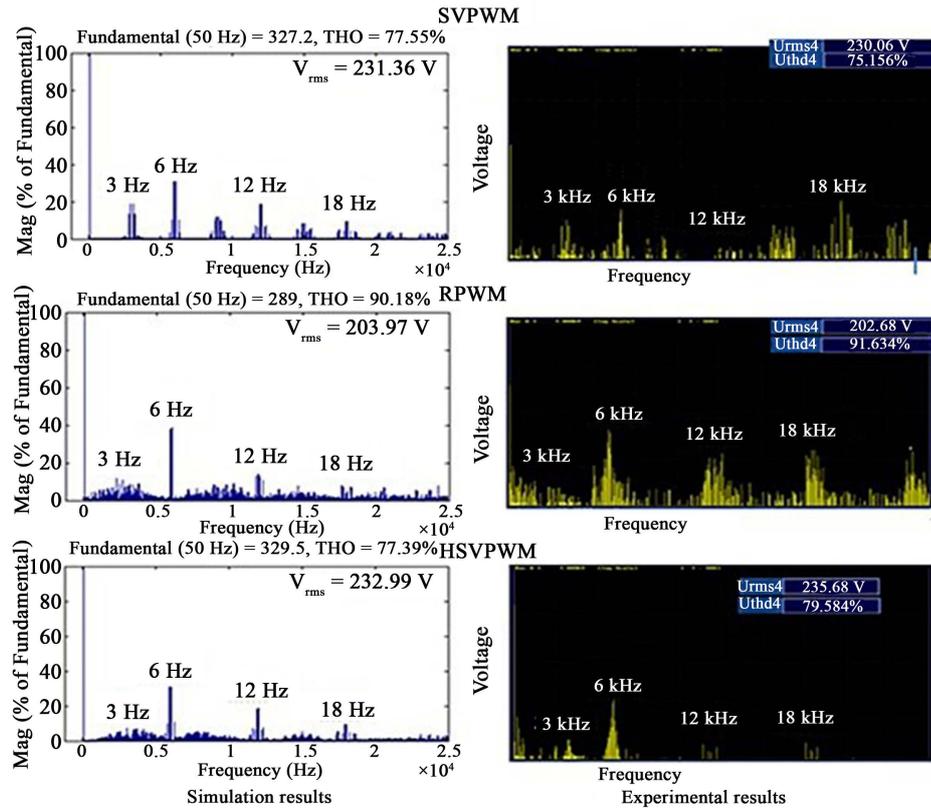


Figure 13. Comparison of simulation results with experimental results of voltage harmonic spectrum for  $M_a = 0.8$  (harmonic order from 0 to 500).

## 8. Conclusion

In this paper, a hybrid Space Vector PWM switching patterns for three phase voltage source inverter is proposed. The main idea of the proposed PWM strategy is to combine the merits of both the SVPWM and RPWM. The HSVPWM is compared systematically with its counterparts SVPWM and RPWM. The results evidenced the success of the HSVPWM methods in term of improved fundamental component, reduced THD and minimal HSF. The strategy finds it suitability with the modern ac drives for noise free working. In addition, this method, blended successfully with FPGA, occupies less area and achieves low propagation delay with very less power dissipation. In future, more randomization can be performed by using 16 bit or 32 bit LFSRs.

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