Circuits and Systems, 2016, 7, 506-519
Published Online April 2016 in SciRes. http://www.scirp.org/journal/cs
http://dx.doi.org/10.4236/cs.2016.74043

Asymmetric Three-Phase Cascading Trinary-DC Source Multilevel Inverter Topologies for Variable Frequency PWM

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Received 27 February 2016; accepted 26 April 2016; published 29 April 2016

Abstract

Asymmetric three-phase cascading Trinary-DC source Multilevel Inverter which can achieve reduced harmonics and superior root mean square (RMS) values of the output voltage is proposed. This topology can achieve cascaded full bridge inverter operation with dissimilar (unequal) DC Source and it is fired by using variable frequency pulse with modulation technique as a switching strategy. This pulse width modulation switching strategy has a newly adopted multicarrier single reference technique. The performance parameter factors like Form Factor (FF), Crest Factor (CF), Total Harmonic Distortion (THD) and fundamental RMS output voltage (V_{RMS}) are estimated by using proposed asymmetrical three-phase cascading multilevel inverter for several modulation indices (0.8 - 1). The research study carries with MATLAB/SIMULINK based simulation and experimental results obtained using appropriate prototype (test board) to prove the viability of the proposed concept.

Keywords

Trinary Multilevel Inverter, Variable Frequency Pulse Width Modulation, Total Harmonic Distortions, Trinary-DC Source, Distortion Factor

1. Introduction

Multilevel inverter has a strained incredible interest in high-power and medium voltage applications, because it has several benefits: it has high-voltage and high-power output over the use of power semiconductor switching devices without the use of a transformer. Whenever, the quantity of the output voltage level increases, the total harmonic distortion of the output voltage and current waveform of a multilevel inverter will reduce. A new ap-

How to cite this paper: Irusapparajan, G. and Periyaazhagar, D. (2016) Asymmetric Three-Phase Cascading Trinary-DC Source Multilevel Inverter Topologies for Variable Frequency PWM. *Circuits and Systems*, **7**, 506-519.
http://dx.doi.org/10.4236/cs.2016.74043

proach for modulation of an 11-level cascade multilevel inverter using selective harmonics elimination technique is given in [1]. The authors [2] proposed topology of a digital control of a three-phase three-stage hybrid multilevel inverter with 18-level output voltage containing minimum switching losses.

The design and implementation of a fresh type of multilevel inverters are given in [3] using cascading of a two three-phase three-level inverters. The control of cascaded asymmetrical type of multilevel inverters using one DC source on circuit is proposed [4]. Single-phase multilevel inverter operations with battery balancing operation with reduced harmonic content presence in the output voltage are proposed by authors in [5]. Application of multilevel inverter with direct drive wind turbine grid interfacing is also discussed in the literature [6]. The three-stage 27-level inverter using "H" bridge [7] converter is analyzed for average and high-power machine drive applications, and trinary type asymmetric 81-level multilevel inverter for STATCOM application [8]. In [9] the authors' present theoretical analysis of CM converters with increased voltage levels, by maintaining this high quality voltage, regeneration in motor mode can be avoided.

A new asymmetrical type of cascaded multilevel inverter with series combinations of several inverter circuits is proposed in [10]. A single-phase photovoltaic (PV) system integrating segmented energy storages (SES) using cascaded multilevel inverter is given in [11]. The design of modular multilevel cascaded inverter based on double-star bridge cells is proposed in [12] using experimental verification. A hybrid five level inverter topology [13] with common-mode voltage elimination for induction motor drives is implemented. The proposed topology in [14] is obtained by using cascading a five-level flying capacitor multilevel inverter with a flying "H"-bridge power cell in each phase using a single DC source [14]. The design of inverted sine PWM technology for asymmetrical cascaded multilevel inverter is used by the authors [15] to reduce the total harmonics distortion.

The design and implementation of cascaded multilevel inverter [16] is operating in current mode. The Neutral Voltage Modulation technique for multilevel cascade inverters under unbalanced dc-link conditions has been proposed in [17]. A novel single-phase five-level multilevel inverter proposed in [18] produces a five-level output voltage with only one DC source using coupled inductors [18]. A new technology of an improved PWM topology for chopper-cell-based modular multilevel converters is established in [19]. A latest converter configuration based on cascaded converter family unit is offered [20]. The recommended multilevel highly developed cascaded converter has settlement such as lessening in number of power semiconductor switches and its losses [20]. A generalized power loss algorithm for multilevel neutral-point clamped pulse width modulation technique is offered, which is appropriate to any level number of multilevel inverter [21]. A fifteen-level photovoltaic fed cascade multilevel inverter for the removal of certain harmonic orders is urbanized for the power quality development [22]. Fresh topologies for a cascade transformer sub-multilevel inverter with every sub-multilevel inverter consists of two DC voltage source with six power semiconductor switches to attain five-level output voltage [23]. An asymmetrical cascaded half-bridge multilevel inverter for 3 hp fuel cell electric vehicle (FCEV) with Direct Torque Control-Space Vector Modulation scheme (DTC-SVM) based electric drive (induction motor) has been implemented in [24].

This paper proposes an asymmetric three-phase cascading Trinary-DC source multilevel inverter. The suggested topologies are gained by cascading a full bridge inverter with uneven DC source. These topologies have several new patterns adopting the variable switching frequency. Multicarrier pulse width modulation techniques are established and simulated for the preferred three phase asymmetric cascaded multilevel inverter. Finally, the proposed asymmetric three-phase cascading multilevel inverter is demonstrated through experimental results based on the research laboratory (test board) prototype model.

2. Proposed Trinary Multilevel Inverter

The three-phase multilevel inverter is being used for a large number of industrial applications due to their capability of high-power accompanying with lesser output harmonics and switching losses. Multilevel inverter has grown into an active and applied resolution for increasing output power and decreasing total harmonics distortion of AC load system.

The proposed Trinary cascaded multilevel inverter contains three single phase unit, which consists of two full bridges with dissimilar voltage source. The first full bridge contains the DC source of 1 V_{dc} and the second full bridge contains the DC source 3 V_{dc} as presented in **Figure 1**. Each DC source is connected to a proposed three phase inverter. Each inverter produces a three dissimilar output voltage levels, such as positive, zero and negative levels by different groupings of the four power semiconductor switches S1, S2, S3 and S4. Whenever the switches, S1 and S4 is turned ON, then the output voltage is positive level (+Ve) and its shown in **Figure 2**;

whenever the switches S2 and S3 is turned ON, then the output voltage is negative level (−Ve) and it is shown in **Figure 3**; whenever either pair of switches (S1 and S2) or (S3 and S4) is turned ON, then the output voltage will

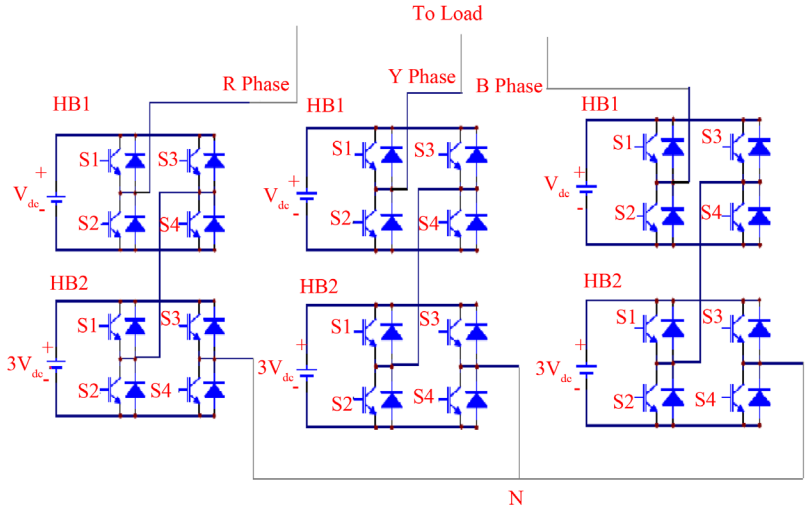

Figure 1. The proposed trinary cascaded multilevel inverter.

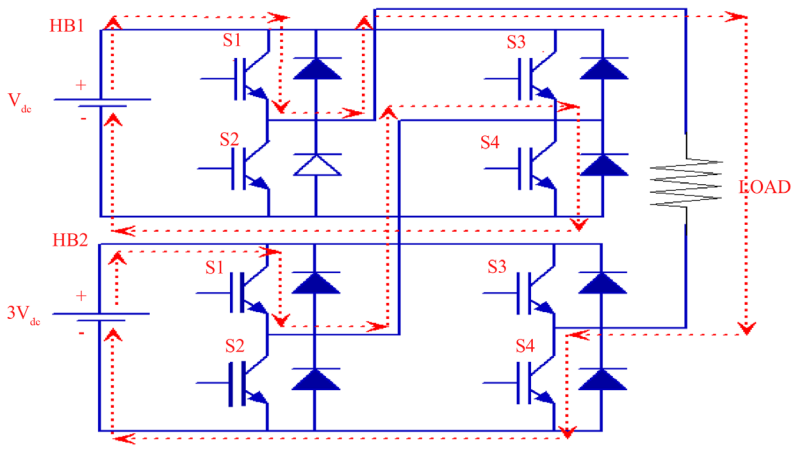

Figure 2. Switching sequences to develop 4 V_{dc} at load.

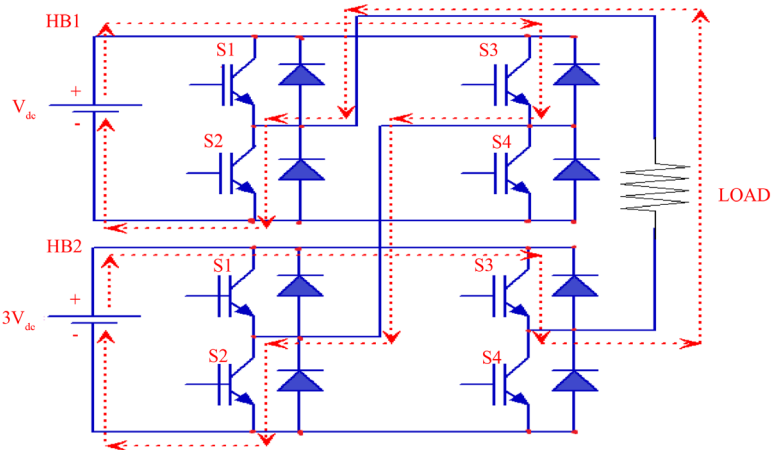

Figure 3. Switching sequences to develop −4 V_{dc} at load.

be at zero level (0) and its shown in **Figure 4**.

Then the output voltage of first bridge can be made equal to the −1 V_{dc}, 0, and 1 V_{dc}, correspondingly the output voltage of second bridge can be made equal to the −3 V_{dc}, 0, and 3 V_{dc} by turning ON and turning OFF its switches appropriately. Consequently, the output voltage of the inverter values for −4 V_{dc}, −3 V_{dc}, −2 V_{dc}, −1 V_{dc}, 0, 4 V_{dc}, 3 V_{dc}, 2 V_{dc}, 1 V_{dc}, can be planned, as represented in **Figure 1** and **Table 1**. The lower inverter (HB2) produces output voltage in three levels, and the upper inverter (HB1) produces stepped waves by adding or subtracting one level from the fundamental output voltage wave. Thus, at the end the output voltage level becomes the summing of each terminal voltage of cascaded H bridges. The output voltage of the load is given in (1)

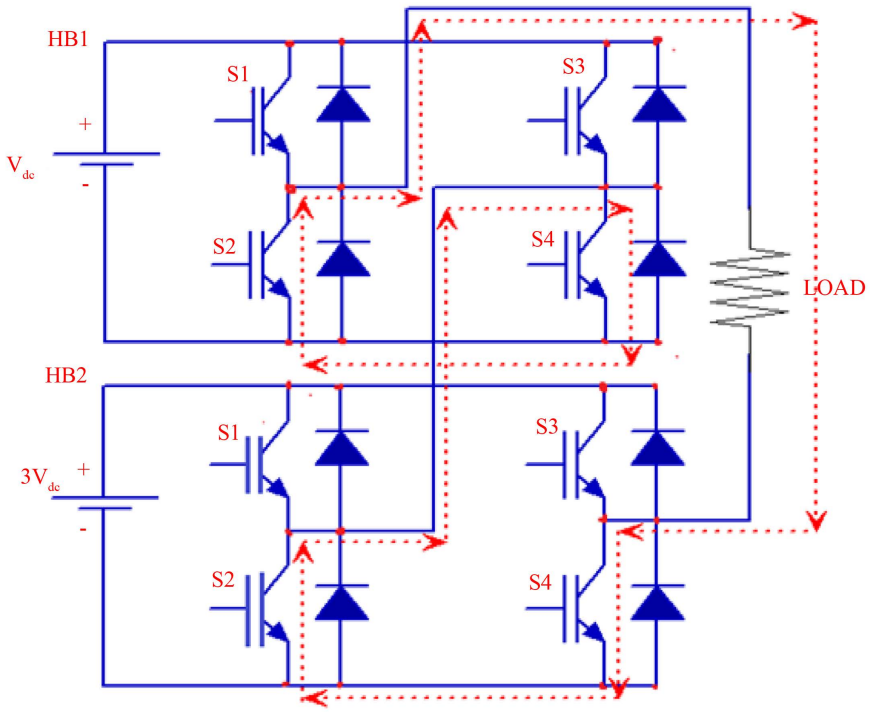

Figure 4. Switching sequences to develop 0 V_{dc} at load.

Table 1. Output voltage level and their switching sequence of proposed MLI.

Output Voltage Level V_{out}	Switching sequence of proposed MLI							
	First Half Bridge (HB1)				Second Half Bridge (HB2)			
	S1	S2	S3	S4	S1	S2	S3	S4
4 V_{dc}	1	0	0	1	1	0	0	1
3 V_{dc}	0	1	0	1	1	0	0	1
2 V_{dc}	0	1	1	0	1	0	0	1
1 V_{dc}	1	0	0	1	0	1	0	1
0	0	1	0	1	0	1	0	0
−1 V_{dc}	0	1	1	0	0	1	0	1
−2 V_{dc}	1	0	0	1	0	1	1	0
−3 V_{dc}	0	1	0	1	0	1	1	0
−4 V_{dc}	0	1	1	0	0	1	1	0

1 = On state, 0 = Off state.

$$V_{out} = V_{HB1} + V_{HB2} \quad (1)$$

3. Variable Frequency Pulse Width Modulation Techniques

It is usually accepted that the presentation of any multilevel inverter, with any switching control tactic can be correlated to the harmonic contents of its inverter output voltage. There a numerous control technique reported in journalism for a cascaded asymmetric multilevel inverter. But the traditionally used modulation control method is the multicarrier Pulse width modulation technique (MCPWM). In this research paper, changeable switching frequency pulse width modulation technologies such as

1) Variable frequency in phase disposition pulse width modulation system (VFIPDPWM).
2) Variable frequency phase opposition disposition pulse width modulation system (VFPODPWM).
3) Variable frequency alternate phase opposition disposition pulse width modulating system (VFAPODPWM).

Which is projected which uses the predictable sinusoidal reference signal and the triangular carrier signals with variable frequency. To put into action of an m-level inverter with (m − 1) triangular carrier are used. There are eight separate triangular carriers with variable frequency and with the same magnitudes all carriers; for the eight triangular carrier signals each pair which has a different frequency. The triangular carrier signal C1 and C8 have same frequency and C2 and C7 have another set of same frequency and C3 and C6 have another set of same frequency and C4 and C5 have another set of same frequency. The firing pulses are produced when the amplitude of the reference signal (modulating signal) is superior to that of the triangular carrier signal.

3.1. Variable Frequency in Phase Disposition Pulse Width Modulation System

The vertical offset of carriers for a nine level Trinary DC source multilevel inverter with variable frequency in phase disposition pulse width modulation techniques are illustrated in **Figure 5**. In phase disposition pulse width modulation technique (IPD), all carriers are in phase with each other (there is no Phase Difference in all eight carriers) and it has same amplitude. In this system for an N level inverter, (N − 1) carriers with the unlike frequency (2000 Hz and 1500 Hz) and equal amplitude are prearranged such that the bands they occupy are continuous.

3.2. Variable Frequency Phase Opposition Disposition Pulse Width Modulation System

The carriers for a nine level Trinary-DC source, multilevel inverter with variable frequency phase opposition disposition pulse width modulation technique is illustrated in **Figure 6**. In this topology, all the carriers are divided uniformly into two groups according to the positive (four carriers from 0 to 4)/negative (four carriers from −4 to 0) standard levels. These two groups are opposite and 180 degrees out of phase width those below the zero values. 180 degrees out of phase with each other while maintenance in phase within the group phase opposition disposition pulse width modulation topology. In this system for an N level inverter, (N − 1) carriers with the unlike frequency (2000 Hz and 1500 Hz) and equal amplitude are prearranged such that the bands they occupy are continuous.

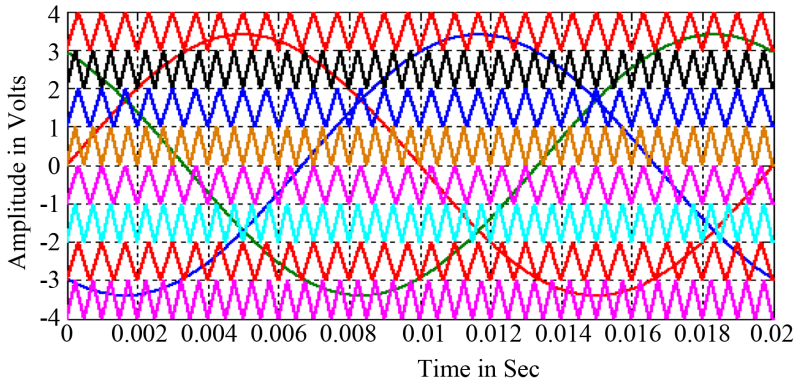

Figure 5. Carrier and reference wave arrangement of a VFIPD PWM control (ma = 0.85 and mf1 = 2000 Hz and mf2 = 1500 Hz).

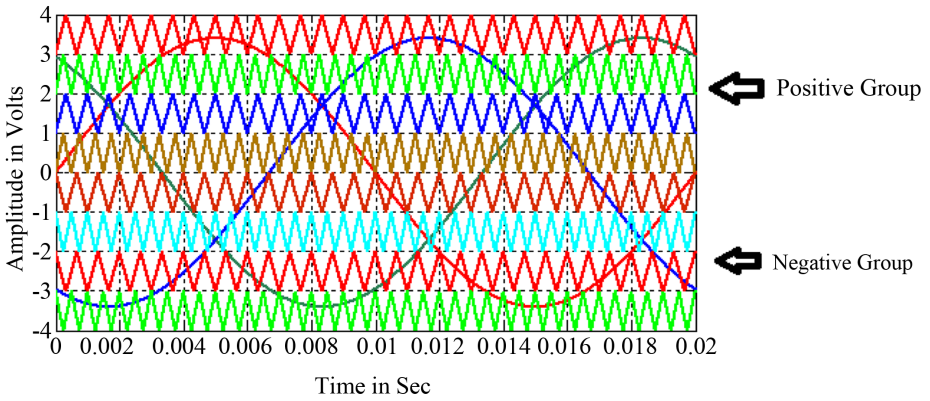

Figure 6. Carrier and reference wave arrangement of a VFPOD PWM control (ma = 0.85 and mf1 = 2000 Hz and mf2 = 1500 Hz).

3.3. Variable Frequency Alternate Phase Opposition Disposition PWM System

The carriers for a nine level Trinary DC source multilevel inverter with variable frequency alternate phase opposition disposition pulse width modulation techniques are illustrated in **Figure 7**. In this topology, the all carriers are 180 degree alternate phase displace from each other. In this system for an N level inverter, (N − 1) carriers with the unlike frequency (2000 Hz and 1500 Hz) and equal amplitude are prearranged such that the bands they occupy are continuous.

4. Simulation Results

A three-phase asymmetric cascading Multilevel Inverter produces nine-level output voltage with a Trinary-input DC Source. These three-phase nine level cascaded multilevel inverters with Trinary-DC Source are modelled in MATLAB/SIMULINK using power systems block set is shown in **Figure 8**.

The proposed Trinary cascaded multilevel inverter contains three single phase unit with uneven voltage Source. These each single phase unit has two full bridges. The first full bridge contains the DC source of 1 V_{dc} and the second full bridge contains the DC source of 3 V_{dc} as presented in **Figure 1**. Each DC source is connected to a proposed three phase inverter. Each inverter produces a three dissimilar output voltage levels, Such as positive, zero and negative levels by different groupings of the four switches S1, S2, S3 and S4. This circuit is developed by using MATLAB/SIMULINK. Whenever the switches, S1 and S4 is turned ON, then the output voltage is positive level (+Ve) and its shown in **Figure 2**; whenever the switches S2 and S3 is turned ON, then the output voltage is negative level (−Ve) and its Shown in **Figure 3**; whenever either pair of switches (S1 and S2) or (S3 and S4) is turned ON, then the output voltage will be at zero level (0) and its shown in **Figure 4**.

The Switching signals of a nine level Trinary multilevel inverter using bipolar pulse width modulation technology are simulated. Simulations are executed for various values of ma (0.8 - 1) and THD is measured using the FFT blocks and their values are exposed in **Table 2**. **Table 3** displays the percentage distortion factor of the inverter output. **Table 4** and **Table 5** display the consequent values of crest factor and form factor. **Table 6** display the fundamental V_{RMS} of inverter output voltage for similar values of modulation indices.

Figures 9-14 show the simulation output voltage and FFT plot of a nine level cascaded multilevel inverter with Trinary DC source, and their appropriate harmonic order of a spectrum with bipolar pulse width modulation technology. But only one sample of the modulation indices is shown.

For modulation indices (ma = 0.85) it is observed from the **Figure 10**, **Figure 12** and **Figure 14**, the harmonic energy level is governing in: **Figure 10** represent the harmonic energy level in VFIPD PWM techniques show 40^{th} order of harmonic. **Figure 12** represents the harmonic energy level in VFPOD PWM techniques shows 38^{th} 40^{th} order of harmonic. **Figure 14** represents the harmonic energy level in VFAPOD PWM techniques shows 29^{th}, 31^{st}, 39^{th} order of harmonic.

Simulations are performed for various values of m_a ranges from 0.8 to 1 and the results are obtained by using following parameter such as V_{dc} = 25 V, 3 V_{dc} = 75 V, load resistance is 100 Ω, carrier frequency f_{c1} is 2000 Hz, carrier frequency fc_2 = 1500 Hz and modulation frequency f_m is 50 Hz. **Table 2** represent the THD contrast of

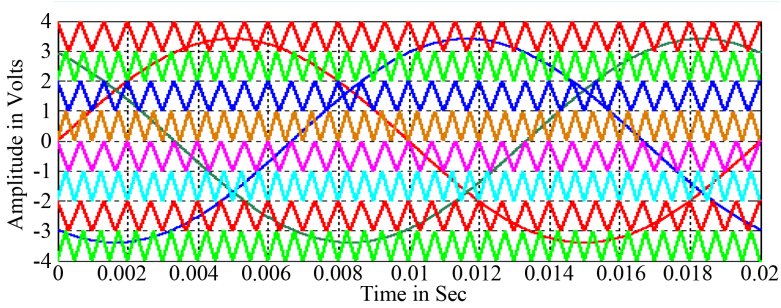

Figure 7. Carrier and reference wave arrangement of a VFAPOD PWM control (ma = 0.85 and mf1 = 2000 Hz and mf2 = 1500 Hz).

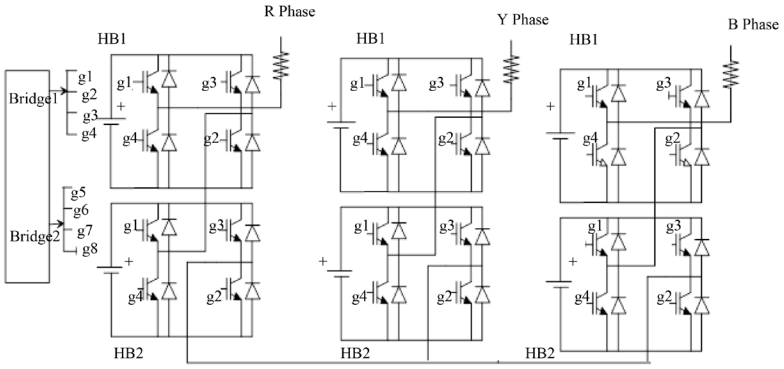

Figure 8. Simulink model of trinary DC source three phase multilevel inverter.

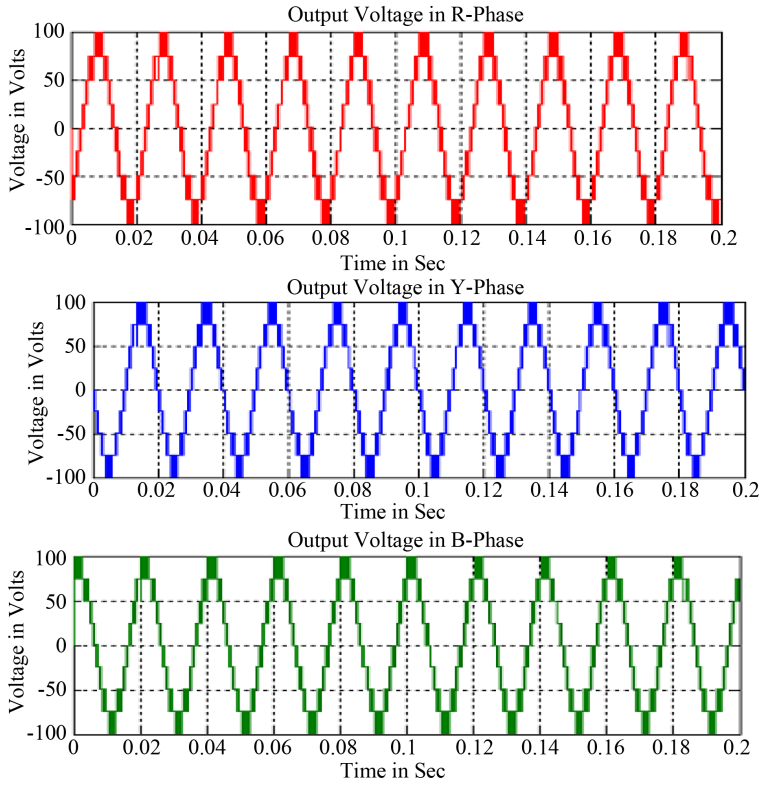

Figure 9. Output voltages generated by variable frequency in phase disposition PWM control with sinusoidal reference.

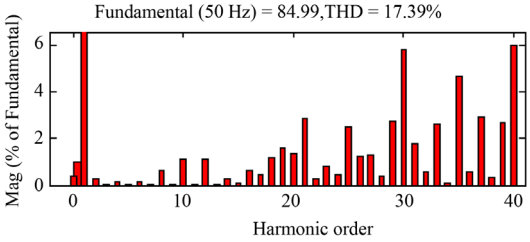

Figure 10. FFT plot for output voltages of variable frequency in phase disposition PWM control with sinusoidal reference.

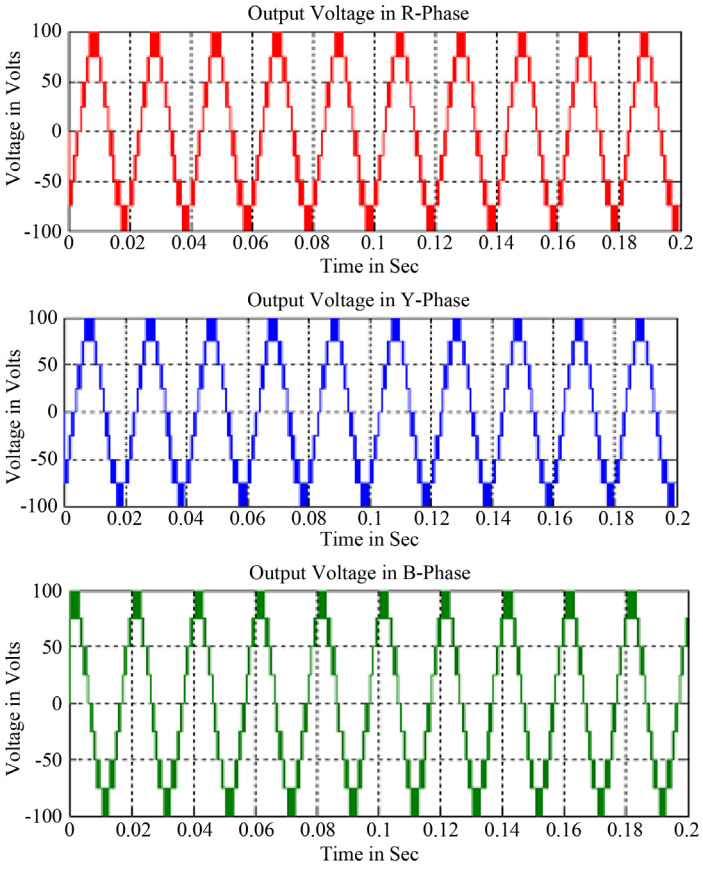

Figure 11. Output voltages generated by variable frequency phase opposition disposition PWM control with sinusoidal reference.

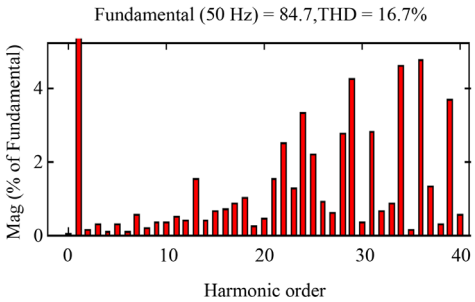

Figure 12. FFT plot for output voltage of variable frequency phase opposition disposition PWM control with sinusoidal reference.

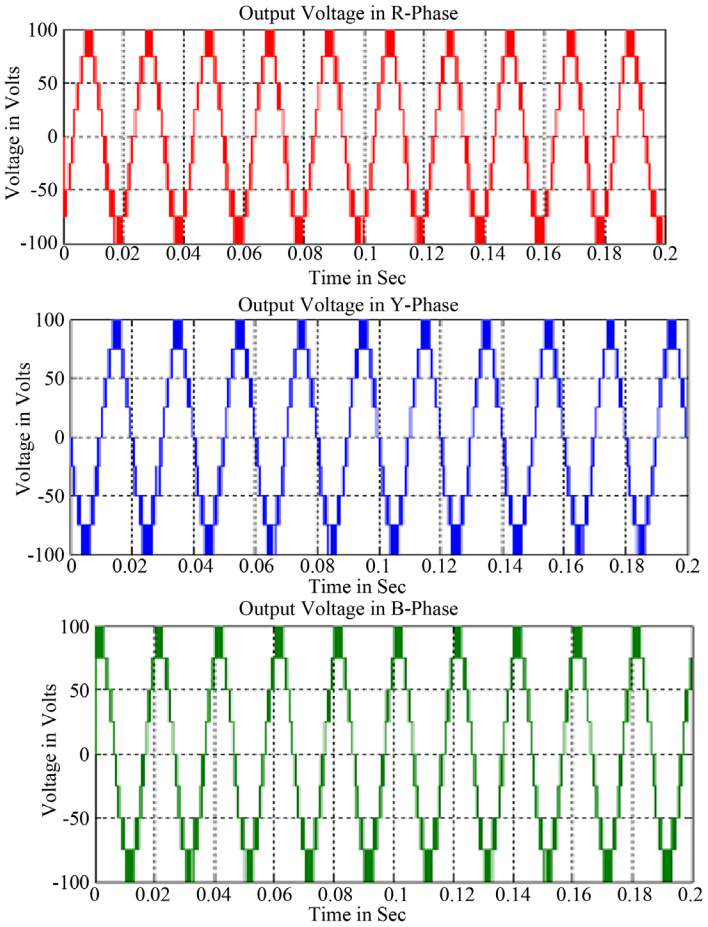

Figure 13. Output voltages generated by variable frequency alternate phase opposition disposition PWM control with sinusoidal reference.

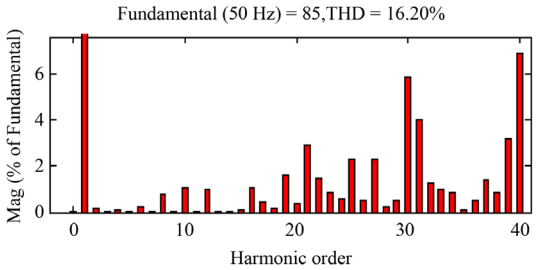

Figure 14. FFT plot for output voltage of variable frequency alternate phase opposition disposition PWM control with sinusoidal reference.

Table 2. % THD for different kind of modulation indices.

Ma	Sine reference		
	VFIPD	VFPOD	VFAPOD
1	12.99	13.01	13.74
0.95	15.22	15.32	15.55
0.9	16.06	16.62	16.35
0.85	17.39	16.70	16.20
0.8	16.10	16.75	16.66

Table 3. Distortion factor for different kind of modulation indices.

Ma	VFIPD	VFPOD	VFAPOD
1	0.000492	0.000881	0.000736
0.95	0.000459	0.00039	0.000257
0.9	0.000721	0.000536	0.000515
0.85	0.000596	0.000345	0.000515
0.8	0.000596	0.000345	0.00079

Table 4. Crest factor for different kind of modulation indices.

Ma	VFIPD	VFPOD	VFAPOD
1	1.414227	1.413457	1.413827
0.95	1.41426	1.414141	1.414322
0.9	1.414232	1.414362	1.414205
0.85	1.414378	1.414259	1.414309
0.8	1.414177	1.422261	1.777827

Table 5. Form factor for different kind of modulation indices.

Ma	VFIPD	VFPOD	VFAPOD
1	587.7805	1.14E+09	1.13E+09
0.95	1216.588	1735.052	3028.404
0.9	719.0783	960.7488	11508.14
0.85	193.7762	1525.471	1795.638
0.8	683.2126	2561.086	318.9402

Table 6. Fundamental RMS voltage for different kind of modulation indices.

Ma	VFIPD	VFPOD	VFAPOD
1	70.71	70.83	70.73
0.95	67.18	67.32	67.17
0.9	63.60	63.64	63.62
0.85	60.69	60.71	60.16
0.8	56.57	56.66	56.58

VFIPD, VFPOD and VFAPOD pulse width modulation techniques no more than one pulse modulation techniques such as VFIPD (Variable Frequency in Phase Disposition) it hold minimum quantity of harmonic distortion. **Table 6** and **Figure 16** represent the V_{RMS} contrast of VFIPD, VFPOD and VFAPOD pulse width modulation techniques no more than one pulse modulation techniques such as VFPOD (Variable Frequency Phase Opposition Disposition) it hold maximum quantity of fundamental RMS output voltage.

Figure 15 shows THD level of VFIPD, VFPOD and VFAPOD pulse width modulation techniques and it shows no more than one pulse modulation techniques such as VFIPD (variable frequency in phase disposition) it hold minimum quantity of harmonic distortion. **Figure 16** shows the V_{RMS} value of VFIPD, VFPOD and VFAPOD pulse width modulation techniques and it shows no more than one pulse modulation techniques such as VFPOD (Variable Frequency Phase Opposition Disposition) it hold maximum quantity of fundamental RMS output voltage.

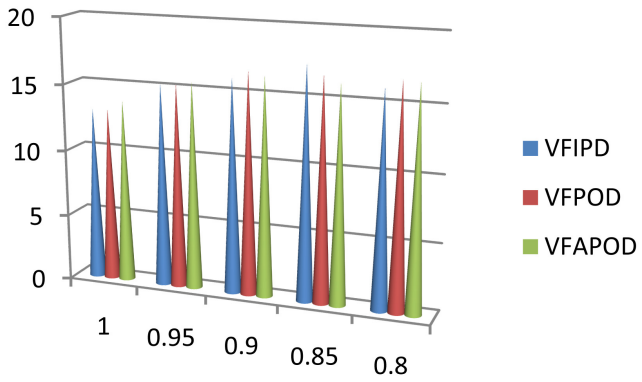

Figure 15. Variable frequency techniques % THD vs modulation indices.

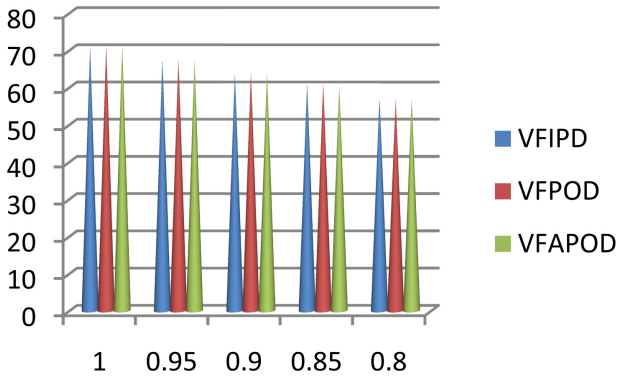

Figure 16. Variable frequency techniques fundamental V_{RMS} vs modulation indices.

5. Hardware Test Board and Results

Experimental prototype model (test board) of a proposed three phase asymmetric cascading Multilevel Inverter topologies with a Trinary-DC source is implemented by using PIC Microcontroller. The PIC Microcontroller is a choice of hardware implementation due to its ability to generate accurate results at a higher computational speed. A nine-level three phase inverter experiments have been fabricated to implement the suggested variable frequency PWM techniques. Gate signal is created by comparing sinusoidal pulse width modulation topologies with triangular carrier arrangement. Experimentally the research authenticates the proposed a three phase asymmetric cascading Multilevel Inverter topologies with a Trinary-DC source produce a nine level output voltage its shown in **Figure 18** and **Figure 19**. A prototype model of (only one phase from three phases) nine level Trinary-DC source cascaded multilevel inverter and it is developed by using IGBTs as a switching devices is shown in **Figure 17**.

6. Conclusion

Asymmetric three-phase cascading Trinary-DC source multilevel inverter with variable frequency pulse width modulation techniques has been developed. The topology has been established that the VFIPD PWM strategy of sinusoidal reference with triangular carrier offers lesser value of total harmonic distortion compared with other PWM technique. VFPOD strategy of sinusoidal reference with triangular carrier offers higher value of fundamental RMS (V_{RMS}) output voltage compared with other PWM technique. Finally, the simulation and research laboratory tests (prototype model) are achieved to show the strength of the proposed asymmetrical three-phase cascading Trinary-DC source multilevel inverter. In future the three-phase asymmetric cascading multilevel inverter test is implemented with the help of three-phase Permanent Magnet Synchronous motor drive using

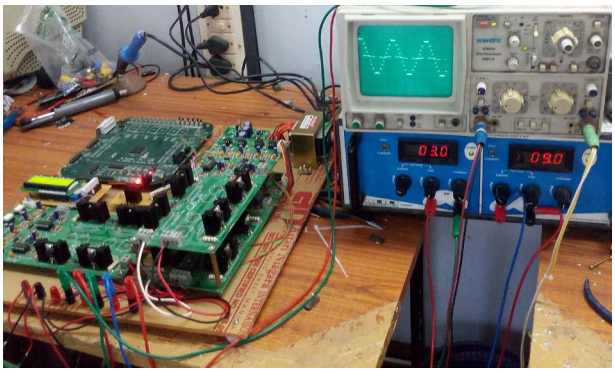

Figure 17. Prototype model of nine level single phase cascaded trinary multilevel inverter by using multicarrier PWM techniques.

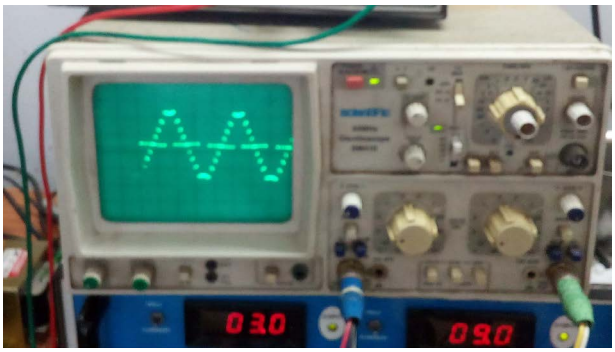

Figure 18. Output voltage waveforms of nine-level single phase cascaded trinary multilevel inverter by using multicarrier PWM techniques.

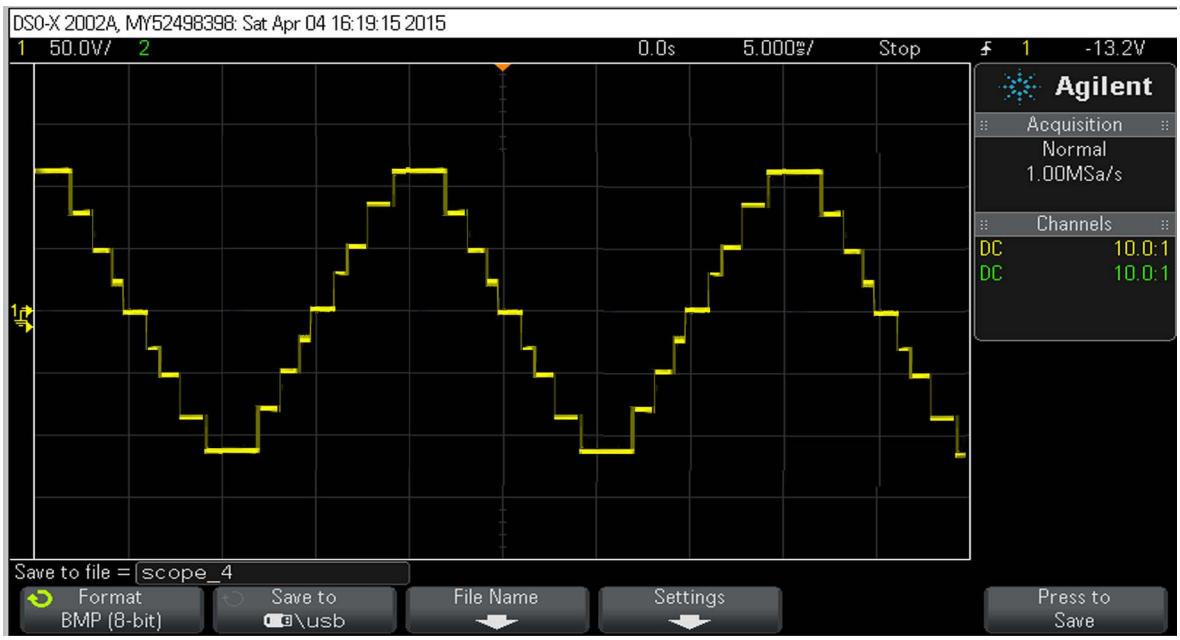

Figure 19. Nine-level output voltage of phase A.

predictable speed and torque control.

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