Circuits and Systems, 2016, 7, 464-474
Published Online April 2016 in SciRes. http://www.scirp.org/journal/cs
http://dx.doi.org/10.4236/cs.2016.74039

FPGA-Based High-Frequency Digital Pulse Width Modulator Architecture for DC-DC Converters

V. Radhika[1], K. Baskaran[2]

[1]Electronics and Instrumentation Engineering, Sri Ramakrishna Engineering College, Coimbatore, India
[2]Electrical and Electronics Engineering, Government College of Technology, Coimbatore, India
Email: radhika.senthil@srec.ac.in, drbaskaran@gct.ac.in

Received 3 March 2016; accepted 26 April 2016; published 29 April 2016

Abstract

Digital pulse width modulator is an integral part in digitally controlled Direct Current to Direct Current (DC-DC) converter utilized in modern portable devices. This paper presents a new Digital Pulse Width Modulator (DPWM) architecture for DC-DC converter using mealy finite state machine with gray code encoding scheme and one hot encoding method to derive the variable duty cycle Pulse Width Modulation (PWM) signal without varying the clock frequency. To verify the proposed DPWM technique, the architecture with control input of six, five and four bits are implemented and the maximum operating frequency along with power consumption results is obtained for different Field Programmable Gate Array (FPGA) devices. The post layout timing results are presented showing that architecture can work with maximum frequency of 326 MHz and derive PWM signal of 3.59 MHz. Experimental results show the implementation of the proposed architecture in low-cost FPGA (Spartan 3A) with on-board oscillator clock frequency of 12 MHz which is multiplied internally by two with Digital Clock Manager (DCM) and derive the PWM signal of 1.5 MHz with a time resolution of 1 ps.

Keywords

Gray Code Encoding Scheme, High Frequency DPWM, Mealy Finite State Machine, One Hot Encoding Scheme

1. Introduction

In recent years, portable devices take a superior place in the modern electronic world. These devices are smaller

How to cite this paper: Radhika, V. and Baskaran, K. (2016) FPGA-Based High-Frequency Digital Pulse Width Modulator Architecture for DC-DC Converters. *Circuits and Systems*, **7**, 464-474. http://dx.doi.org/10.4236/cs.2016.74039

in size, need low power and a higher efficiency power converter for its longer battery life. As there are frequent changes in load current and supply voltage, higher-efficiency switching mode power supplies are commonly used in these type devices [1] [2]. Pulse Width Modulation technique (PWM) becomes crucial in power converters to control the amount of voltage delivered [3] [4]. A digitally controlled power converter becomes superior to an analog due to its inherent advantages like reprogrammable nature and insensitive to process and temperature variations [4]. Digital Pulse Width Modulators (DPWM) are implemented in FPGA and can be used as digital switching controller for the power converters [5]. PWM signals generated by DPWM can be used to control the switch of a power converter and modulate the output voltage of DC-DC converters.

Several architectures were developed for DPWM operating in the frequency range from KHz to MHz. These include the Counter Comparator based DPWM, Delay line based DPWM, Hybrid Delay line based DPWM architectures [6] and many soft computing techniques [7] [8], each of it having its own advantage and disadvantage. All these architectures have come with an improvement in area, linearity, speed, minimized delay and minimized power consumption. The latest DPWM architectures have used the resources available in FPGA to provide a better performance. A new DPWM architecture is proposed that combines synchronous block and asynchronous block using the Delay Locked Loop (DLL) capability with FPGA [9]. The clock multiplying and phase shifting capability of DLL is used here to derive the PWM pulse under 2 ns resolution. Another architecture that uses the DCM block available in FPGA derives the variable duty cycle PWM pulse. DCM block is utilized to shift the phase of clocks in small increments. The resolution obtained by this method is greater than the traditional methods with a drawback of delay in phase shift update time [10]. Hybrid DPWM architecture utilizing the DCM block along with comparator and counter is proposed [5] [11]. Initially a duty cycle control value of n bits is loaded to a register and at the same time it has set the PWM signal. Register value is compared with the code of incremented counter and if two values are equal, it resets the PWM signal with SR flip flop. This architecture provides a lower FPGA clock period and avoids time resolution limitation. Windowed segmented DCM and segmented based DPWM architecture [12] [13] utilizes two cascaded DCM blocks. This eventually has higher power efficiency when compared to all the other DPWM architectures and also provides a better resolution by efficiently utilizing the phase shifting capability of DCM.

This work aims at utilizing the utmost resources available in FPGA to derive a new DPWM architecture with a higher operating frequency and lower power consumption. Variable duty cycle PWM pulse ensuing from the DPWM architecture can be used to control the switch which modulates the voltage delivered by the power converters. The architecture was developed with Verilog hardware language and its behavioral simulation results are obtained for functional verification. The netlist is generated, placed and routed and timing analysis is performed. The post layout simulation results are obtained and the resultant binary file is transferred to a low-cost SPATRAN 3A FPGA and now the FPGA can be used to generate a variable duty cycle PWM pulse based on the control inputs. Different combinations of control inputs are given for varying the duty cycle of PWM pulse and results are viewed with a digital storage oscilloscope. The proposed DPWM architecture is explained in Section 2 and its results and discussion are shown in Section 3. The experimental results are shown in Section 4 and conclusion is given in Section 5.

2. Architecture of Proposed DPWM for DC-DC Converters

Figure 1 shows the block diagram of proposed DPWM architecture. As FPGA's are rich in flip-flops [14] this proposed architecture best utilizes the flip-flops with limited usage of logic gates. It combines the combinational block and synchronous sequential block to deliver a variable duty PWM pulse without varying the clock frequency. DCM block provides the clock frequency twice of the external frequency to the architecture. Almost all the DPWM architectures available in the literature are implemented with a binary counter and comparator but this work uses Mealy State machine with gray code encoding scheme combined with one hot encoding scheme so that it can operate faster than traditional architectures. In this approach for an N bit control input a state machine is designed with D flip-flop. The state machine output is fed to the K bit ($K = 2^N$) one hot encoder and one hot encoder output is given to the pulse width control circuit. Pulse width control circuit is implemented with the Look Up Tables (LUT's) and multiplexers. Pulse width control circuit selects the one hot encoder states based on control input signal and adjusts the duty cycle of the PWM pulse through the SR flip flop.

Frequency of signal derived PWM signal is given by

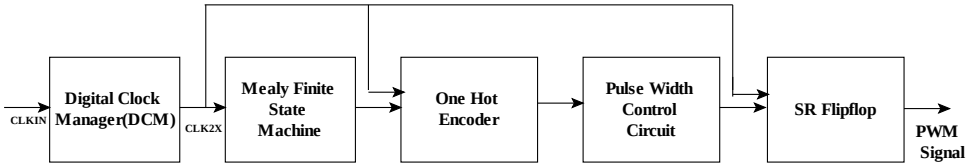

Figure 1. Block diagram of proposed high frequency DPWM architecture.

$$\text{PWM frequency } f_{PWM} = \frac{fclk}{2^N} \tag{1}$$

$$\text{Duty cycle Percentage } \% = \frac{\text{Data input}}{2^N} \tag{2}$$

2.1. Digital Clock Manager (DCM)

Digital clock manager provides elaborate clocking capability to SPARTAN 3A FPGA based applications. DCMs multiply or divide the incoming clock frequency to synthesize a new clock frequency. DLL block in DCM eliminates the delay from the external clock input port and minimizes the clock skew [13]. DLL gets the input from the CLKIN and CLKFB pins and generates phase shifted (CLK 90, CLK180, CLK270), clock frequency multiplied (CLK2X) and clock frequency divided (CLKDV) values [15].

In this design clock doubler (CLK2X) is used and the onboard clock frequency of 12 MHz is multiplied to yield a new clock frequency of 24 MHz.

2.2. Synchronous Block

The Synchronous block in the architecture is a Mealy State Machine with gray code encoding scheme and a one hot encoder with CLK2X pulse derived from DCM block as a clock input.

2.2.1. Mealy State Machine

Most of the DPWM architectures available in the literature use synchronous binary counter and comparator to generate PWM signals of variable duty cycle. Binary counter is simple but multiple bits change at a time between each state which causes multiple flip-flops to change its state at a time result in hazard and also consumes more power and comparator used to compare the predefined value with counter output for generating variable duty cycle PWM pulse. This new proposed DPWM architecture utilizes the Mealy state machine with gray code encoding scheme. The gray code encoding scheme has only one bit change between successive states so that it can minimize the switching activity and power consumption. Further in Mealy machine a combinational logic block is present to provide the output based on both present state and present input. So mealy machine has less number of states and responds immediately to change of state and so it faster than counters used in traditional architectures [14]. Flip-flops used in state machine are clocked with the same clock frequency (CLK2X). The proposed work has an external input (X1) given to state machine and depending on the present state and external input (X1) the state machine proceeds to the next state. When the desired state is reached it enables the states of the 2^N bit one hot encoder flip-flops (D_K to D_0) one by one

2.2.2. One Hot Encoder

In one hot encoding scheme, a series of flip-flops are connected together were, the Q output of first flip-flop is connected to the D input of second flip-flop is shown in **Figure 2**. Further, Q output of last flip-flop connected in the series is connected to the D input of first flip-flop. For every new clock edge each flip-flop transfers its state to the next flip-flop and this proceeds to the last flip-flop connected in the series. One hot encoder uses one flip-flop for each state and in this proposed method for N bit control input value, K bit one hot encoder is designed with K ($K = 2^N$) flip-flops and all are clocked with same clock frequency (CLK2X). As one hot encoder utilizes the higher number of flip-flops, it is better suited for implementation in flip-flop rich architectures like FPGAs offered by Xilinx [14]. In this scheme only one state variable (D_0 to D_k) is high at a time, all the other state bits are zero which means that only one flip-flop will be active at a time and this minimizes the number of

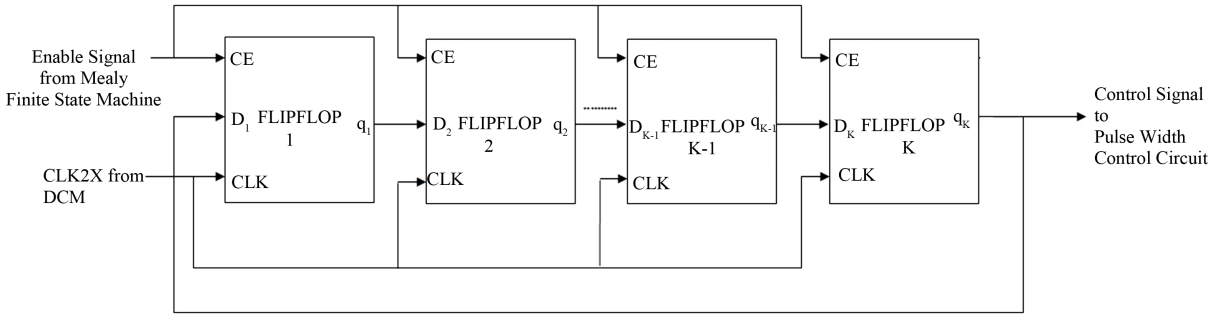

Figure 2. K state one hot encoder with K flip-flops.

transitions. This reduces the power consumption and makes it less prone to glitches. In one hot state machine the speed is independent of number states instead only on number of transitions. As DPWM is a key component for the digital control of high frequency converters one hot encoder and mealy state machine combination provides a solution for higher switching frequency in the range of MHz. Architectural timings can be improved by adding pipeline register layers in critical path between one hot encoder flip-flops and pulse width control circuit. The serial string of K flip-flops can be evaluated in parallel by connecting them to LUT's of pulse width control circuit with these pipeline registers. If the clock period is given by t_c then the delay in the critical path for K^{th} state of one hot encoder would be Kt_c which can reduced to Kt_c/K with these pipeline registers. Each time when the state machine reaches its final state it makes the state variables (D_0 to D_k) of one hot encoder as high one by one. Finally when D_k bit of one hot encoder reaches a high state it issues the set signal to SR flip flop which further makes the PWM signal to set condition and in the next cycle one more time remaining state variables of one hot encoder (D_0 to D_{k-1}) is made high. Based on the value of control input (I_0 to I_{N-1}) the state variables (D_0 to D_{k-1}) is connected to reset input SR flip flop through pulse width control circuit. One hot Encoder states with 4 bit control input signal value and its corresponding duty cycle percentage is shown in the **Table 1**.

2.3. Pulse Width Control Circuit

The pulse width circuit is realized with LUT's and multiplexer's shown in **Figure 3**. As FPGA are made of configuration logic blocks (CLB's) and each of the CLB hold LUT's and multiplexer's, the LUT's can be easily wired to the multiplexer and it minimizes the internal delay in routing paths. To avoid larger multiplexer structure for connecting the one hot encoder output to SR flip-flop, four input LUT's present in each slice of FPGA can be used to combine the output of one hot encoder flip-flops and finally connect them to multiplexer. Larger multiplexer structures need larger number of wires and this slows down the performance of the device. The LUT's has a combination of AND logic and OR logic function realized with it. The LUT's with the control input signal as one of the inputs connects the one hot encoder states to the SR flip-flop.

Initially when the D_k state of one hot encoder is high it issues a set signal to the SR flip flop which in turn issues a set signal to the PWM pulse. Based on the control input value N (I_0 to I_{N-1}) one particular state variable of one hot encoder (D_0 to D_{k-1}) is connected to the reset input of SR flip flop which resets the PWM signal.

3. Results and Discussion

The proposed DPWM architecture for different control input values is designed with Verilog Hardware language and experimental results are obtained with Spartan 3A FPGA. For the functional verification behavioral simulation results are viewed with Xilinx ISE 14.2 simulator tool. Synthesized and implemented with PlanAhead 14.2 tool. Timing constraints is given to the signals in various paths and the performance of the design with each of these delay values is obtained.

Simulation Results

Timing Simulation results are obtained for different control input bits ranging from four bit (0000 to $1111)_2$, five bit (00000 to $11111)_2$ and six bit (000000 to $111111)_2$ to derive the PWM signals of different duty cycle percentage. For instance, with a four bit control input (adc) of $(1000)_2$ and the clock input (clk) of time period 80 ns is

Table 1. States of one hot encoder for 4 bit input control signal and duty cycle percentage.

Control input signal value	One hot encoder state (D_{15}-D_0)	Duty cycle %
0000	0000000000000001	0
0001	0000000000000010	6.2
0010	0000000000000100	12.5
0011	0000000000001000	18.7
0100	0000000000010000	25
0101	0000000000100000	31.2
0110	0000000001000000	37.5
0111	0000000010000000	43.7
1000	0000000100000000	50
1001	0000001000000000	56.2
1010	0000010000000000	62.5
1011	0000100000000000	68.7
1100	0001000000000000	75
1101	0010000000000000	81.2
1110	0100000000000000	87.5
1111	1000000000000000	93.7

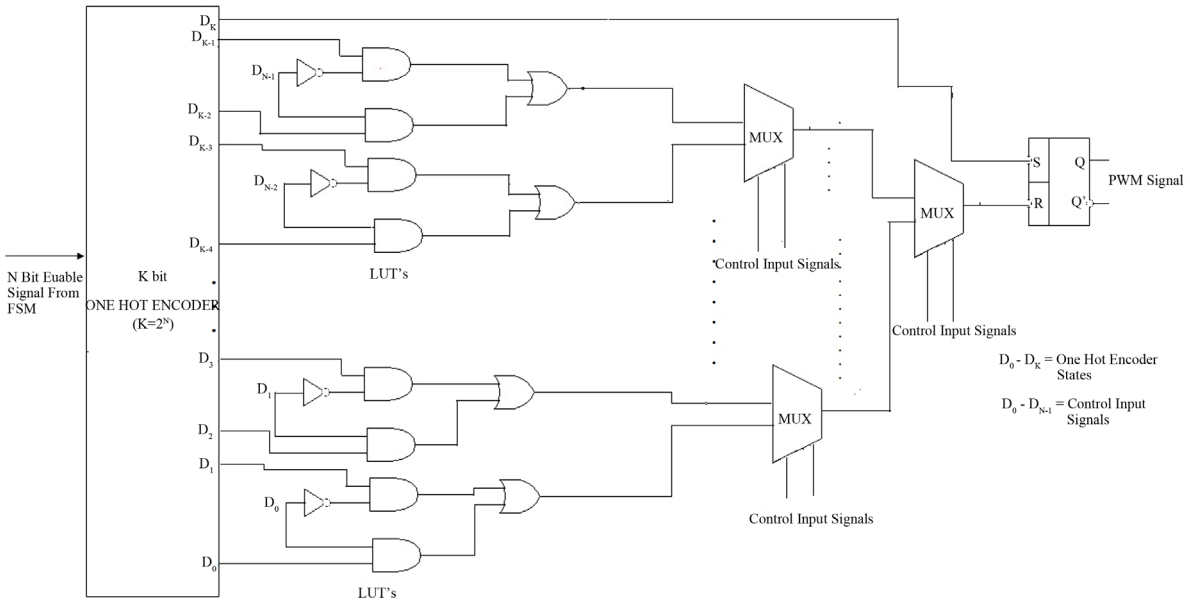

Figure 3. Pulse width control circuit with SR flip-flop.

given, initially at the first clock pulse D_0 flip-flop will be set to the state of one and this continues to the D_{15} flip-flop of one hot encoder. D_{15} flip-flop will be connected to SET input of SR flip-flop. As control input (adc) is given as $(1000)_2$, in the next cycle once again the states of one hot encoder flip-flops (D_0-D_8) is set to condition of one and when D_8 flip-flop of one hot encoder set to the condition of one, it get connected to the RESET input of SR flip-flop. This set and reset condition of flip-flop derives the PWM signal of 50% duty cycle and again for next control input of $(1100)_2$, D_{15} bit of one hot encoder is connected to the set input of SR flip-flop and D_{12} bit of one hot encoder is connected to the reset input of SR flip-flop which derives PWM signal of 81.2%

duty cycle.

The duty cycle percentage for 6 bit input data of $(100100)_2$ is 57.2% while for the 5 bit input data $(10010)_2$ it is 62.5% and for 4 bit input data of $(1000)_2$ it is 53.2% as shown in **Figures 4-6**.

Timing analysis is done with Xilinx Physical Design file (.ncd) and Xilinx Physical Constraint file (.pcf) of the architecture for various FPGA devices manufactured by Xilinx. Maximum operating clock frequency for the

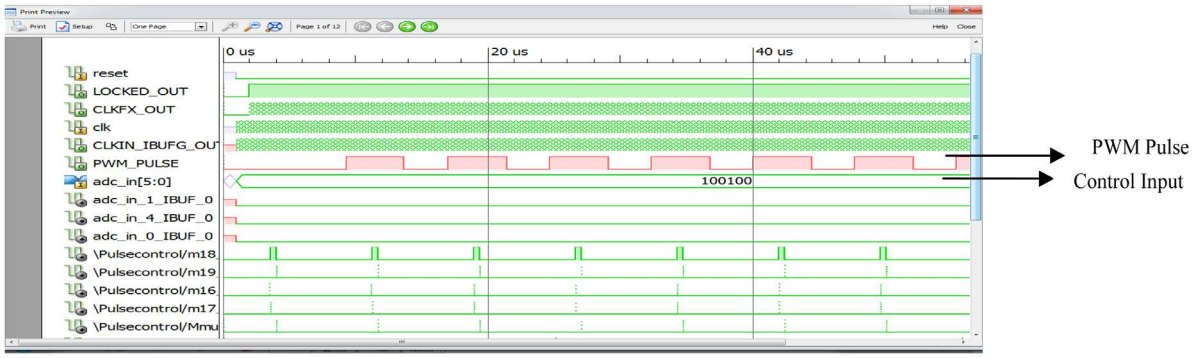

Figure 4. Post layout timing simulation result for 56.2% duty cycle with 6 bit control input $(100100)_2$.

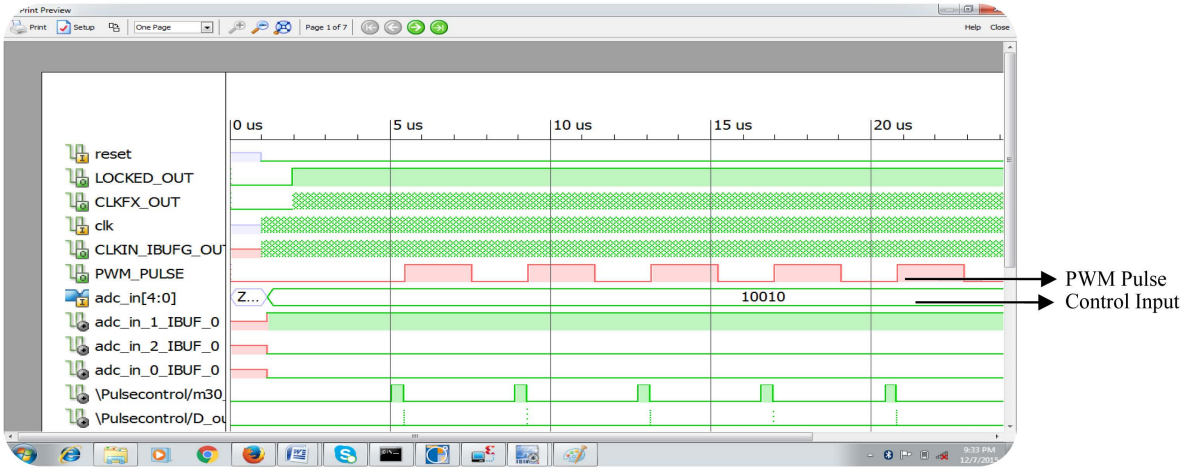

Figure 5. Post layout timing simulation result for 62.5% duty cycle with 5 bit control input $(10100)_2$.

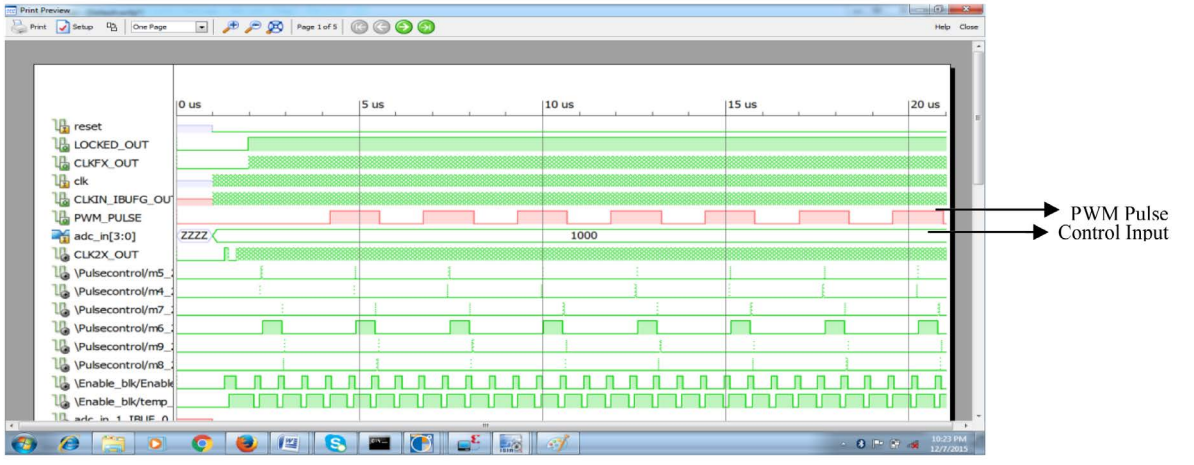

Figure 6. Post layout timing simulation result for 50% duty cycle with 4 bit control input $(1000)_2$.

proposed system is obtained for control input data of four, five, six bits and the resulting PWM signal frequency shown in **Table 2**. Timing results shows that the proposed architecture works with maximum clock frequency of 326 MHz. Power consumption of the proposed architecture is obtained with XPower Analyzer by using Xilinx Physical Design File (.ncd) of the architecture for different control input bits is shown in **Table 3**. Logic resources utilized is given in **Tables 4-6** shows that the architecture occupies only 3% to 9% of logic resources and the remaining resources can be utilized for the other control operations.

Table 2. Post layout timing results for various XILINX FPGA devices.

Device type	6 bit control input		5 bit control input		4 bit control input	
	Max. Clock Frequency (MHz)	PWM Frequency (MHz)	Max. Clock Frequency (MHz)	PWM Frequency (MHz)	Max. Clock Frequency (MHz)	PWM Frequency (MHz)
xc3s100etq144-5	229.83	3.59	314.46	9.82	326.05	20.37
xc3s100etq144-4	193.08	3.01	240.55	7.51	311.13	19.44
xa3s250evqg100-4	187.16	2.92	253.55	7.92	309.11	19.31
xc3s50avq100-5	281.61	4.40	330.14	10.31	342.14	21.30
xc3s50avq100-4	212.26	3.31	302.84	9.46	330.14	20.63
xc3s100evq100-5	210.88	3.29	289.51	9.04	326.05	20.37
xc3s100evq100-4	193.61	3.02	235.01	7.34	270.41	16.90

Table 3. Power analysis results for various XILINX FPGA devices.

Device type	4 bit control input	5 bit control input	6 bit control input
	Power consumption (mW)		
xc3s100etq144-5	40.78	41.84	44.60
xc3s100etq144-4	40.76	41.59	44.56
xa3s250evqg100-4	40.60	41.72	44.48
xc3s50avq100-5	39.60	39.27	40.34
xc3s50avq100-4	39.70	39.22	40.33
xc3s100evq100-5	40.58	41.67	45.14
xc3s100evq100-4	40.60	41.84	44.84

Table 4. Device utilization summary for different FPGA devices for 6 bit control input.

FPGA device	Slice flip flop	4 input LUT	BUFGMUX
xc3s100etq144-5	139 out of 1920	33 out of 1920	3 out of 24
xa3s250evqg100-4	139 out of 4896	33 out of 4896	3 out of 24
xc3s50avq100-5	139 out of 1408	33 out of 1408	3 out of 24
xc3s100evq100-5	139 out of 1920	33 out of 1920	3 out of 24

Table 5. Device utilization summary for different FPGA devices for 5 bit control input.

FPGA device	Slice flip flop	4 input LUT	BUFGMUX
xc3s100etq144-5	75 out of 1920	16 out of 1920	3 out of 24
xa3s250evqg100-4	75 out of 4896	16 out of 4896	3 out of 24
xc3s50avq100-5	75 out of 1408	17 out of 1408	3 out of 24
xc3s100evq100-5	75 out of 1920	16 out of 1920	3 out of 24

When comparing the architectures for three different control inputs architecture with less control bits has higher operating, PWM frequency and also consumes less logic resources with lower power consumption. But the architecture with high number of control input bits can derive PWM signals with higher resolution. Furthermore resulting PWM frequency depends on target FPGA device and speed of the FPGA device.

4. Experimental Results

After performing functional and timing verification, bit stream file is generated and transferred to the target XILINX SPARTAN XC3S50A FPGA kit with JTAG cable to test the functionality. The value of data input is given externally by the switches present in the FPGA Board and the architecture uses the clock of 12 MHz derived from on board oscillator circuit available in FPGA. The clock frequency is multiplied by two (CLK2X) with DCM available in FPGA to derive a new clock frequency of 24 MHz. The proposed system was tested for all the input combinations and measured duty cycle equals the theoretical value for the particular input combination. For an instance input data of four bit$(1000)_2$ is given through the switches, duty cycle percentage obtained is 50% shown in **Figure 10**. Frequency of PWM signal obtained experimentally can be increased with a higher input clock frequency obtained through external high frequency clock generator and by using high frequency on board oscillator circuit. The digital oscilloscope showing the output waveforms for various duty cycles is shown in the **Figures 7-11**.

Table 6. Device utilization summary for different FPGA devices with 4 bit control input.

FPGA device	Slice flip flop	4 input LUT	BUFGMUX
xc3s100etq144-5	44 out of 1920	4 out of 1920	3 out of 24
xa3s250evqg100-4	44 out of 4896	4 out of 4896	3 out of 24
xc3s50avq100-5	44 out of 1408	4 out of 1408	3 out of 24
xc3s100evq100-5	44 out of 1920	4 out of 1920	3 out of 24

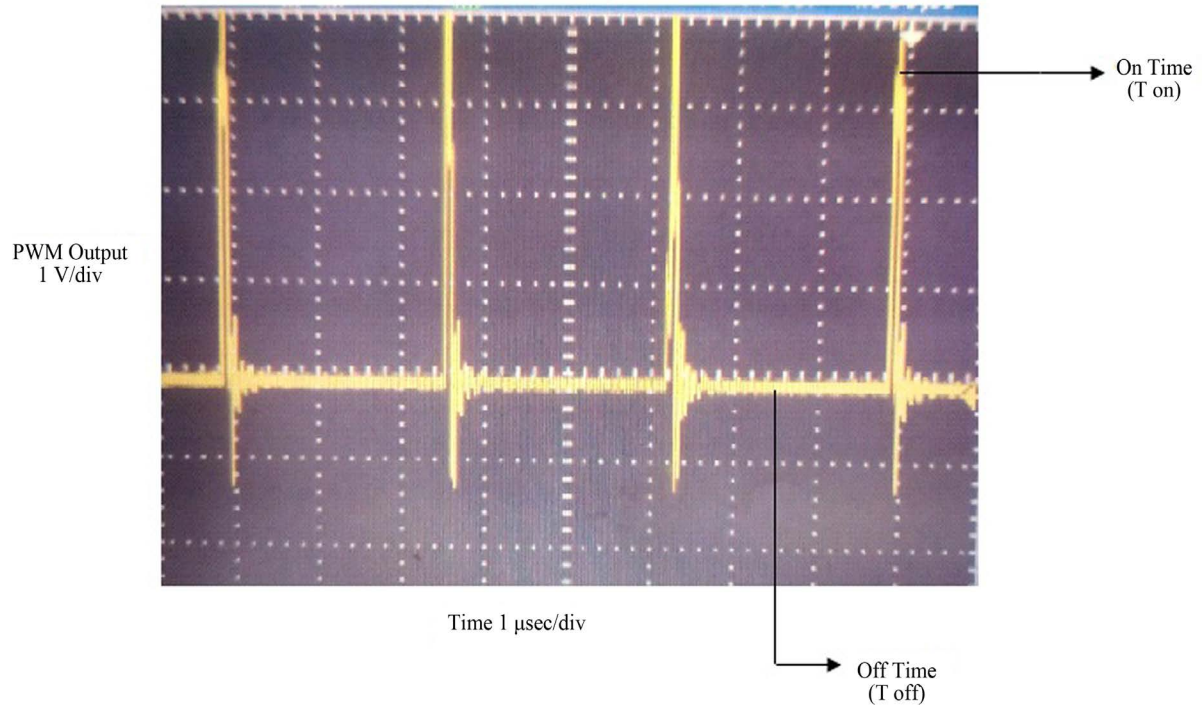

Figure 7. Digital storage oscilloscope waveform for duty cycle = 6.4%.

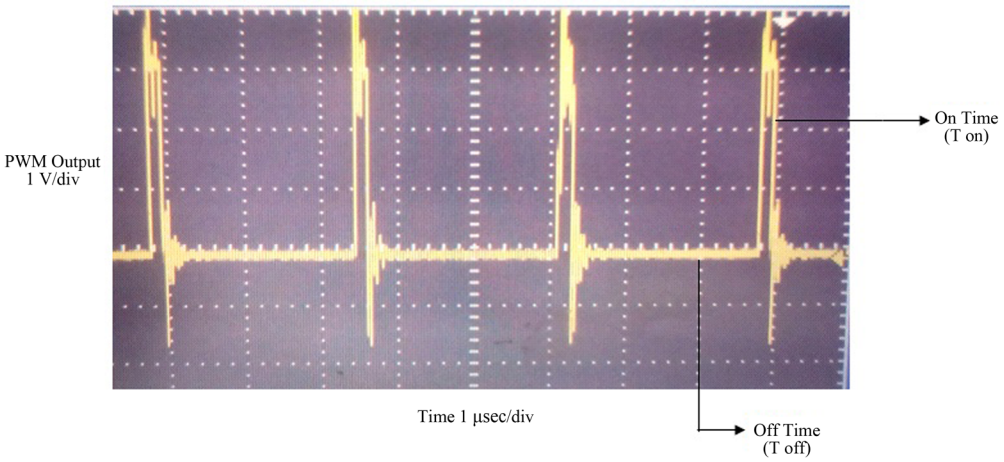

Figure 8. Digital storage oscilloscope waveform for duty cycle = 13.3%.

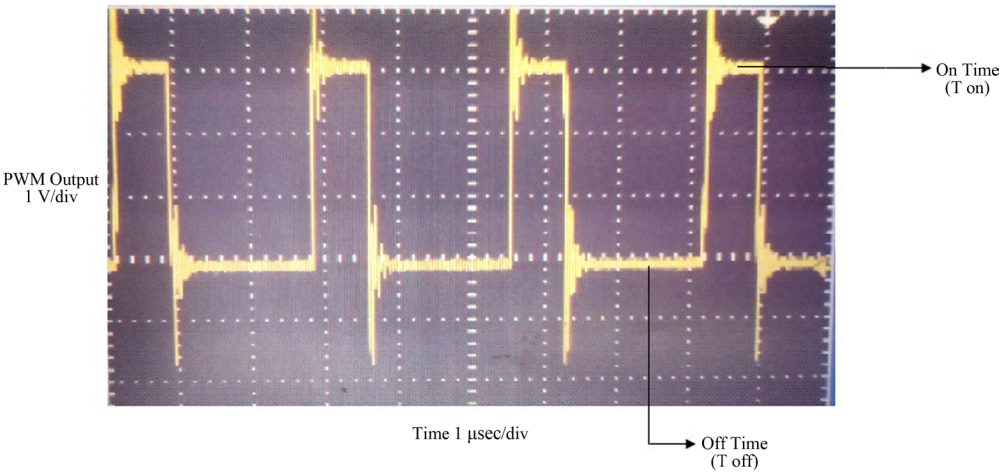

Figure 9. Digital storage oscilloscope waveform for duty cycle = 28.7%.

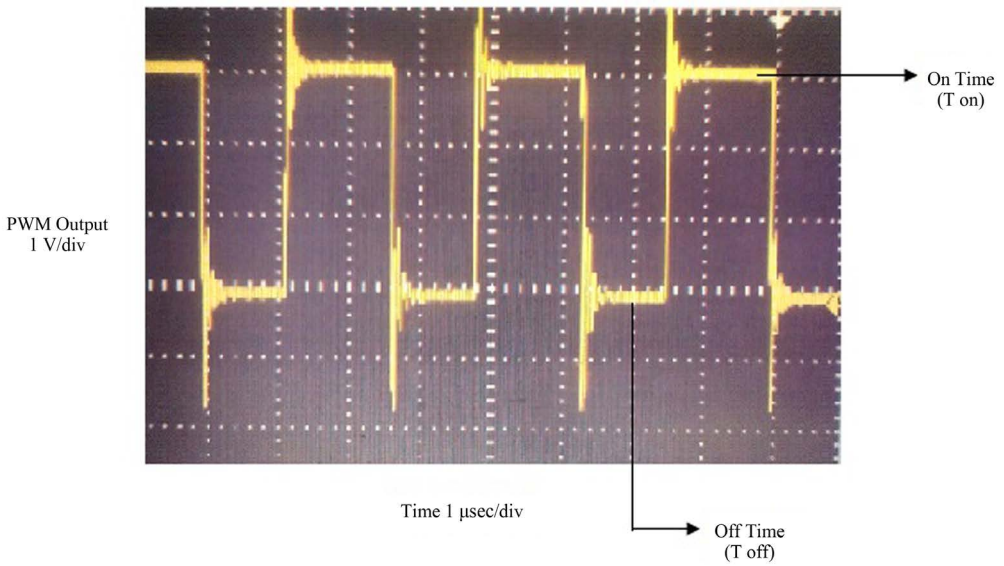

Figure 10. Digital storage oscilloscope waveform for duty cycle = 50%.

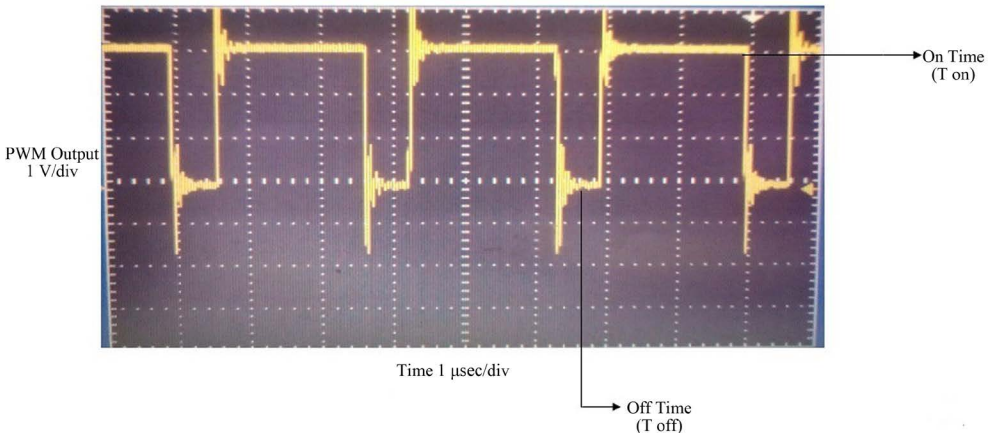

Figure 11. Digital storage oscilloscope waveform for duty cycle = 78.5%.

5. Conclusion

In this paper a new DPWM architecture for controlling the DC-DC converter with higher operating frequency was presented. The proposed method is based on the mealy machine with gray encoding scheme which has fewer states when compared to the sequential encoding scheme used in traditional architecture which makes them faster. This DPWM is easier to design and the resolution can also be changed easily. Operating frequency of the architecture differs depending on the target FPGA device and number of control input bits. Depending on the application requirements, the proposed DPWM architecture can be implemented in suitable FPGA device with necessary control input bits and clock frequency. The proposed DPWM architecture is verified experimentally with low-cost FPGA SPATRAN 3A. These PWM signals can be used as switching control for the DC-DC converter which regulates the output voltage.

References

[1] Gjanci, J. and Chowdhury, M.H. (2011) A Hybrid Scheme for On-Chip voltage Regulation in System-on-a-Chip (Soc). *IEEE Transactions on Very Large Scale Integration* (*VLSI*) *Systems*, **19**, 1949-1959. http://dx.doi.org/10.1109/TVLSI.2010.2072997

[2] Duan, Y. and Jin, H. (1999) Digital Controller Design for Switching Mode Power Converters. *Proceeding of the IEEE Applied Power Electronics Conference and Exposition* (*APEC*'99), **2**, 667-673

[3] Zhen, S.W., Zhang, B., Luo, P., Huo, S.j., Ye, J.X. and Ma, X. (2011) A Digitally Controlled PWM/PSM Dual Mode DC/DC Converter. *Journal of Semiconductors*, **32**, 115007-1-115007-7. http://dx.doi.org/10.1088/1674-4926/32/11/115007

[4] Syed, A., Ahmed, E. and Maksimovic, D. (2004) Digital Pulse Width Architectures. 35th *Annual IEEE Power Electronics Specialist Conference*, **6**, 4989-4995.

[5] Koutroulis, E., Dollas, A. and Kalaitzakis, K. (2005) High-Frequency Pulse width Modulation Implementation Using FPGA and CPLD ICs. *Journal of Systems Architecture*, **52**, 332-344. http://dx.doi.org/10.1016/j.sysarc.2005.09.001

[6] Navarro, D., Lucha, O., Barraghan, L., Artigas, J., Urriza, I. and Jimenez, O. (2012) Synchronous FPGA Based High Resolution Implementations of Digital Pulse Width Modulators. *IEEE Transactions on Power Electronics*, **27**, 2515-2525. http://dx.doi.org/10.1109/TPEL.2011.2173702

[7] Ofoli, A. and Rubaai, A. (2005) Real-Time Implementation of a Fuzzy Logic Controller for DC-DC Switching Converters. *Proceeding of the IEEE Annual Meeting Conference on Industrial Applications* (*IAS*'05), **2**, 1292-1299.

[8] Ramos, R., Roset, X. and Mhuel, A. (2000) Implementation of Fuzzy Logic Controller for DC/DC Converters Using Field Programmable Gate Array (FPGA). *IEEE Conference on Instrumentation and Measurement Technology* (*IMTC*'00), **1**, 160-163. http://dx.doi.org/10.1109/imtc.2000.846846

[9] Huerta, S., de Castro, A., Garcia, O. and Cabos, J. (2008) FPGA Based Digital Pulse width Modulator with Time Resolution under 2ns. *IEEE Transactions on Power Electronics*, **23**, 208-215. http://dx.doi.org/10.1109/TPEL.2008.2005370

[10] Castro, A.D. and Todorovich, E. (2010) High Resolution FPGA DPWM Based on Variable Clock Shifting. *IEEE Transactions on Power Electronics*, **25**, 1115-1119. http://dx.doi.org/10.1109/TPEL.2009.2037818

[11] Li, J., Qiu, Y., Sun, Y., Huang, B. and Xu, M. (2007) High Resolution Digital Duty Cycle Modulation Schemes for Voltage Regulators. *Proceeding of the IEEE Applied Power Electronics Conference and Exposition* (*APEC*'07), Anaheim, 25 February-1 March 2007, 871-876. http://dx.doi.org/10.1109/apex.2007.357617

[12] Batarseh, M.G., Al-Hoor, W., Huang, L., Lanella, C. and Bataresh, I. (2009) Window Masked Segmented Digital Clock Manager FPGA Based Digital Pulse Width Modulator Technique. *IEEE Transactions on Power Electronics*, **24,** 2649-2660. http://dx.doi.org/10.1109/TPEL.2009.2033066

[13] Yousefzadeh, V., Takayama, T. and Maksimovi, D. (2006) Hybrid DPWM with Digital Delay-Locked Loop. *Proceeding of the IEEE Work Shop on Computers in Power Electronics* (*COMPEL*'06), Piscataway, 16-19 July 2006, 14-48. http://dx.doi.org/10.1109/compel.2006.305666

[14] Vaidya, B. and Anupam, D. (2013) A Study of Different Finite State Machine Design and Efficient Encoding Techniques. *Journal of Information, Knowledge and Research in Electronics and Communication Engineering*, **2**, 493-496.

[15] Xilinx Application Note: Spartan 3 and Spartan 3L FPGA Families (2006).