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A Bi-Polar Triple-Output Converter with Duty Cycle Estimation

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Abstract

This paper proposes a triple output converter with buck, boost and inverted outputs and controlled through duty cycle estimation. In the existing converter, to generate the negative output, the power flows from load to the supply (from the boost output to the supply) during a part of the cycle, which increases cycle time and losses, and reduces the power level. To overcome this, a modified converter with a main and an auxiliary inductance and with reduced number of switches is proposed. The converter can operate in continuous and discontinuous conduction modes and the outputs can be independently controlled. An analysis of the converter is done for both modes. A simplified control of the converter through duty cycle estimation is suggested to regulate the outputs, which does not have the constraint that the current ripple has to be small. The control works both in the continuous and discontinuous modes. The simulation results closely match with the analysis. A prototype of the converter is constructed with a Spartan FPGA system and results have been presented.

Keywords

Multi-Output, Dual Output, DC-DC Converter, Predictive Control, Bi-Polar

1. Introduction

Multi-output DC-DC converters have become very popular recently and they are particularly used in many portable and handheld consumer applications. Portable devices use sub-modules which have different voltage requirements. Their small-size and light-weight make them very attractive and the cost is also optimized. Traditionally, isolated transformer-based multi-output DC-DC converters were widely employed to provide multiple output voltages. However, they are relatively bulky due to the presence of the reactive components. The single-

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inductor multi-output DC-DC converters were developed to effectively reduce the hardware required for providing multiple output voltages. The converters provide more than one output while requiring only one inductor and this helps in saving board space and reducing the overall cost. Multi-output converters apart from requiring buck and boost outputs also sometimes require a negative supply voltage as in an OLED display panel application. Hence it becomes necessary that the single converter supplies all the three types of voltages, step-down, step-up and a negative output simultaneously. Various such configurations have been discussed in literature [1]-[12]. Predictive control of DC-DC converters has been discussed in [13]-[16]. A Single-Inductor converter with all types, buck, boost and inverted outputs (SIBBI) has been proposed in [12] and is shown in **Figure 1**.

The inductor is initially charged by making S_0 ON. When S_0 is opened, S_1 is closed and the inductor charges the boost output V_1. The inductor current is allowed to become zero after which the boost output charges the inductor in the opposite direction through the body diode of the switch S_1 and through the supply. Thus power is returned back to the supply for the sake of charging the inductor in the reverse direction. When the switch S_1 is opened, S_2 is closed and the stored energy in the inductor is partly transferred to the negative output V_2. When S_2 is opened, S_3 is closed and power is transferred to the buck output V_3 through the inductor L. This converter while providing all the three types of outputs has the problem that there is a reverse power flow from the load to the supply to generate the inverted output. This increases the ripple since the current has to pass through zero, twice in a cycle. The cycle time and losses are also increased.

The problems mentioned above are overcome in the proposed converter with reduced number of switches as shown in **Figure 2**. The converter is capable of generating buck, boost and inverted outputs simultaneously. The single inductor is split into two separate inductors L_1 and L_2 in the proposed converter. V_1 is the boost output, V_2 is the inverted output and V_3 is the buck output. C_1, C_2, and C_3 are the output filter capacitors to the outputs V_1, V_2, and V_3, respectively, where R_1, R_2 and R_3 are the corresponding loads. These three outputs are achieved by using two inductors (L_1, L_2) with three switches (S_0, S_1 and S_2). In the proposed configuration, the voltage levels of all three outputs can be adjusted by varying the duty cycles of switches S_0, S_1, and S_2. S_0 is ON for the time dT_s, S_1 is ON for the time d_2T_s and S_2 is ON for the time d_1T_s in every cycle where T_s is the cycle time period. The inductor L_1 is charged through switch S_0 during dT_s and simultaneously L_2 and the buck output is powered through switch S_2 for duration of d_1T_s. Once S_0 is turned OFF, $D1$ turns ON to drive the inverted output (V_2) for the rest of the cycle if V_2 is operating in continuous conduction mode. When switch S_2 is turned off, S_1 is turned ON to store additional energy required by the boost output in the inductor for duration of d_2T_s. When S_1 is turned off, the stored energy in the inductor L_2 is transferred to the boost output V_1 through diode D_3 for the balance duration d_3T_s.

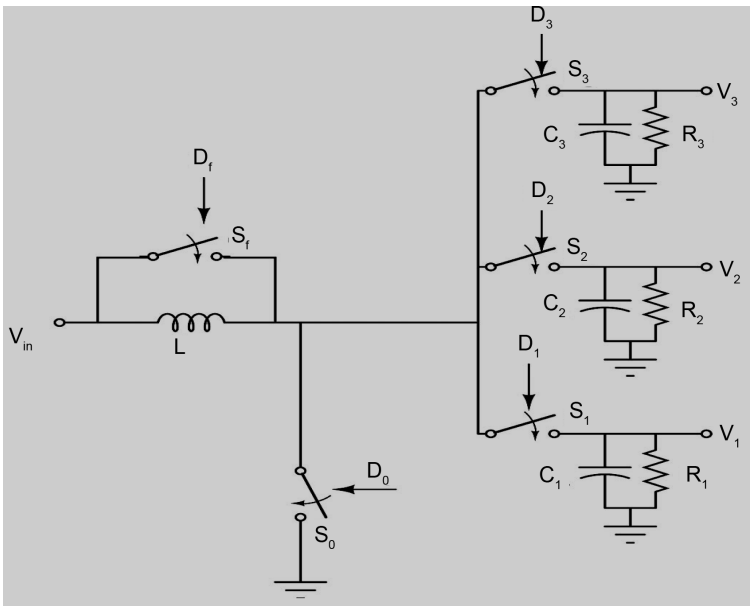


Figure 1. Converter with buck, boost, inverted outputs.

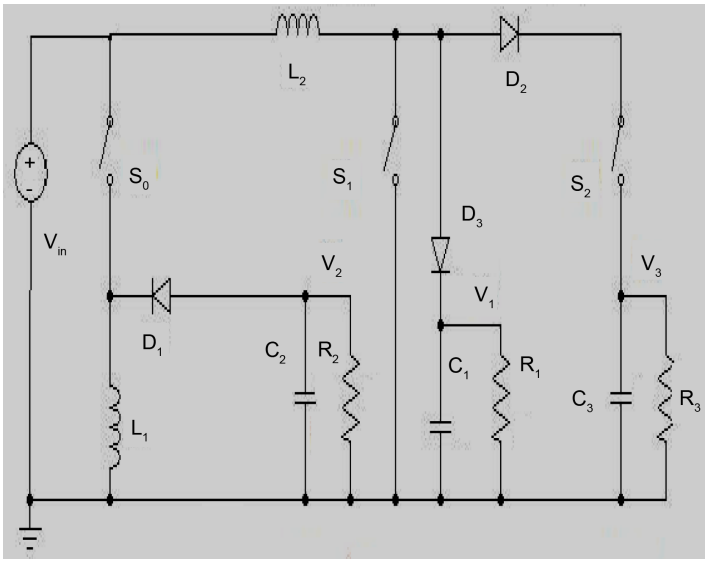


Figure 2. Proposed converter with buck, boost, inverted output.

If the converter is operating in discontinuous conduction mode, the cycle repeats after a dead time. For operation in continuous conduction mode, the inductor current reaches its steady-state minimum value at the end of d_3T_s. There are five modes of operation in the converter. The inductor current waveforms are shown in **Figure 3** for discontinuous operation mode of buck and boost outputs.

2. Modes of Operation

The equivalent circuits during the modes are shown in **Figures 4(a)-(d)**.

2.1. Mode 1

Initially, at the beginning of the cycle, the switches S_0 and S_2 are turned ON and the inductors L_1 and L_2 are charged simultaneously for duration of dT_s and d_1T_s respectively. During the charging of the inductor L_2, the buck output is also simultaneously fed power.

2.2. Mode 2

In mode 2, the switch S_0 is turned OFF and the diode D_1 becomes forward biased and starts conducting. The energy stored in the inductor L_1 is discharged through D_1 (*i.e.* the current flows from inductor L_1 through D_1) to drive the inverted output for the balance duration in the cycle.

2.3. Mode 3

In this mode, the switch S_2 is turned OFF when the requirement of buck output is met. The switch S_1 is turned ON to further charge inductor L_2 since the boost output may require more energy than what is already stored in the inductor L_2 to produce the required output voltage.

2.4. Mode 4

When switch S_1 is turned OFF, the stored energy in the inductor L_2 is completely transferred to the boost output through diode D_3 till the current becomes zero.

2.5. Mode 5

After a dead time given by $T_s * (1 - d_1 - d_2 - d_3)$, the cycle repeats.

The modes of operation for the continuous conduction mode are similar to the above with the difference that

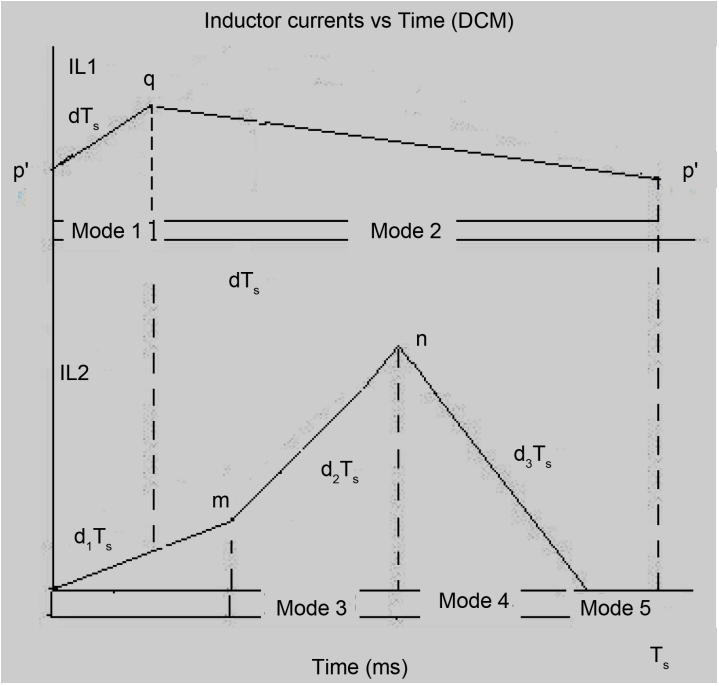


Figure 3. Inductor current waveforms of L_1 and L_2 (DCM).

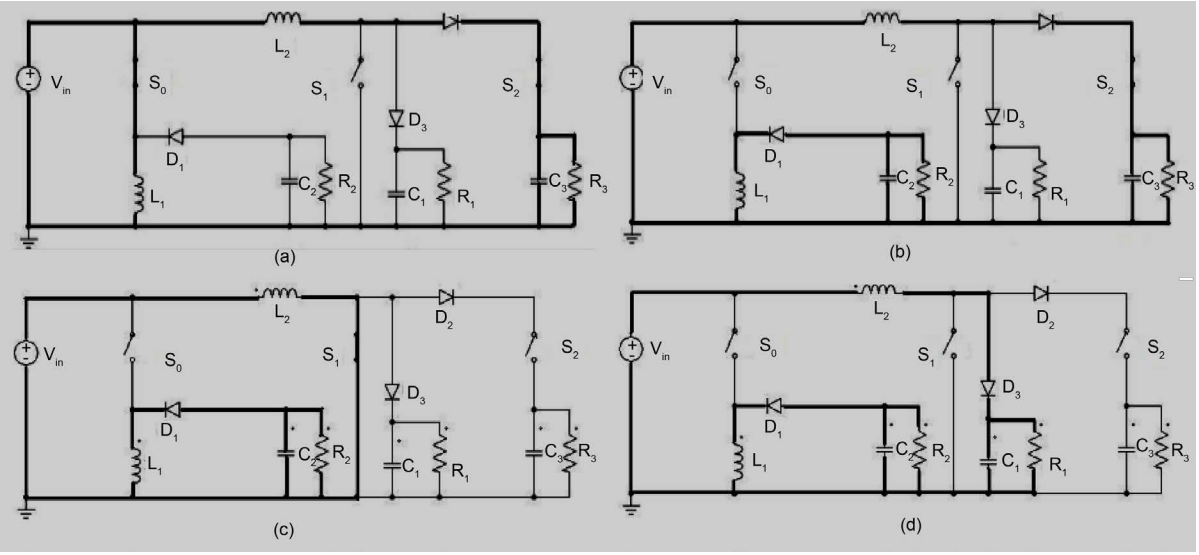


Figure 4. (a) Equivalent circuit for Mode 1. (b) Equivalent circuits for Modes 2. (c) Equivalent circuits for Mode 3. (d) Equivalent circuits for Mode 4.

that the current starts from a value of "*m*" in the beginning of the cycle and at the end of the cycle, it again reaches "*m*" (at steady state). The inductor current waveforms are shown in **Figure 5**.

3. Steady State Analysis and Design

3.1. Discontinuous Conduction Mode (DCM)—Figure 3

During Mode 1, from volt-second balance of inductor L_2,

$$m = \left(V_s - V_3\right) d_1 T_s / L_2$$

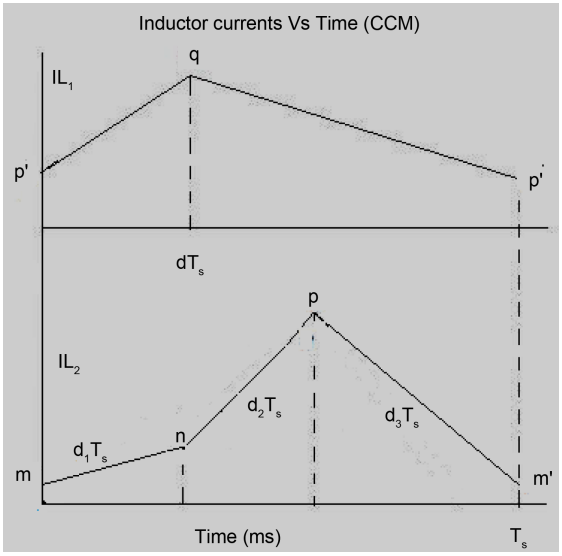


Figure 5. Inductor current waveforms of L_1, L_2 (CCM).

$$T_s/L_2 = a\,,\quad m/d_1 = a\left(V_s - V_3\right) \tag{1.1}$$

From capacitor charge-balance considerations,

$$\left(m/2\right)d_1T_s = \left(V_3/R_3\right)T_s\,,\ \text{or}$$

$$md_1 = 2V_3/R_3 \tag{1.2}$$

During Mode 2, the inductor current rises from "*m*" to "*n*". Applying volt-second balance

$$\left(n-m\right)/d_2 = aV_s \tag{1.3}$$

During Mode 3, the current falls from "*n*" to zero. Applying volt-second balance for the inductor L_2,

$$n/d_3 = -a\left(V_s - V_1\right) \tag{1.4}$$

Applying charge balance consideration to the boost output,

$$\left(n/2\right)d_3T_s = \left(V_1/R_1\right)T_s \quad \text{or} \quad nd_3 = 2V_1/R_1 \tag{1.5}$$

For discontinuous conduction mode operation, the dead time gives an additional degree of freedom which helps to achieve a unique solution. If the dead time is chosen as 5%, the sum of the three duty cycles d_1, d_2 and d_3 would be 0.95 which is a required design equation.

$$d_1 + d_2 + d_3 = 0.95 \tag{1.6}$$

Since $\left(T_s/L_2\right) = a$ is considered as one variable, there are 6 variables, "d_1", "d_2", "d_3", "*m*", "*n*" and "*a*" and six equations from (1.1) to (1.6). Hence an unique solution can be obtained. Knowing "*a*" and choosing T_s, L_2 can be obtained. The negative output is from a buck-boost converter whose output voltage (for continuous conduction) is

$$\left(V_2/V_s\right) = -d/\left(1-d\right) \tag{1.7}$$

The inductor value L_1 can be obtained based on ripple considerations. Assuming a permitted inductor ripple current of "*r*" % of the rated current,

$$\left(q - p'\right) = \left(r/100\right)\left(V_2/R_2\right) \tag{1.8}$$

From volt-second balance of inductor L_1,

$$\left(q - p'\right) = V_s \cdot d \cdot T_s/L_1 \tag{1.9}$$

From (1.7), (1.8) and (1.9),

$$L_1 = (1-d)T_s R_2 / (r/100) \tag{1.10}$$

From (1.10), L_1 can be obtained for a permitted ripple "r". As a design example, the specifications for a chosen converter is shown in **Table 1**. The corresponding design parameters are obtained from Equations (1.1) to (1.10) above. The value of "a" is obtained as "1" and choosing a switching frequency of 50 KHz, the time period is 20uS and the inductance value L_2 is obtained as 20 uH. Inductance value L_1 is found to be 141 uH. The duty cycles are found to be $d_1 = 0.535$, $d_2 = 0.053$ and $d_3 = 0.365$.

3.2. Range of Operation

While the buck output is supplied, the inductor is also charged along with it. The energy stored in the inductor at the end of the buck operation may not be adequate for supplying the boost output and additional charging may be required for the time duration $d_2 T_s$. The condition for this is obtained as follows:

For d_2 to exist, n should be greater than "m" and $n^2 \geq m^2$. From (1.1) and (1.2)

$$m^2 = (2V_3/R_3)(V_s - V_3)a \tag{1.11}$$

From (1.4) & (1.5),

$$n^2 = -2V_1(V_s - V_1)a/R_1 \tag{1.12}$$

For $n^2 \geq m^2$, using (1.11) and (1.12) and simplifying,

$$(P_1 + P_3)/V_s \geq I_1 + I_3$$

is the required condition, where P_i and I_i are the load power and load current of the ith output.

3.3. Continuous Conduction Mode (CCM)—Figure 5

From volt-second considerations of inductor L_2,

$$(V_s - V_3)/L_2 = (n-m)/d_1 T_s \tag{1.13}$$

$$V_s/L_2 = (p-n)/d_2 T_s \tag{1.14}$$

$$(V_s - V_1)/L_2 = (m'-p)/d_3 T_s \tag{1.15}$$

From output capacitor charge balance considerations,

$$(m+n)d_1/2 = V_3/R_3 = a' \tag{1.16}$$

$$(m'+p)d_3/2 = (V_1/R_1) = b' \tag{1.17}$$

$$d_1 + d_2 + d_3 = 1 \tag{1.18}$$

Table 1. Specifications of converter.

Circuit parameters	Values
Supply voltage V_s	12 V
Switching frequency	50 KHz
Load resistance R_1	30 Ω
Load resistance R_2	10 Ω
Load resistance R_3	5 Ω
Output voltage V_1	24 V
Output voltage V_2	−5 V
Output voltage V_3	+5 V

There are 7 variables, "d_1", "d_2", "d_3", "m", "n", "p", "T_s/L" and six equations from (1.13) to (1.18). Since there are 6 equations for 7 variables, there is no unique solution and several solutions are possible. For higher values of "m", the average current to each output increases and ripple decreases, T_s/L_2 would decrease and L_2 would increase for particular T_s. The solution can be obtained from any iterative software and a typical solution for a switching frequency of 50 KHz is L_1 as 141 µH, L_2 as 87 µH, d_1 as 0.52, d_2 as 0.09 and d_3 as 0.39. The simulation of the system was done using PSIM software with the specifications of the converter as given in **Table 1**. The simulation waveforms for the inductor currents, switch currents and output voltages for the converter are shown in **Figures 6(a)-(e)** for discontinuous conduction mode. The waveforms for continuous conduction mode are shown in **Figures 7(a)-(f)**.

4. Control through Duty Cycle Estimation

The control strategy followed in this paper is based on the approaches suggested by Zhonghan Shert *et al*. in [16] and Chen in [13]. The valley current measured at the beginning of the present cycle and the duty cycles of the present cycle are used to predict the valley current at the beginning of the next cycle. This information along with the outputs of the voltage regulators (corresponding to the different outputs) are used as input information, to estimate the duty cycles for the next cycle. In the method suggested in [16], to simplify the equations, the authors have assumed that the inductor ripple current is small. In the proposed method, since we are directly determining the currents at every switching transition analytically, we are able to solve the equations exactly and hence this constraint of small ripple current is redundant and the control works even for smaller inductances with larger ripples. This is shown in **Figure 8(i)** where the waveforms are shown for an inductor value of 7.5 µH instead of 30 µH. The prediction part of the control is limited to determining the current at the beginning of the next cycle from the present duty cycle and current information.

The output of the PI voltage regulator for a particular output indicates the demanded current and this must

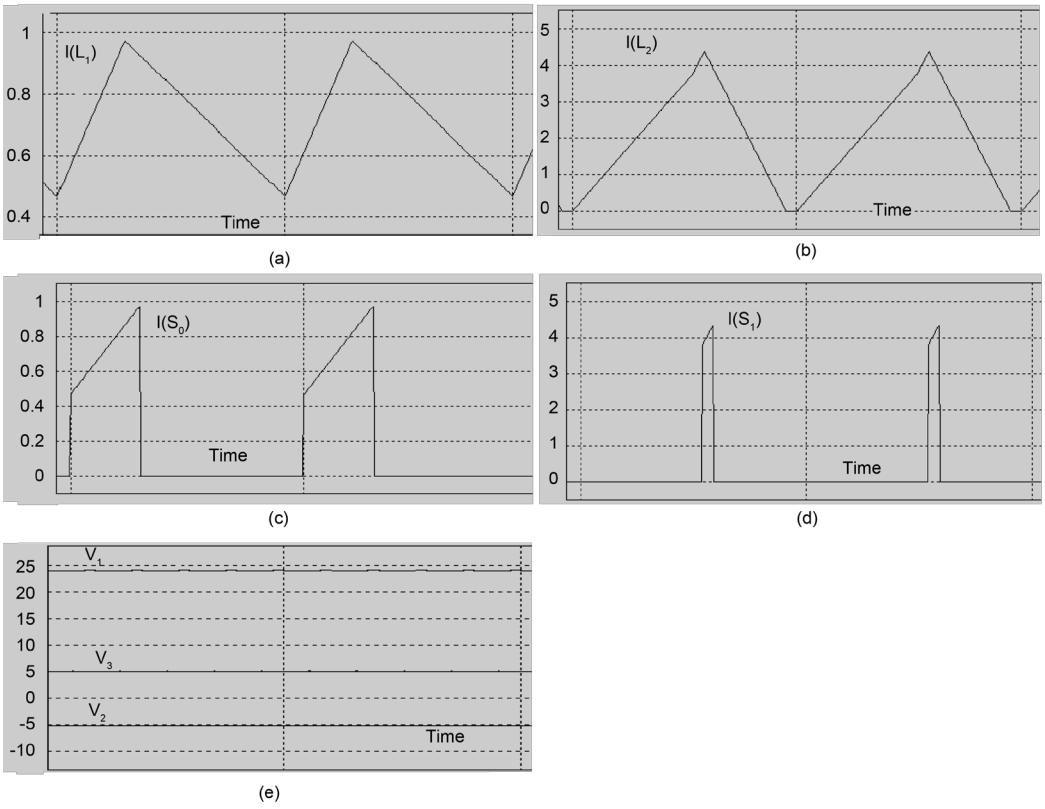


Figure 6. (a) Inductor current L_1 (Amps) in DCM V_s time. (b) Inductor current L_2 (Amps) in DCM V_s time. (c) Switch current S_0 (Amps) in DCM Vs time. (d) Switch current S_0 (Amps) in DCM V_s time. (e) Output Voltages.

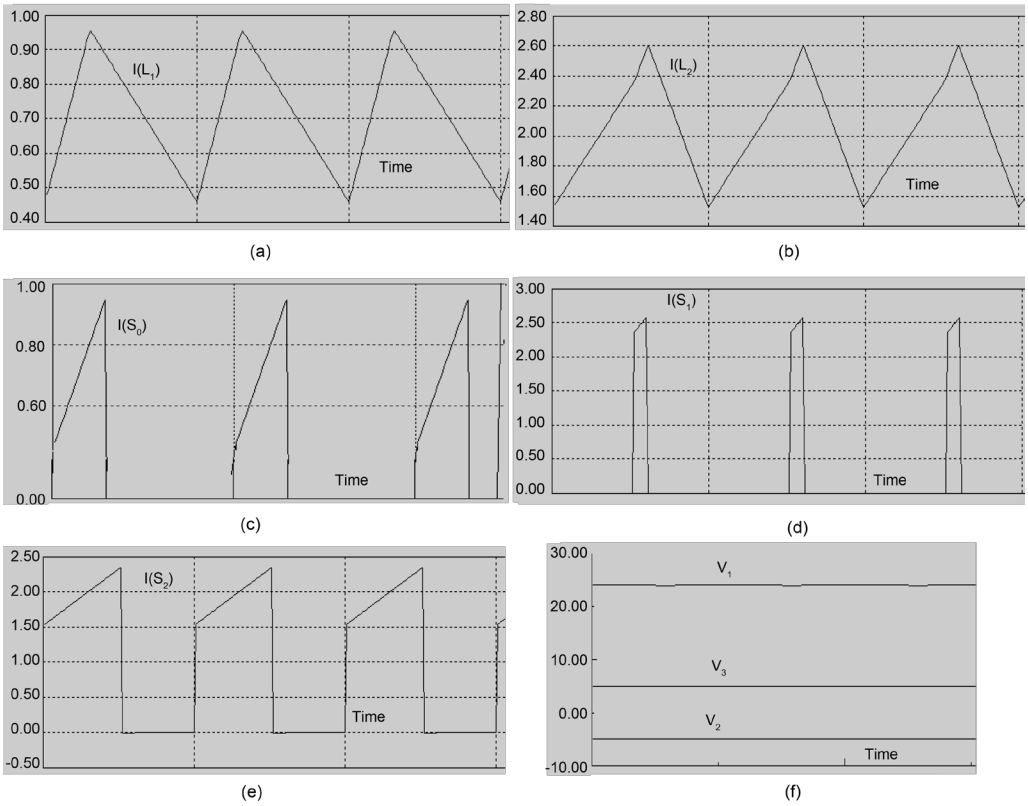


Figure 7. (a) Inductor current (Amps) of L_1 in CCM V_s time (V_1 = 24 V, V_2 = −5 V, V_3 = 5 V). (b) Inductor current (Amps) of L_2 in CCM Vs time. (c) Switch current (Amps) of S_0 in CCM V_s time. (d) Switch current (Amps) of S_1 in CCM V_s time. (e) Switch current (Amps) of S_2 in CCMVs time. (f) Output Voltage (Volts) in CCM V_s time (V_1 = 24 V, V_2 = −5 V, V_3 = 5 V).

relate to the overall average inductor current during the period when power is discharged in to the particular buck/boost output. Using this property, the duty cycles for the different modes are estimated. The duty cycles of the different modes are predicted based on the present duty cycles and the current demand of the two outputs. The actual (valley) current at the beginning of the cycle is measured and this corresponds to the value of "*m*" in the equations (1.13) to (1.18) discussed above. The current "*m*" is typically measured with an analog-digital converter like TLC1541. Multiple current measurements are not required and only one sample is required at the beginning of a full time period. Alternatively, a current mirror concept can also be used. The buck and boost outputs are compared with their set points and the error signals are passed through PI regulators. The output of the regulators for the buck and boost outputs are denoted as a' and b' in the equations (1.16) and (1.17).

$$n^2 - m^2 = 2a'\left(V_s - V_3\right)T_s/L \tag{1.19}$$

$$n = \sqrt{m^2 + 2a'\left(T_s/L\right) * \left(V_s - V_3\right)} \tag{1.20}$$

Choosing (T_s/L) and measuring "*m*", "*n*" can be found. From (1.13), since "*n*" is found, d_1 can be obtained as

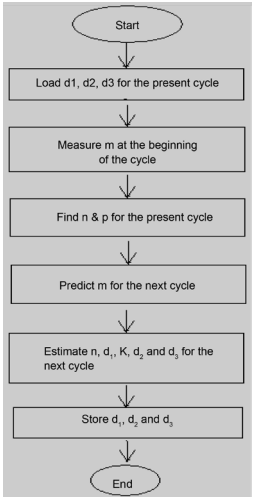
$$d_1 = \left(L/T_s\right)\left(n - m\right)/\left(V_s - V_3\right) \tag{1.21}$$

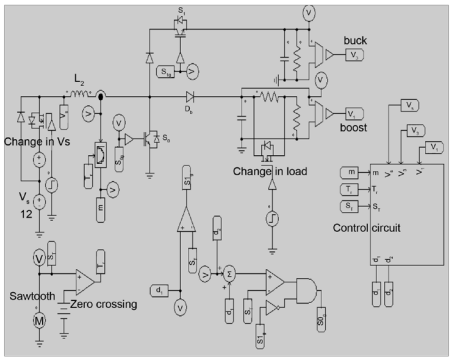
The average inductor current during mode 2 (say "K") can be obtained as the difference between the overall average inductor current and the sum of the average currents of the two outputs as

$$\left\{\left(a'V_3 + b'V_1\right)/V_s - \left(a' + b'\right)\right\} = \left(p + n\right)d_2/2 \tag{1.22}$$

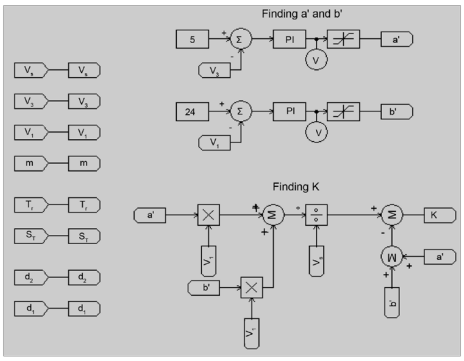
Combining (1.22) with (1.14), d_2 can be obtained as

$$d_2 = \left\{-n + \sqrt{n^2 + \left(2V_sT_s/L\right)K}\right\}\Big/\left(V_sT_s/L\right) \tag{1.23}$$

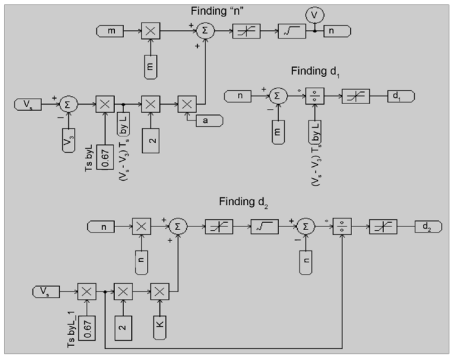

Start
Load d1, d2, d3 for the present cycle
Measure m at the beginning of the cycle
Find n & p for the present cycle
Predict m for the next cycle
Estimate n, d1, K, d2 and d3 for the next cycle
Store d1, d2 and d3
End


buck
boost
Change in Vs
Change in load
Control circuit
Sawtooth
Zero crossing

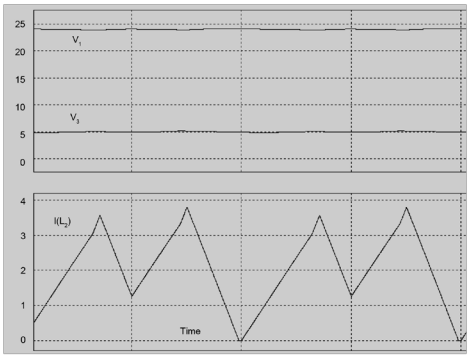
(a)


Finding a' and b'
Finding K

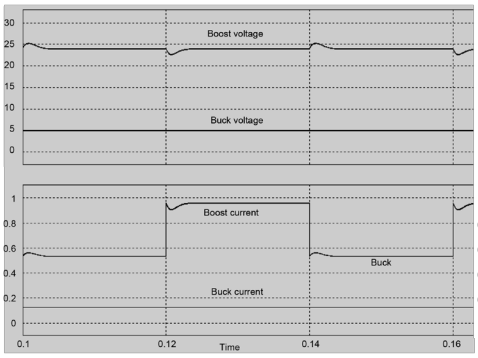
(b)


Finding "n"
Finding d1
Finding d2

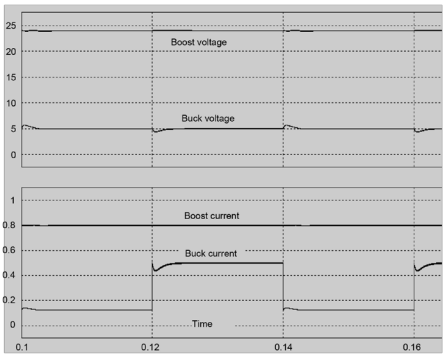
(c)


Time

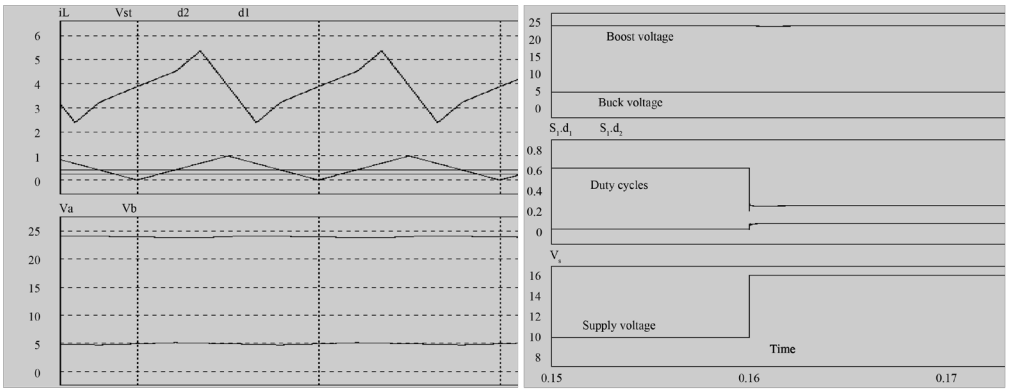
(d)


Boost voltage
Buck voltage
Boost current
Buck current
Buck
Time

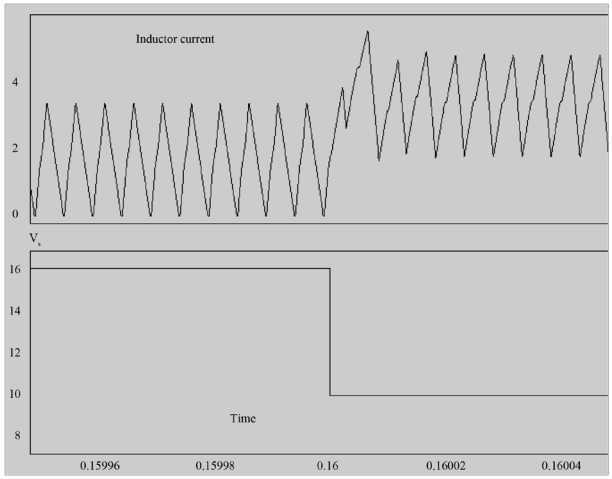
(e)


Boost voltage
Buck voltage
Boost current
Buck current
Time

(f)



(g) (h)



(i)

Figure 8. Prediction control algorithm. (a) Power and control schematic-Part 1. (b) Power and control schematic-Part 2. (c) Power and control schematic-Part 3. (d) Output voltages and inductor current (L = 30 µH). (e) Change in boost load from 0.53 to 0.96 A (L = 30 µH). (f) Effect of sudden change in buck load (L = 30 µH). (g) Output voltage, Inductor current, Triangular carrier. (h) Change in supply from 10 to 16 V (L = 7.5 µH). (i) Change in supply from 16 to 10 V (L = 7.5 µH).

Knowing d_1 and d_2, d_3 can be found as

$$d_3 = 1 - d_1 - d_2 \tag{1.24}$$

The algorithm for the prediction control is shown in **Figure 8**. The control block diagram is shown in **Figures 8(a)-(c)** below for the buck and boost outputs. The inverted output is an independent output and can be controlled without any difficulty. The closed loop simulation results for the buck and boost outputs are shown in **Figures 8(d)-(i)**. The inductor current (without slope compensation) and the output voltages are shown in **Figure 8(d)**. The effect of a sudden change in the boost output between 0.53 to 0.96 A is shown in **Figure 8(e)**. Similarly, the effect of a sudden change in the buck output between 0.125 to 0.5 A is shown in **Figure 8(f)**. The output voltages are found to be closely regulated and no cross regulation are observed. The period-doubling current oscillations can be removed by using a triangular carrier as suggested by Chen *et al*. (2003) and the corresponding inductor current and output voltages along with the carrier waveforms are shown in **Figure 8(g)**.

To highlight the fact that the predictive control also works for a large ripple, the inductance value was changed from 30 µH to 7.5 µH and for a sudden change in supply voltage between 10 and 16 V, the output voltages, duty cycles and inductor current waveforms are shown in **Figures 8(h)-(i)**. In **Figure 8(h)**, for a sudden increase in the supply voltage from 10 to 16 V, the duty cycles adjust themselves to maintain the output voltages at the required values. Similarly, for a sudden drop in supply voltage, the inductor current smoothly rises as shown in **Figure 8(i)** to regulate the outputs.

5. Experimental Results

The hardware implementation is done for the converter in discontinuous mode using an FPGA controller, Spartan 3E XC3S250E system working at a clock frequency of 20 MHz. The pulses generated from the FPGA controller are passed through opto-couplers 6N137 and then given to the driver TC4584BP. They are then used to switch the MOSFETs IRF 840. The hardware waveforms are given in **Figures 9(a)-(e)** and the hardware setup is shown in **Figure 10**.

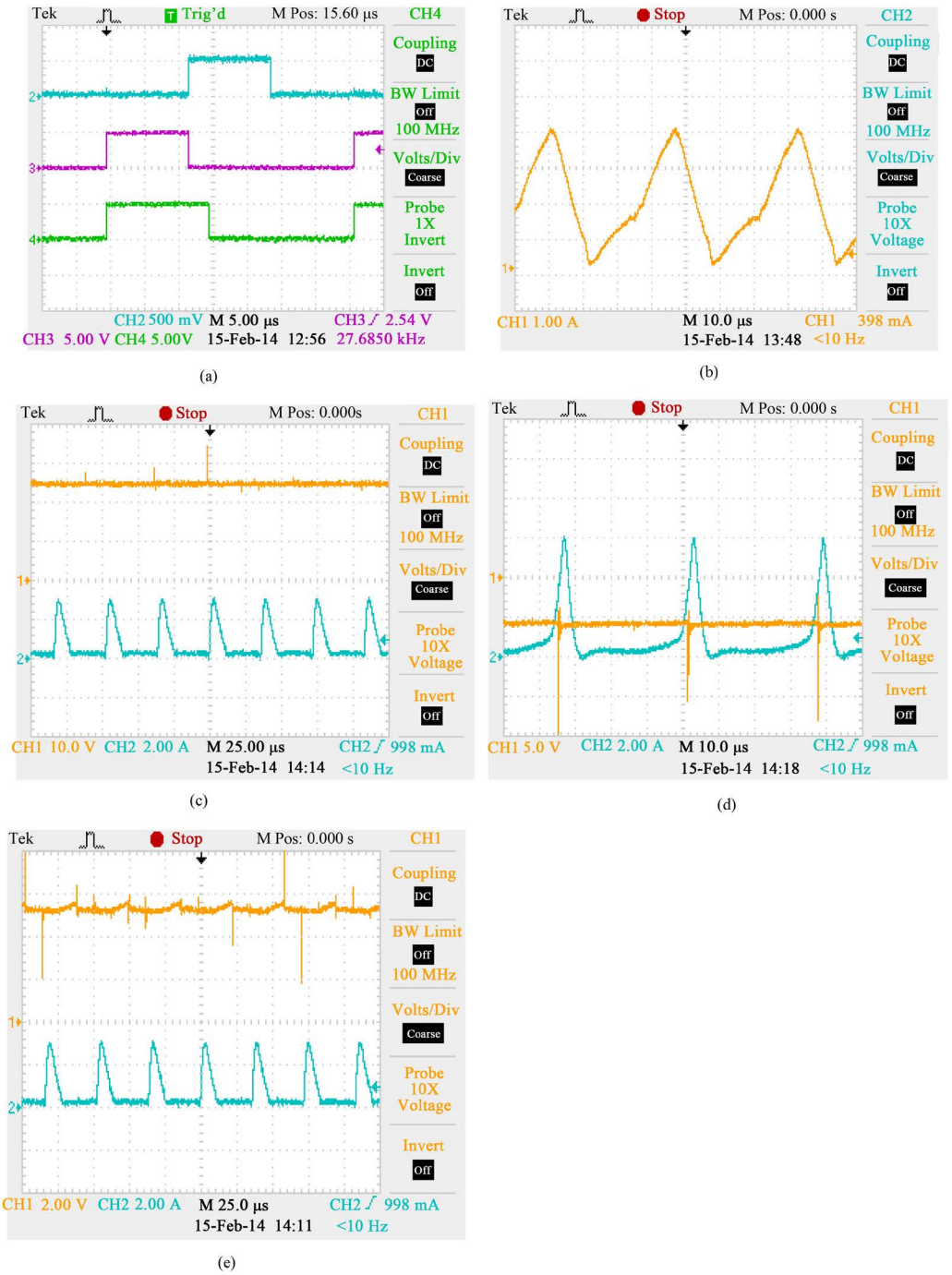


Figure 9. (a) Gate pulses to the switches. (b) Inductor current waveform. (c) Boost output. (d) Inverted output. (e) Buck output.

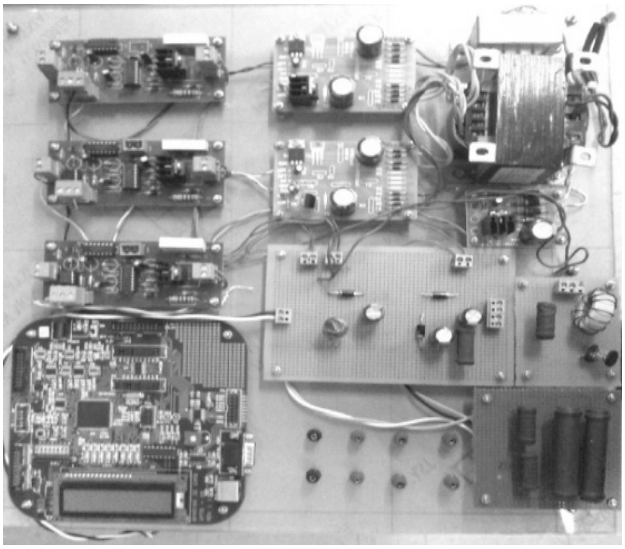


Figure 10. Hardware setup.

6. Conclusion

This paper proposed an alternate converter with a main and an auxiliary inductor, capable of generating both positive and negative outputs and in both buck and boost configurations. The topology does not involve any reverse power flow to the supply and hence time periods can be shorter and higher power levels are possible. The topology is validated through simulation using PSIM software and further through hardware results obtained with a Spartan FPGA system. The suggested topology is generic and is extendable to more outputs. A novel control method through duty cycle estimation has been suggested which is capable of regulating output voltages against line and load disturbances. Since the duty cycles of the next time period are estimated in the present cycle by direct computation, the control method is capable of overcoming cross-regulation issues.

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