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The Design of Ultra-Low Power Adder Cell in 90 and 180 nm CMOS Technology

Masoud Sabaghi[1*], Saeid Marjani[1,2], Abbas Majdabadi[1]

[1]Laser and Optics Research School, Nuclear Science and Technology Research School, Atomic Energy Organization of Iran, Tehran, Iran
[2]Department of Electrical Engineering, Ferdowsi University of Mashhad, Mashhad, Iran
Email: *msabaghi@aeoi.org.ir

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Abstract

In this paper, an ultra-low power adder cell is proposed. With cascading two XNOR cells, the sum of two inputs is achieved. Regarding to advantages of m-GDI XNOR cell, we constructed the adder cell based on this architecture. The simulation results show that the power consumption of the adder cell designed with GDI technology is 12.993 µw, whereas for this cell designed with m-GDI technology is 4.1628 µw, which both are designed at 0.18 um technology. Moreover, simulation results in 90 nm CMOS technology for m-GDI adder cell show average power consumption of 0.90262 µw and 6.3222 µw in 200 MHz and 2GHz, respectively.

Keywords

Adder Cell, Gate-Diffusion-Input (GDI), Bit-Serial Adder

1. Introduction

The adders are the most common arithmetic circuits in digital systems as key components of multipliers and dividers that are used to do subtraction. There are several types of adders with different configurations, speeds and areas that we can select an appropriate one which satisfies our requirements. When information transferring is serial to reduce wiring, the serial adders are generally used [1]-[3]. The adder is one section of comparator (digital-comparator) [4]-[6] and successive approximation ADC control system [7] [8]. Also, the adder implements the delta-sigma analog to digital converter (decimation filter) [9]-[12]. Analog adder circuit is one of important sections in phase locked loop that is used in the cavity to maintain the mode locking conditions for lasers [13]-[22] and VCSELs [23]-[35].

*Corresponding author.

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The design of a 4-bit serial adder in 90 nm technology and supply voltage of 1.2 V is the goal of this paper. At first, the most important step of designing is choosing an adder cell which meets our requirements. Ideally, we have to use a full adder with minimum transistors in order to consume little power and occupy minimum space on the die. During the last years in the worldwide market, the increase in the demand of complex mobile systems led the designers to take into account a novel objective in the design of complex digital circuits including the minimization of power consumption. One of the most important reasons that fuel the need for an ultra-low power design is the high diffusion of systems such as laptop, cellular phones, wireless modems and portable multimedia applications. Also, the need for minimization of power dissipation of a system is enforced by some thermal considerations like a large percentage of the energy demanded by a device from the power supply which is converted into heat. In this way, the heat dissipation system and cooling mechanisms become indispensable for the correct, reliable and safe operation of the device. An increase of 10˚C in the working temperature of an electronic device causes a 100% increase in its failure rate. Therefore, it is possible to reduce the associated costs for expensive cooling and complex packaging needs if it is possible to decrease the heat dissipation.

The registers are other undividable parts of serial adders that consist of the latches. The cascading D Flip-flops is the simplest way to build the registers. We can achieve this register by cascading 4 D Flip-Flops since our design goal is a 4-bit adder. Choosing of proper D Flip-Flops is of our interests that beside high reliability, meet our requirements of lower power consumption and high speed. Finally, post-layout simulation will be accomplished to bring parasitic capacitances existing in the die to account. The paper is organized as follows: Section 2 briefly describes the serial adder, Section 3 provides the details of the proposed ultra-low power full adders, and Section 4 presents the results and discussions. Finally, in Section 5, we conclude.

2. Serial Adder

A serial adder operates similarly to manual addition. The serial adder, at each step, calculates the sum and carries at one bit position. It starts at the least significant bit position and each successive next step it sequentially moves to the next more significant bit position where it calculates the sum and carry. At the *n*-th step, it calculates the sum and carries at the most significant bit position. In other words, the serial adder serially adds augend X and addend Y by adding xi, yi, and c_i at the i-th bit position from $i = 0$ to $n - 1$. We have sum bit $s_i = x_i \oplus y_i \oplus c_i$ and carry to the next higher bit position

$$c_{i+1} = x_i \cdot y_i \oplus c_i \cdot (x_i \oplus y_i)$$

where "·" is AND, "∨" is OR, and "⊕" is XOR, and henceforth, "·" will be omitted. This serial addition can be realized by the logic network, called a serial adder, or bit-serial adder. The addition of each i-th bit is done at a rate of one bit per cycle of clock, producing sum bits, si's, at the same rate, from the least significant bit to the most significant one. In each cycle, s_i and c_{i+1}, are calculated from x_i, y_i, and the carry from the previous cycle, c_i. The core logic network, shown in the rectangle in **Figure 1**, for this one-bit addition for the i-th bit position is called a full adder (FA).

The 1-Bit full adder design is one of the most critical components of a processor that determines its throughput, as it is used in ALU, the floating point unit, and address generation in case of cache or memory accesses. The logic symbol and truth table for a full adder circuit are shown in **Figure 2**. The logic functions for the sum and carry outputs can be written as:

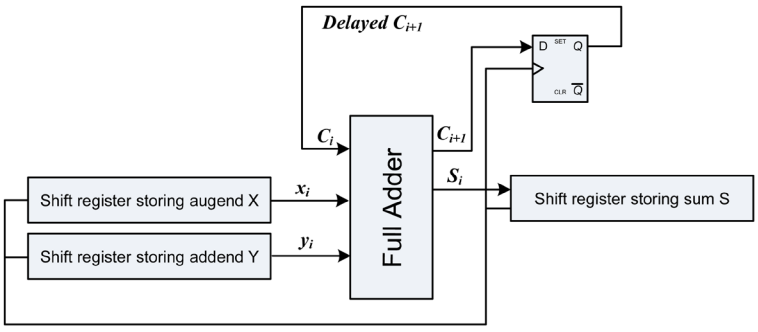
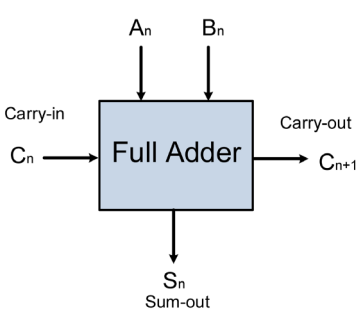


Figure 1. A serial adder.



An	Bn	Cn	Sn	Cn+1
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 2. The logic symbol and truth table for a full adder.

$$s_i = x_i \oplus y_i \oplus c_i \tag{1}$$

$$c_{i+1} = x_i \cdot y_i \oplus c_i \cdot \left(x_i \oplus y_i\right) \left(\text{also} c_{i+1} = x_i \cdot y_i \oplus c_i \cdot \left(x_i \oplus y_i\right)\right). \tag{2}$$

We obtain the logic network for a FA shown in **Figure 3** using AND, OR, and XOR gates. A D-type flip-flop may be used as a delay element which stores the carry for a cycle [3]. We can obtain this cell using conventional CMOS logics, but it highly suffers from large number of transistors and therefore high power consumption, large occupied are. As a results other structures, with less transistors are proposed.

3. The Proposed Ultra-Low Power Full Adders

3.1. 8 Transistors (8-T) Full Adder

As shown in **Figure 4**, the 8-T full adder contains three modules-two 3-T XOR gates and a 2-transistor multiplexer (2-T MUX). Owing to the appealing traits of a small number of transistors and a mere 2-transistor (2-T) delay, it can work at high speed with low power dissipation.

3.2. 10 Transistors (10-T) Full Adder

The 10-T full adder consists of four modules, including one 3-T XOR gate, one 3-T XNOR gate, and two 2-T multiplexers (2-T MUX) as shown in **Figure 5**. According to the logic equations and the GDI XOR and XNOR gates, full adders can be redesigned in two patterns including GDI XOR full adder and GDI XNOR full adder. Compared to the 8-T full adder, the GDI adders may be slightly slower, since more transistors are used in GDI circuits. As is well known, the number of transistors in circuits can influence performance in many aspects, especially speed.

3.3. GDI (Gate-Diffusion-Input) XOR Full Adder

The transistor level implementation of GDI XOR full adder is shown in **Figure 6**. This full adder consists of three modules-two GDI XOR gates and a multiplexer. In the worst case, *Sum* has 4-T delay while *Cout* has 3-T delay. However, due to the advantages of GDI cell, this circuit still can achieve its benefit of low power consumption [36]-[38].

Figure 7 shows the GDI XNOR full adder which is another basic architecture of the application of GDI cells. This scheme also includes three modules. It contains two GDI XNOR gates and a multiplexer. In the worst route, *Sum* has 4-T delay and *Cout* has 3-T delay [39]. The other new leaf cells and the circuits built on the basis of GDI technique is presented by P. Balasubramanian *et al.* and is called m-GDI technique [36]. The structure of a XNOR m-GDI cell is shown in **Figure 8**.

3.4. The Proposed Adder Cell

With cascading two XNOR cells we can achieve the sum of two inputs, regarding to advantages of m-GDI XNOR cell, we constructed the adder cell based on this architecture. The output carry can be resulted of a GDI cell shown in **Figure 9**. The simulations show low high to low speed of carry out when input A is high, input B is low and carry in is low. A restoration PMOS is used to implement the carry out.

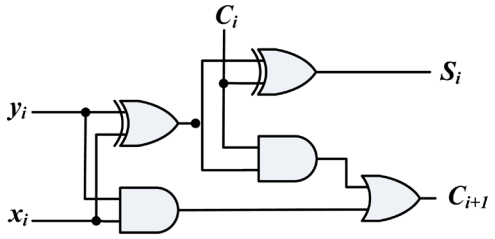


Figure 3. The logic network for a full adder.

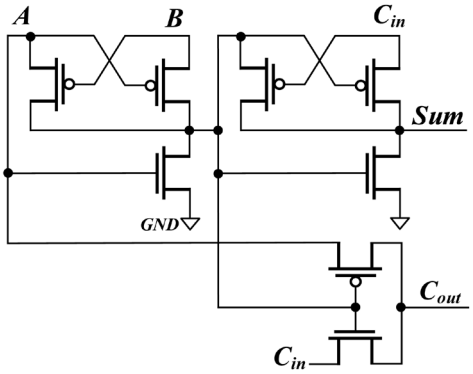


Figure 4. The 8 transistors full adder.

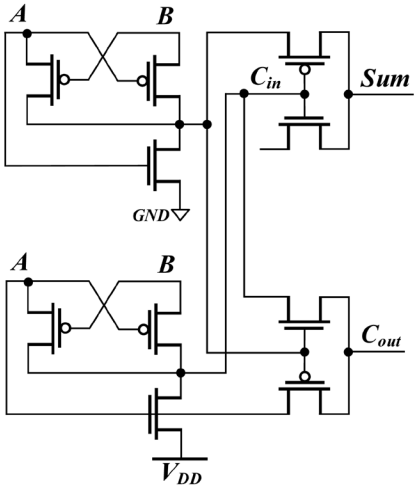


Figure 5. The 10 transistors full adder.

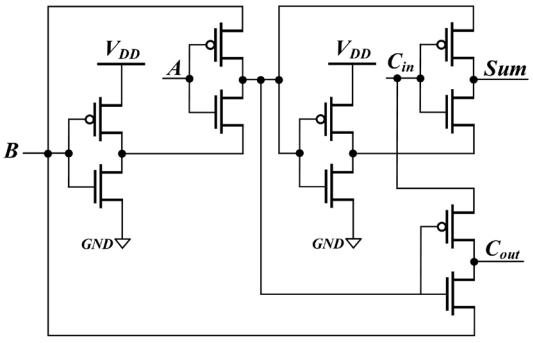


Figure 6. The GDI XOR full adder.

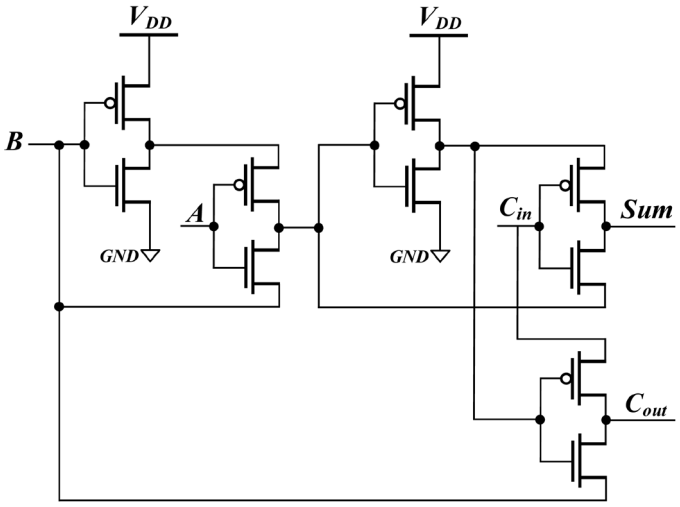


Figure 7. The GDI XNOR full adder.

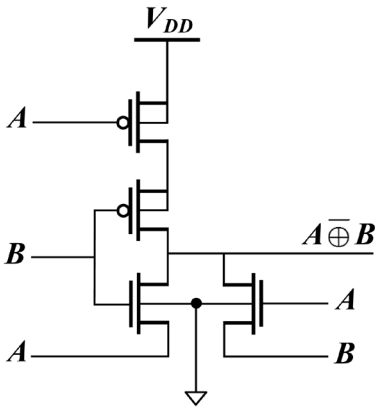


Figure 8. The m-GDI XNOR cell.

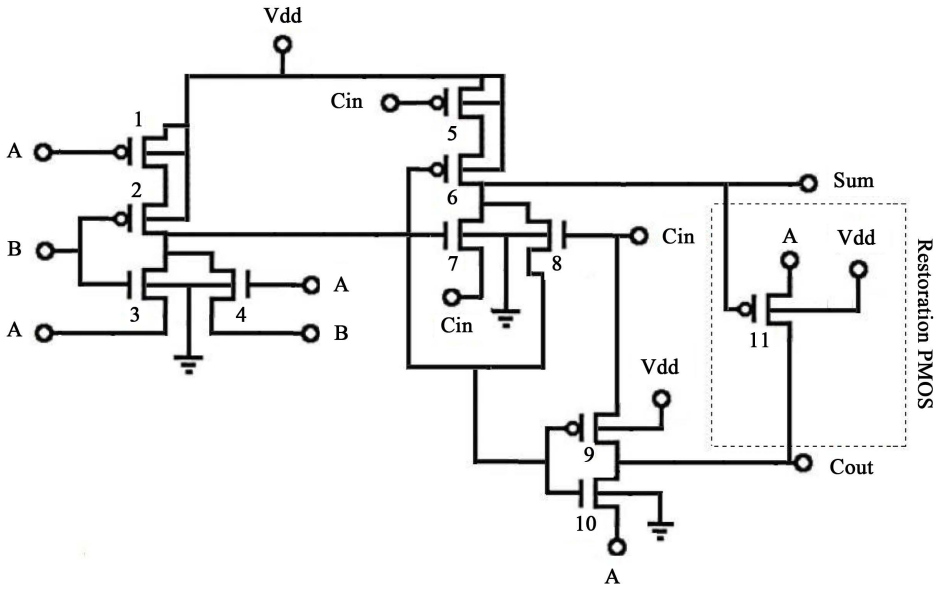


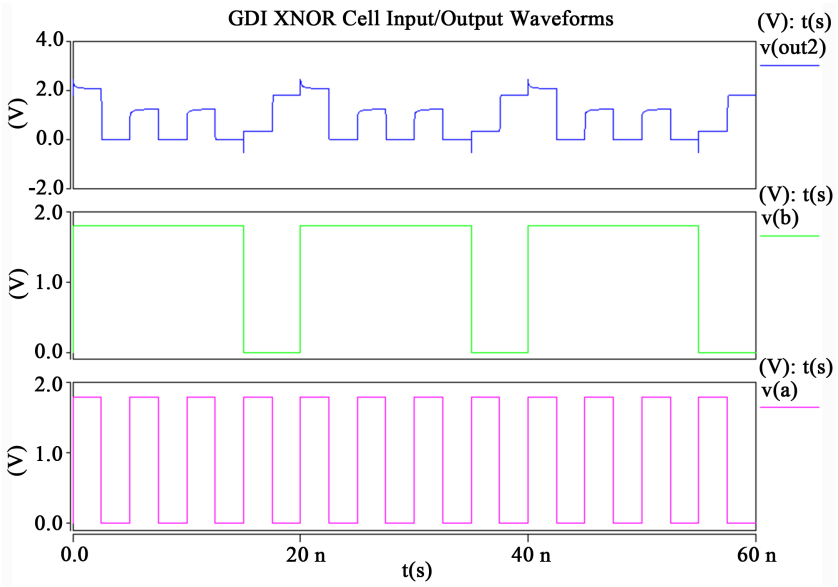
Figure 9. The proposed adder cell.

4. Results and Discussions

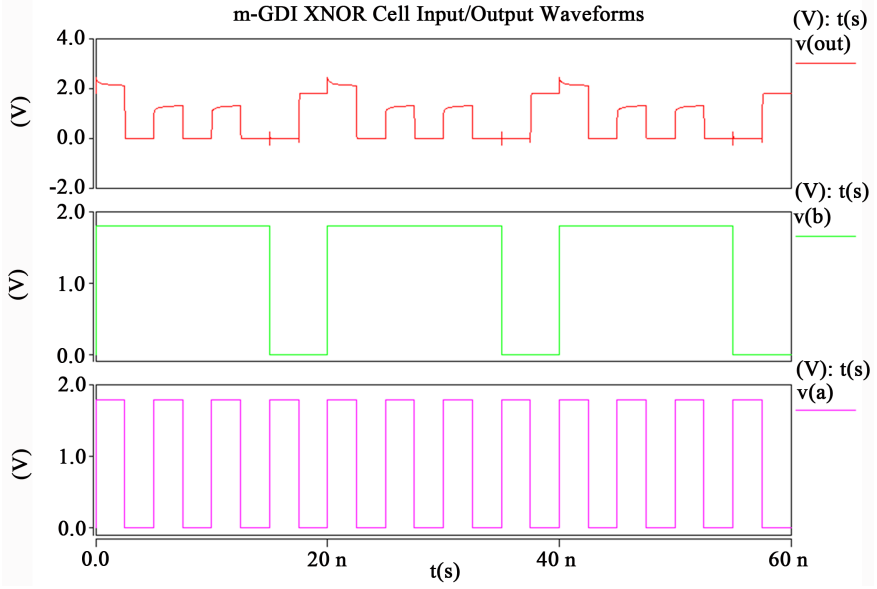
The input/output waveforms of GDI XNOR and m-GDI XNOR cells in 180 nm technology and supply voltage 0f 1.8 v are illustrated in **Figure 10**. The m-GDI XNOR has better swing, lower power consumption and higher speed. **Table 1** indicates lower power consumption and higher speed of m-GDI XNOR cell in comparison with GDI XNOR cell.

The power consumption of the adder cell designed with GDI technology is 12.993 µw, whereas for this cell designed with m-GDI technology is 4.1628 µw (both are designed at 0.18 um technology and shown inputs). HSPICE simulations of two structures are illustrated and compared in **Figure 11**.

The input/output waveform of a m-GDI adder cell, with restoration PMOS, in 90 nm technology is shown in **Figure 12**. **Table 2** indicates average power consumption and rise/fall time of m-GDI adder cell in 90 nm technology.

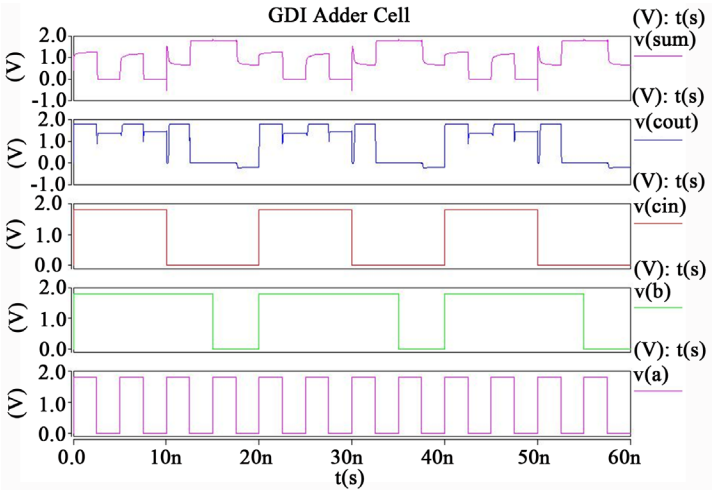


(a)

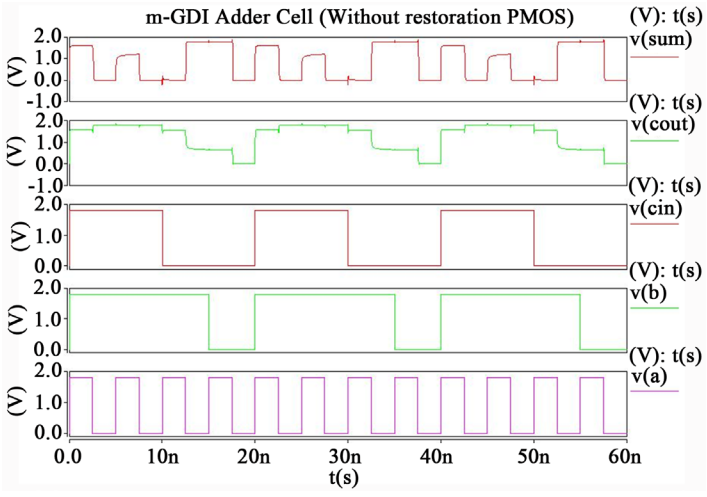


(b)

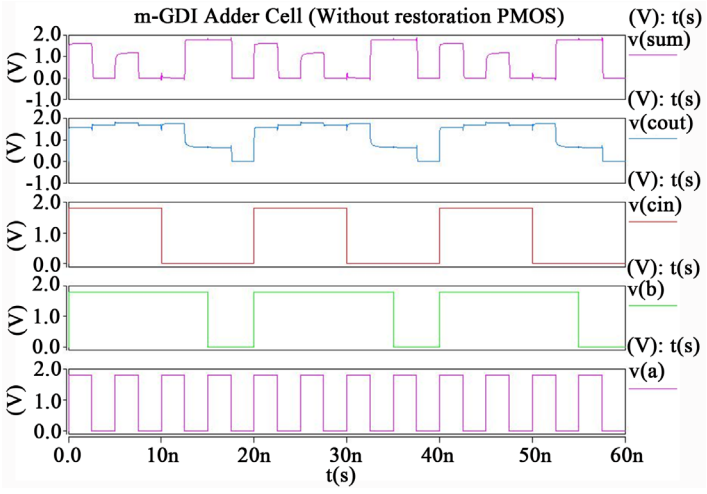
Figure 10. The input/output waveforms of XNOR cells (a) GDI; (b) m-GDI.



(a)

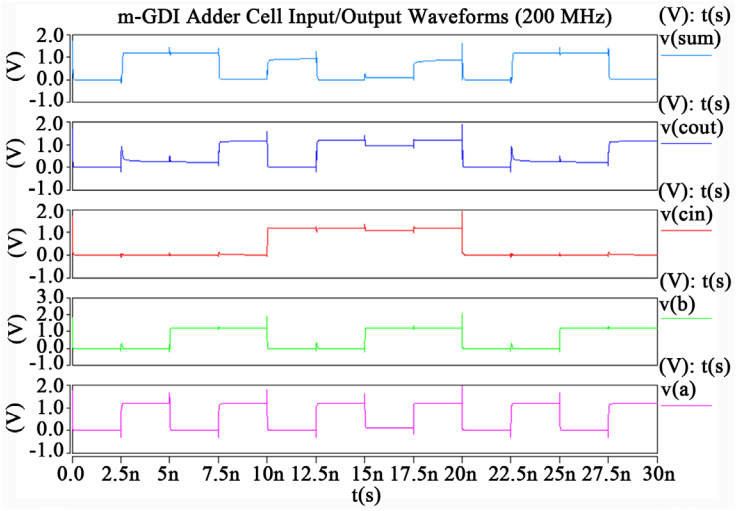


(b)

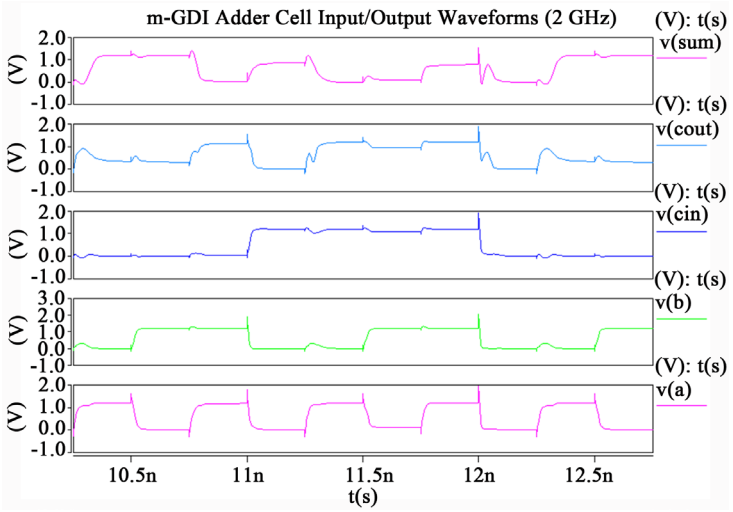


(c)

Figure 11. The input/output waveforms of adder cells (a) GDI XNOR full adder; (b) m-GDI XNOR full adder, without restoration PMOS; (c) m-GDI XNOR full adder, with restoration PMOS.



(a)



(b)

Figure 12. The m-GDI adder cell input/output waveforms in 90 nm technology (a) 200 MHz; (b) 2 GHz.

Table 1. Comparison of GDI and m-GDI power consumption and delay.

XNOR cell	Average power (μw)	Rise time (ps)	Fall time (ps)
m-GDI	1.2796	50	148
GDI	3.9206	74	213

Table 2. Average power consumption and rise/fall time of m-GDI adder cell in 90 nm technology.

Frequency	Average vdd power consumption (μw)	Average inputa power consumption (μw)	Average inputb power consumption (μw)	Average cin power consumption (μw)	Rise time (ps)	Fall time (ps)
200 MHz	0.90262	0.30007	0.17399	0.11401	57	75
2 GHz	6.3222	0.31976	0.19282	0.13620	94	123

5. Conclusion

An ultra-low power adder cell is proposed with cascading two XNOR cells. In this way, we can achieve the sum

of two inputs, regarding to advantages of m-GDI XNOR cell. The simulation results show that the power consumption of the adder cell designed with GDI technology is 12.993 µw, whereas for this cell designed with m-GDI technology is 4.1628 µw at 0.18 µm technology. Also, simulation results show average power consumption of 0.90262 µw and 6.3222 µw in 200 MHz and 2 GHz, respectively for m-GDI adder cell in 90 nm CMOS technology.

Acknowledgements

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