Circuits and Systems, 2016, 7, 1-10
Published Online January 2016 in SciRes. http://www.scirp.org/journal/cs
http://dx.doi.org/10.4236/cs.2016.71001

Design of Low-Voltage, Low-Power FGMOS Based Voltage Buffer, Analog Inverter and Winner-Take-All Analog Signal Processing Circuits

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Received 1 December 2015; accepted 10 January 2016; published 13 January 2016

Abstract

This paper proposes novel floating-gate MOSFET (FGMOS) based Voltage Buffer, Analog Inverter and Winner-Take-All (WTA) circuits. The proposed circuits have low power dissipation. All proposed circuits are simulated using SPICE in 180 nm CMOS technology with supply voltages of ±1.25 V. The simulation results demonstrate increase in input range for FGMOS based voltage buffer and analog inverter and maximum power dissipation of 0.5 mW, 1.9 mW and 0.429 mW for FGMOS based voltage buffer, analog inverter and WTA circuits, respectively. The proposed circuits are intended to find applications in low voltage, low power consumer electronics.

Keywords

FGMOS, Voltage Buffer, Analog Inverter, Winner-Take-All (WTA), Analog Signal Processing Circuits

1. Introduction

Current trends in consumer electronics strive to achieve low-voltage and low-power circuit designs of voltage buffer, analog inverter and WTA having utility in portable electronics. Floating Gate MOS technology is a low voltage design technique with its attractive features such as reduced circuit complexity and simplified signal

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How to cite this paper: Suchitta, A., Srivastava, R., Dewaker, A. and Gupta, M. (2016) Design of Low-Voltage, Low-Power FGMOS Based Voltage Buffer, Analog Inverter and Winner-Take-All Analog Signal Processing Circuits. *Circuits and Systems*, **7**, 1-10. http://dx.doi.org/10.4236/cs.2016.71001

processing chain of a design. It is capable of shifting the signal levels and incorporating tunable mechanisms due to its programmable threshold voltage. It operates normally below the operational limits of supply voltage levels for a particular technology and thus consumes less power than the minimum power required for a CMOS circuit of same technology without compromising on device performance [1]. Applications of FGMOS transistors in neural networks [2], voltage-controlled resistors [3], electronic programming [4], current mirrors [5], digital-to-analog and analog-to-digital converters [6], multipliers [7], squarers [8], operational transconductance amplifier [9], etc. have been reported. Exclusive features such as flexibility, controllability and tenability of FGMOS that yield better results in terms of power supply voltage motivated us to propose FGMOS based Voltage Buffer, Analog Inverter and WTA.

Voltage buffer circuit implemented using CMOS technology has been reported in literature extensively. However, some FGMOS based voltage buffers have also been reported, to refer some of them, K. Moolpho and J. Ngarmnil [10] have proposed low voltage FGMOS based class AB buffer error amplifier comprising of three main building blocks in which one of the blocks is the two input gate additive inverter using FGMOS devices and Gupta M. *et al.* [11] have presented improved FGMOS based low power voltage follower circuit. In this paper, we have implemented a new FGMOS based voltage buffer circuit which dissipates less power.

Implementation of FGMOS inverter to generate the nonlinear functions has been proposed by Trejo-Guerra, R. *et al.* [12]. Performance related properties such as power, delay, power-delay product (PDP), and energy-delay product (EDP) of FGMOS inverter operating in subthreshold region are investigated in [13]. Differential Floating Gate analog inverter has been reported in [14]. Here, we propose an FGMOS based differential difference voltage buffer (FGDDVB) circuit based on the well-established and versatile Differential Difference Amplifier (DDA) circuit topology.

WTA networks are an important class of circuits widely used in neural networks and pattern-recognition systems [15]. Not much work has been published on FGMOS based WTA circuit. A novel FGMOS based Winner-Take-All (WTA) circuit with reduced power dissipation is presented.

Thus, in summary, this paper introduces FGMOS based analog signal processing circuits—voltage buffer, analog inverter and winner-take-all. Simulated results are provided to demonstrate reduced power dissipation and an increase in the input range due to the use of floating gate transistors.

The paper is organized as follows. The operation of FGMOS transistor is described in Section 2. Proposed FGMOS based voltage buffer, analog inverter and WTA circuits are presented in Section 3. Simulation results are discussed in Section 4 to verify theoretical results. Finally, conclusions are drawn in the last section.

2. Basics of FGMOS Transistor

FGMOS transistor has multiple inputs whose gate is subject to capacitive couplings between itself and input terminals. Threshold voltage of the transistor is tuned by capacitor values and applied bias voltage. **Figure 1** shows equivalent representation of FGMOS transistor [1].

The input signals $(V_1, V_2, \cdots, V_N)$ are applied at floating gates $G_1, G_2, \cdots, G_N$ of FGMOS transistor, respectively. The voltage on floating gate V_{FG} is given as [1] $V_{FG} = \sum_{i=1}^{N} \frac{C_i}{C_T} V_i + \frac{C_{GS}}{C_T} V_S + \frac{C_{GD}}{C_T} V_D + \frac{Q_{FG}}{C_T}$

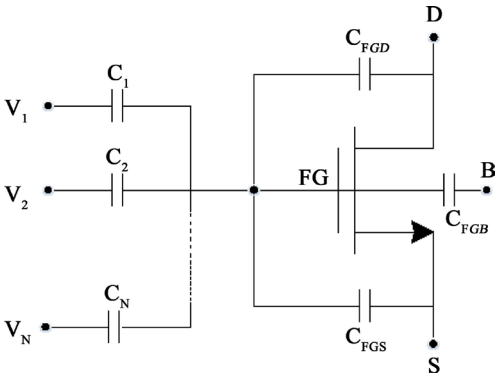

Figure 1. Equivalent representation of FGMOS.

where C_i is the set of capacitors associated with effective inputs and the floating gate. Total floating gate capacitance is given by $C_T = \sum_{i=1}^{N} C_i + C_{FGS} + C_{FGD} + C_{FGB}$ where C_{FGD}, C_{FGS} and C_{FGB} are overlap capacitances of floating gate with drain, source and bulk, respectively, V_D is the drain voltage, V_S is the source voltage, V_B is the bulk voltage, and Q_{FG} is the residual charge trapped in the oxide-silicon interface during fabrication process. By the justification suggested in [8], neglecting residual charge, Q_{FG} and assuming $C_i \gg C_{FGD}$, C_{FGB} [1], the drain current of FGMOS transistor in saturation region can be expressed as

$$I_D = \frac{\beta}{2}\left(\sum_{i=1}^{N} K_i V_{iS} - V_T\right)^2$$

where $k_i = C_i/C_T$, β is the transconductance, V_T is the threshold voltage.

3. Circuit Descriptions

3.1. Proposed FGMOS Voltage Buffer

Analog voltage buffers play a significant role in mixed signal designs where they are used for signal monitoring and for driving large capacitive loads [16]. Voltage buffer with floating gate transistors has been implemented with modifications being made to the circuit of voltage buffer implemented using CMOS whose structure is similar to differential difference amplifier [17], published in [18].

The proposed FGMOS circuit is obtained by replacing the matched differential stage (M_1 and M_2), by two input floating gate transistors. The configuration is similar to DDA realization, but the first and second inputs are removed; hence the third input and output become a voltage follower building block. The complete FGMOS voltage buffer is shown in **Figure 2**. PMOS transistors operate in saturation region described by the following equation:

$$I_{DP} = k_P\left(V_{SGP} - |V_{TP}|\right)^2$$

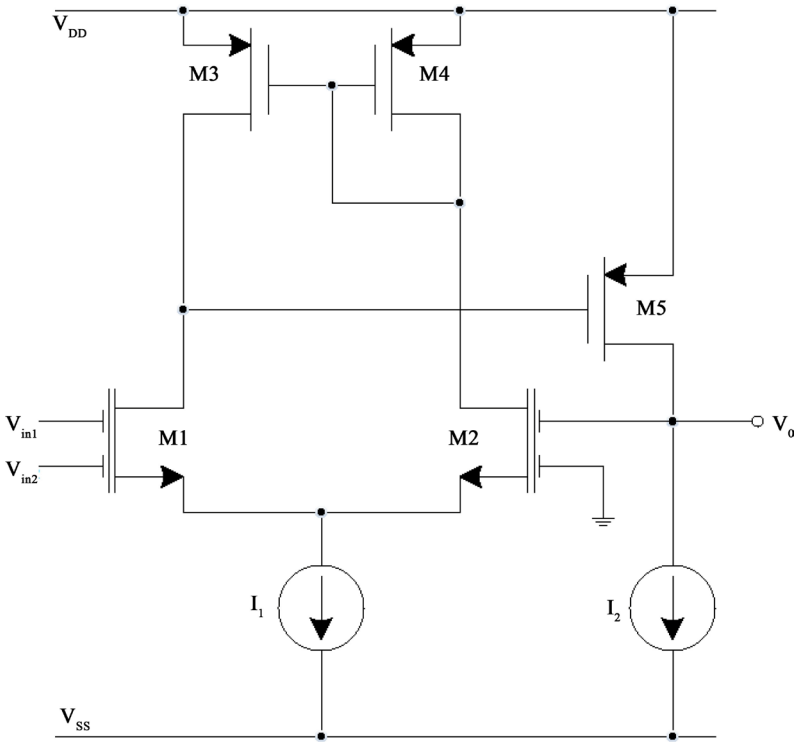

Figure 2. FGMOS based voltage buffer.

where $k_P = (\mu_P C_{OX}/2)(W/L)$, V_{TP} is threshold voltage, μ_P is surface mobility, C_{OX} is channel oxide capacitance, W is channel width and L is channel length of the transistor. M_1 and M_2 operate in saturation region and their drain currents can hence be written as:

$$I_{D1} = \frac{\beta}{2}\left(V_{in1S}K_1 + V_{in2S}K_2 - V_T\right)^2$$

$$I_{D2} = \frac{\beta}{2}\left(V_{0S}K_1 + \left(-V_S\right)K_2 - V_T\right)^2$$

With current mirrors M_3 and M_4 perfectly matched, $I_{D1} = I_{D2}$.

$$\frac{\beta}{2}\left(V_{in1S}K_1 + V_{in2S}K_2 - V_T\right)^2 = \frac{\beta}{2}\left(V_{0S}K_1 + \left(-V_S\right)K_2 - V_T\right)^2$$

Cancelling the common terms gives,

$$\Rightarrow V_0K_1 = V_{in1}K_1 + V_{in2}K_2$$

$$\Rightarrow V_0 = V_{in1} + V_{in2}\frac{K_2}{K_1}$$

If V_{in2} is zero, then $V_0 = V_{in1}$, *i.e.*, the output follows the input, thus the circuit operates as a voltage buffer.

3.2. Proposed FGMOS Analog Inverter

Differential difference voltage buffer (DDVB) [19] basically consists of two voltage buffers which invert the input to the first buffer from the input to the second buffer, hence acts as an analog inverter. CMOS implementation of DDVB has been presented in [17].

Proposed FGMOS analog inverter is obtained by replacing MOSFETs M1, M2, M3 and M4 in DDVB circuit [19] by two input floating gate transistors which results in circuit of **Figure 3**. All p-type and n-type MOSFETs as well as floating gate transistors in the proposed circuit operate in saturation region.

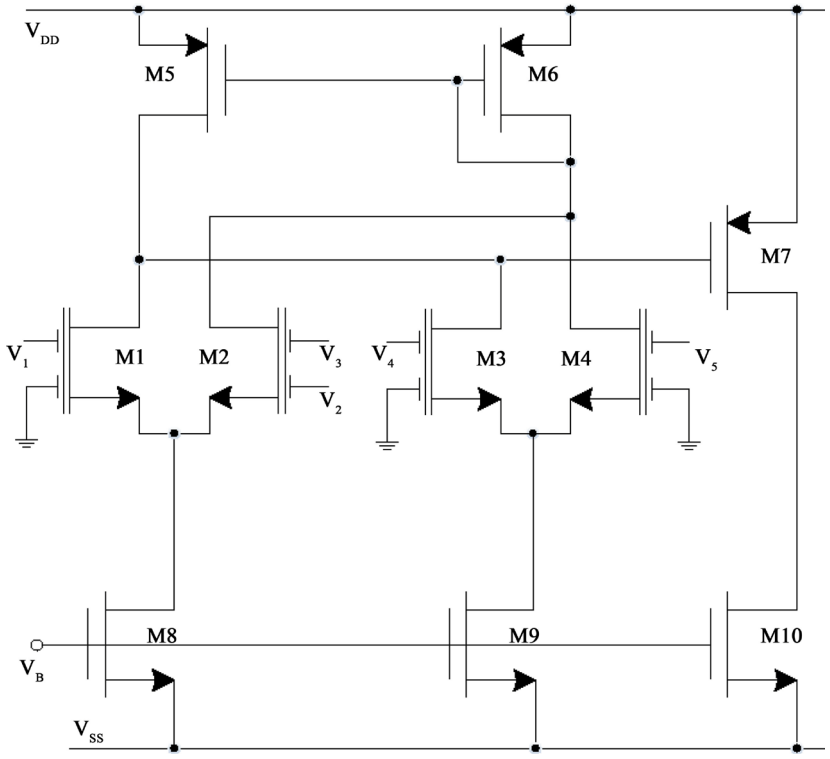

Figure 3. FGMOS based analog inverter.

3.3. Proposed FGMOS Based WTA Circuit

The proposed n-input FGMOS WTA maximum circuit as indicated in **Figure 4** is drawn on similar lines as CMOS WTA max circuit published in [18]. All MOSFETs and floating gate transistors operate in strong inversion saturation region with $V_{GS} > V_T$. The operating principle remains the same.

4. Simulation Results

The conventional and proposed FGMOS based analog signal processing circuits are simulated using SPICE (Pspice version 16.5) in CMOS 180 nm technology. Rail-to-rail input range is assumed and a supply voltage of ±1.25 V is taken for simulating both circuits. The aspect ratios of the transistors of the conventional circuits and proposed circuits are listed in **Table 1**. The performance parameters of the proposed circuits and their corresponding conventional circuits are compared in **Table 2**. To overcome DC convergence error during simulation because of the floating gate (FG) of FGMOS, model suggested in [1] has been used in all proposed FGMOS based circuits. In this model, very high value resistors (R_G) are connected in between the FG node and a set of voltage sources.

DC response of CMOS voltage buffer and FGMOS based voltage buffer is shown in **Figure 5**. Proposed FGMOS voltage buffer was implemented with two inputs to floating gate MOSFET M1. Output was observed at one of the inputs to M2, with input to the MOSFET being grounded. It can be seen from the DC analysis that the operating (linearity) range increases in case of FGMOS voltage buffer compared to CMOS voltage buffer. While it can be observed from simulation that the proposed FGMOS based voltage buffer justifies its operation in the entire supply voltage range, *i.e.*, from −1.25 V to 1.25 V, CMOS based voltage buffer operates as a buffer in the voltage range from−1.25 V to 1 V. This is evident due to the fact that the effective input signal at the floating gate is scaled down by equivalent capacitance ratio (C_i/C_T), which results into a lower distortion and hence a larger input range is achieved. Frequency response of conventional and proposed voltage buffer is shown in **Figure 6**. DC response for CMOS analog inverter and the proposed FGDDVB are shown in **Figure 7**. Simulation results reveal that power dissipation reduces drastically for the proposed FGDDVB. The linearity range has increased for the proposed FGDDVB (0 to 1 V) compared to the conventional CMOS based analog inverter (0 to 0.9 V). Frequency response of conventional and proposed analog inverter are shown in **Figure 8**. It

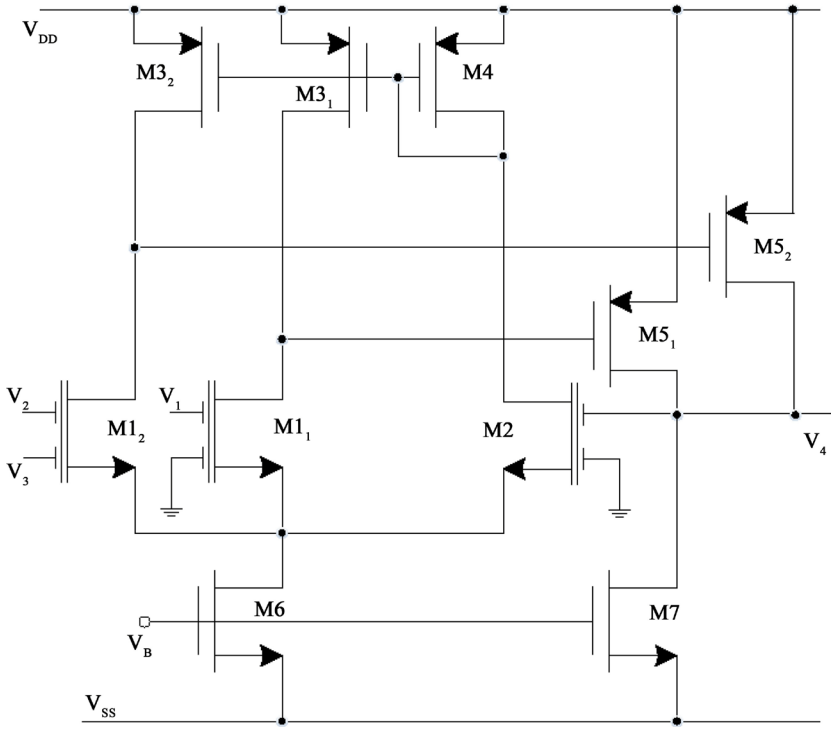

Figure 4. FGMOS based WTA circuit.

Table 1. Aspect ratio values (a) conventional CMOS buffer and proposed FGMOS voltage buffer; (b) conventional DDVB (analog inverter) circuit using CMOS; (c) proposed FGDDVB circuit; (d) conventional WTA using CMOS and proposed FGMOS based WTA.

(a)

Transistor	W (μm)	L (μm)
M1 - M2	1	0.25
M3 - M5	5	0.25

(b)

Transistor	W (μm)	L (μm)
M1 - M4	1	0.25
M5 - M7	5	0.25
M8 - M10	3	0.25

(c)

Transistor	W (μm)	L (μm)
M1 - M2	1	0.25
M3 - M4	3	0.25
M5 - M7	5	0.25
M8 - M10	3	0.25

(d)

Transistor	W (μm)	L (μm)
M11 - M12	1	0.25
M2	1	0.25
M31 - M32	5	0.25
M51 - M52	5	0.25
M6 - M7	3	0.25

Table 2. Comparison of conventional and proposed circuits.

Parameters	Experimental results					
	Voltage buffer		Analog inverter		WTA	
	CMOS	FGMOS	CMOS	FGMOS	CMOS	FGMOS
Process technology	180 nm	180 nm	180 nm	180 nm	180 nm	180 nm
V_{DD} & V_{SS}	±1.25 V	±1.25 V	±1.45 V	±1.25 V	±1.25 V	±1.25 V
Linearity range	−1.25 V to 1 V	−1.25 V to 1.25 V	0 to 0.9 V	0 to 1 V	-	-
Gain	0.9670	0.9962	−0.9653	−1.005	-	-
Power dissipation (mW)	0.500	0.500	13	1.900	1.450	0.429
Input resistance (Ω)	10^{20}	2×10^{11}	10^{20}	2×10^{11}	10^{20}	2×10^{11}
Output resistance (kΩ)	1.584	0.193	0.259	3.436	0.097	1.696

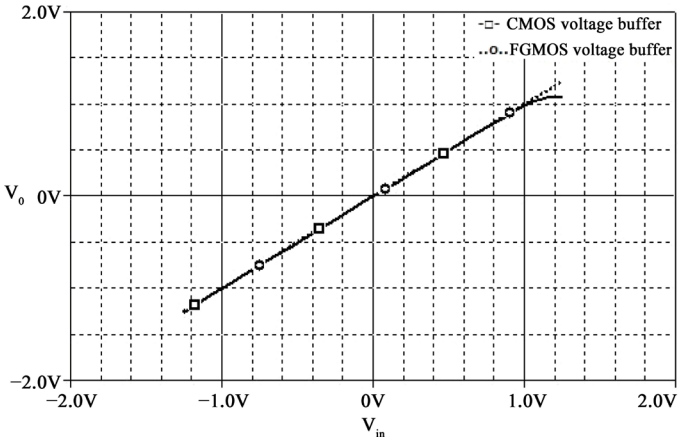

Figure 5. DC response of conventional CMOS and proposed FGMOS based voltage buffer.

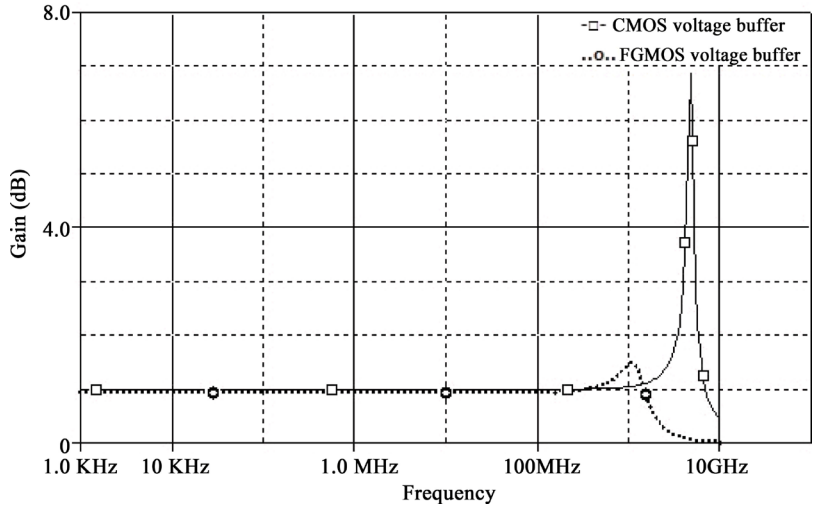

Figure 6. AC response of conventional CMOS and proposed FGMOS based voltage buffer.

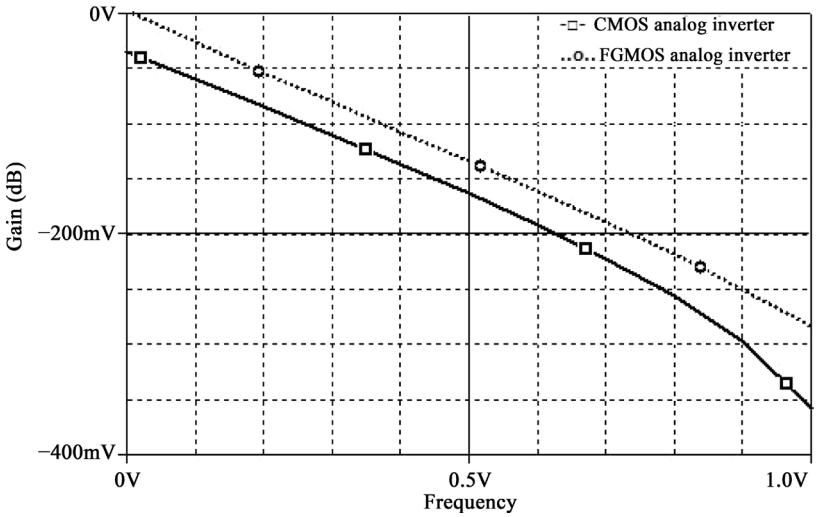

Figure 7. DC response of conventional CMOS and proposed FGMOS based DDVB.

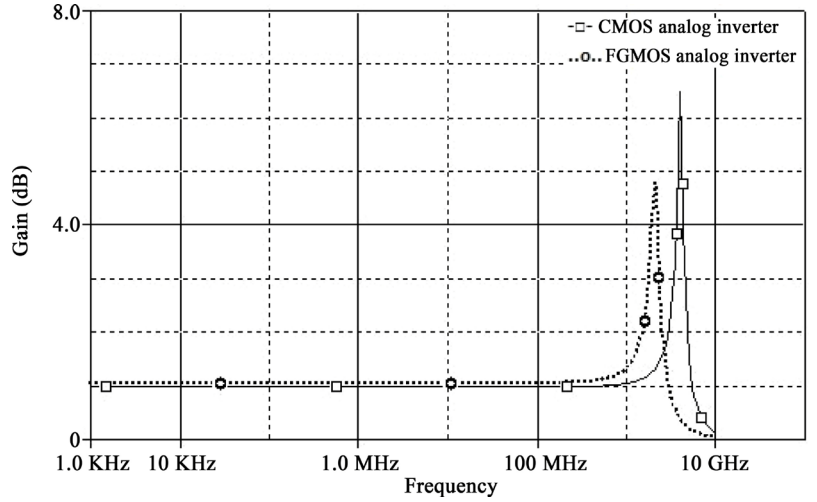

Figure 8. AC response of conventional CMOS and proposed FGMOS based DDVB.

can also be seen that the proposed configuration operates at lower supply voltage compared to the conventional DDVB. DC response and frequency response of CMOS WTA and the proposed FGMOS based WTA are shown in **Figure 9** and **Figure 10** respectively. From the simulation results it can again be observed that power dissipa-

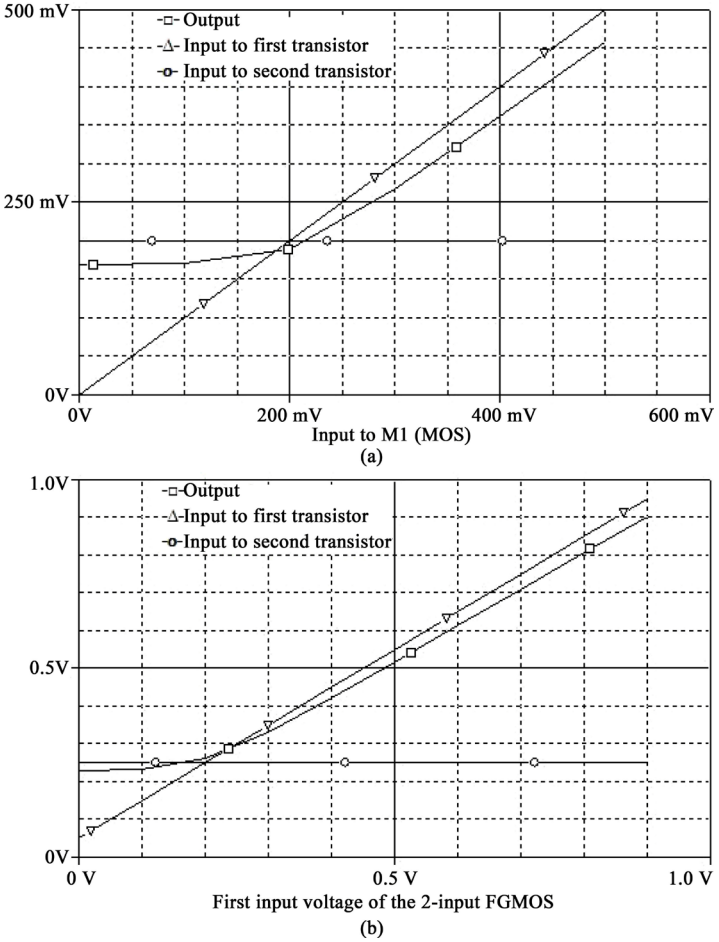

Figure 9. (a) DC response of conventional CMOS WTA; (b) DC response of proposed FGMOS WTA.

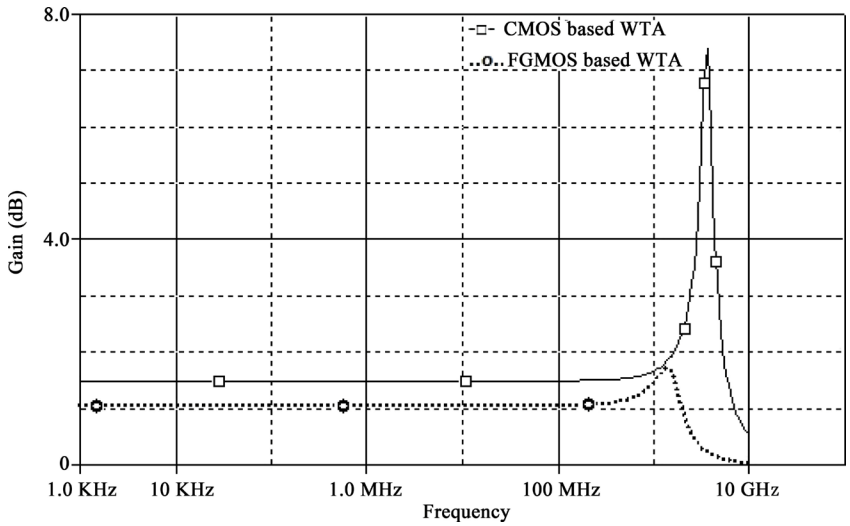

Figure 10. AC response of conventional CMOS and proposed FGMOS based WTA.

tion is reduced for proposed WTA circuit. In general, for all the proposed FGMOS based analog signal processing circuits, power dissipation is reduced compared to the conventional circuits proposed earlier.

5. Conclusion

In this paper, novel FGMOS based analog signal processing circuits—voltage buffer, analog inverter and winner-take-all circuits are presented. All proposed circuits operate at ±1.25 V. A larger operating range is achieved for FGMOS based voltage buffer and FGMOS based analog inverter compared to their corresponding conventional circuits, as desired. Power dissipation is reduced in all the proposed FGMOS based circuits, thus making these circuits useful in low-voltage and low-power applications. The proposed circuits are intended to find applications in low voltage, low power consumer electronics.

Acknowledgements

The work was carried out at Netaji Subhas Institute of Technology, New Delhi (University of Delhi) as a partial fulfillment of engineering degree.

References

[1] Rodriguez-Villegas, E. (2006) Low Power and Low Voltage Circuit Design with the FGMOS Transistor (IET Circuits, Devices and Systems Series 20). The Institution of Engineering and Technology, London.

[2] Kumar, M.G.L., Khare, K. and Sharma, P. (2012) Low Voltage-Power-Area FGMOS Neural Classifier Circuit for VLSI Analog BIST. *International Journal of Engineering Research & Technology*, **1**, 1-4.

[3] Pandey, R. and Gupta, M. (2010) FGMOS Based Voltage-Controlled Grounded Resistor. *Radioengineering*, **19**, 455-459.

[4] Berg, Y. and Lande, T.S. (1997) Programmable Floating Gate MOS Logic for Low-Power Operation. *Proceedings of IEEE International Symposium on Circuits and Systems*, **3**, 1792-1795. http://dx.doi.org/10.1109/iscas.1997.621493

[5] Manhas, P.S., Sharma, S., Pal, K., Mangotra, L.K. and Jamwal, K.S. (2008) High Performance FGMOS-Based Low Voltage Current Mirror. *Indian Journal of Pure & Applied Physics*, **46**, 355-358.

[6] Liming, Y., Embadi, S.H.K. and Sanchez-Sinencio, E. (1997) A Floating Gate MOSFET D/A Converter. *Proceedings of IEEE International Symposium on Circuits and Systems*, **1**, 409-412. http://dx.doi.org/10.1109/iscas.1997.608754

[7] Srivastava, R., Gupta, M. and Singh, U. (2014) Low Voltage Floating Gate MOS Transistor Based Four Quadrant Multiplier. *Radioengineering*, **23**, 1150-1160.

[8] Gupta, M., Srivastava, R. and Singh, U. (2014) Low Voltage Floating Gate MOS Transistor Based Differential Voltage Squarer. *ISRN Electronics*, **2014**, Article ID: 357184.

[9] Ramirez-Angulo, J., Choi, S.C. and Altamirano, G.G. (1995) Low Voltage Circuits Building Blocks Using Multiple Input Floating Gate Transistors. *IEEE Transactions on Circuits and Systems - I*, **42**, 971-974. http://dx.doi.org/10.1109/81.477210

[10] Moolpho, K. and Ngarmnil, J. (2006) Low Voltage High-Performance Class-AB FGMOS Buffer. *IEEE Asia Pacific Conference on Circuits and Systems*, Singapore, 4-7 December 2006, 1779-1782. http://dx.doi.org/10.1109/apccas.2006.342163

[11] Gupta, M., Singh, U. and Srivastava, R. (2013) High-Frequency and Low-Power Output Stages Based on FGMOS Flipped Voltage Follower. *ISRN Electronics*, **2013**, Article ID: 914058.

[12] Trejo-Guerra, R., Tlelo-Cuautle, E., Jimenez-Fuentes, M. and Sánchez-López, C. (2010) Multiscroll Oscillator Based on Floating Gate CMOS Inverter. *7th International Conference on Electrical Engineering Computing Science and Automatic Control* (*CCE*), Tuxtla Gutierrez, 8-10 September 2010, 541-545. http://dx.doi.org/10.1109/iceee.2010.5608587

[13] Alfredsson, J., Aunet, S. and Oelmann, B. (2005) Basic Speed and Power Properties of Digital Floating-Gate Circuits Operating in Subthreshold. *Proceedings of IFIP VLSI-SOC* 2005, 229-232.

[14] Berg, Y., Aunet, S., Ness, O. and Hovin, M. (2001) Floating-Gate CMOS Differential Analog Inverter for Ultra Low-Voltage Applications. *IEEE International Symposium on Circuits and Systems*, **1**, 9-12. http://dx.doi.org/10.1109/iscas.2001.921775

[15] Shen, J., Zhang, Y.X. and Mu, G. (1993) Optical Pattern Recognition System Based on a Winner-Take-All Model of a Neural Network. *Optical Engineering*, **32**, 1053-1056. http://dx.doi.org/10.1117/12.61200

[16] Carrillo, J.M., Duque-Carrillo, J.F., Torralba, A. and Carvajal, R.G. (2005) Class-AB Rail-to-Rail CMOS Analog Buf-

fer. *IEEE International Symposium on Circuits and Systems*, **2**, 1008-1011. http://dx.doi.org/10.1109/iscas.2005.1464761

[17] Sackinger, E. and Guggenbuhl, W. (1987) A Versatile Building Block: The CMOS Differential Difference Amplifier. *IEEE Journal of Solid-State Circuits*, **22**, 287-294. http://dx.doi.org/10.1109/JSSC.1987.1052715

[18] Prommee, P. and Chattrakun, K. (2011) CMOS WTA Maximum and Minimum Circuits with Their Applications to Analog Switch and Rectifiers. *Microelectronics Journal*, **42**, 52-62. http://dx.doi.org/10.1016/j.mejo.2010.09.004

[19] Chiu, W., Liu, S.I., Tsao, H.W. and Chen, J.J. (1996) CMOS Differential Difference Current Conveyors and Their Applications. *IEE Proceedings on Circuits Devices and Systems*, **143**, 91-96. http://dx.doi.org/10.1049/ip-cds:19960223