Circuits and Systems, 2015, 6, 121-135
Published Online May 2015 in SciRes. http://www.scirp.org/journal/cs
http://dx.doi.org/10.4236/cs.2015.65013

Scientific Research Publishing

Reliability of High Speed Ultra Low Voltage Differential CMOS Logic

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Received 26 March 2015; accepted 19 May 2015; published 22 May 2015

Abstract

In this paper, we present a solution to the ultra low voltage inverter by adding a keeper transistor in order to make the semi-floating-gate more stable and to reduce the current dissipation. Moreover, we also present a differential ULV inverter and elaborate on the reliability and fault tolerance of the gate. The differential ULV gate compared to both a former ULV gate and standard CMOS are given. The results are obtained through Monte-Carlo simulations.

Keywords

CMOS, Differential, Floating-Gate, Semi-Floating-Gate, Keeper, Recharge, Ultra Low Voltage, High Speed, Monte-Carlo, Cadence, STM, 90 nm

1. Introduction

In the last decade, sophisticated portable electronics has dramatically increased in the consumer market. The new trends are toward energy harvesting electronics and drive the need for low power and low voltage due to a limited budget of processed energy, while on the other hand demand for high-performance electronics regarding speed. Thus, in the last decade, major developments have made low power designs a key objective in addition to speed and silicon area, in order to lower the energy consumption several approaches exists. One of the most fundamental and effective approach is to lower the supply-voltage [1] [2]. Furthermore, it is called ultra low voltage (ULV) when the supply voltage is reduced to hundreds of milli-volts [3] [4]. However, the scaling of the supply-voltage has the adverse effect on the performance of the design concerning speed. The main challenge is to obtain high speed at as low as possible supply-voltages. To maintain good evaluation response time at ultra low supply-voltages, the threshold voltages of the transistors must also be reduced. Unfortunately, this requires a change in the CMOS fabrication process. Multiple-technique has been proposed for low voltage high perfor-

How to cite this paper: Mirmotahari, O. and Berg, Y. (2015) Reliability of High Speed Ultra Low Voltage Differential CMOS Logic. *Circuits and Systems*, **6**, 121-135. http://dx.doi.org/10.4236/cs.2015.65013

mance circuits designs [5] without changing the fabrication process. Floating-gates (FG) have also been proposed for ultra low voltage and low power (LP) logic [6]. Unfortunately, modern processes face significant gate leakage due to the thin oxide. A ULV floating-gate inverter employing a frequent recharge technique has shown good properties in achieving high speed at ultra low voltages [7]. Even though the ULV gate has shown good performance, it also has limitations due to the leakage at the semi-floating-gates (SFG). A differential ULV gate has been proposed by including a keeper function [8] which is argued to have the speed of an ULV but the stability as a standard CMOS.

In this paper, the differential ULV inverter is presented. The improvement in term of stability and delay relative to the ULV is elaborated. Furthermore, the reliability, yield and the defect tolerance of the differential ULV inverter compared with both standards CMOS and with ULV floating-gate inverter are examined. The main goal is to find the designs behaviour and pinpoint the adjustment parameter giving the best yield and fault tolerance.

The outline of this paper is as follows. In Section 1, key aspects of the ultra low voltage (ULV) gate are presented. Section 3 elaborates on the leakage problem of the ULV gates and presents a solution with keeper functionality. In Section 4, a differential ULV gate including the keeper function is thoroughly presented and the key advantages are pointed out. Section 5 presents the aspects of reliability such as speed, stability and noise-margin of the differential ULV both compared with CMOS and with ULV floating-gate inverter. And in Section 5, a discussion on the achieved results is given. Finally, the paper concludes by pointing out the optimal design parameters. The simulation results demonstrated throughout this paper were obtained by simulation produced in a STM 90 nm process environment provided by Cadence.

2. Ultra Low Voltage Floating-Gate Inverter

A ultra low voltage (ULV) inverter were first introduced in [7] and is shown in **Figure 1**. The inverter has been demonstrated with measurements for supply voltage of 0.4 V. Moreover, its potential has been simulated to be more than ten times the operating frequency than compared footed domino logic gates resulting in a improved EDP of 20 times better than standard inverter. Further comparisons to CMOS have been elaborated in [9], which also strengthen the ULV inverters potential. Furthermore, this gate has been used in the field of power analysis

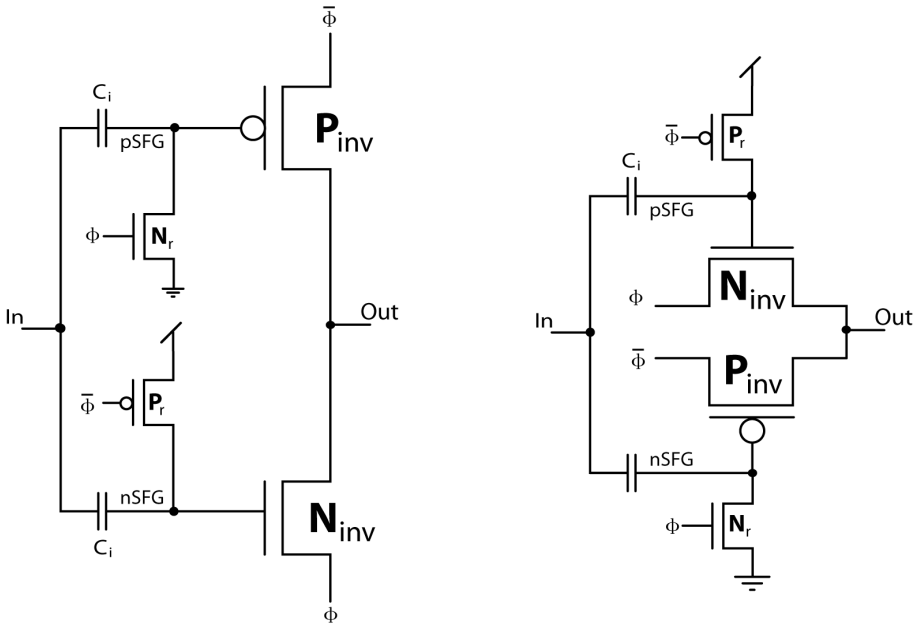

Figure 1. The figure illustrates the ultra low voltage gate. Both designs are logically and electrically equivalent. In (a) the design clearly shows the inverter and the biasing/recharging of the floating-gate, while (b) is designed to emphasise that the output is not directly connected to the supply voltage. (a) ULV design resembles a UV-floating-gate inverter; (b) ULV design with focus on the output regarding to supply-voltage.

and it has been found to be able to camouflage its instantaneous current dissipation due to the clock drivers [10]. Extracting the joint advantages of this particular ULV gate, we find the combination of high speed and low voltage giving quite good EDP numbers than other known similar logic, such as CMOS and footed domino logic. Although, the ULV inverter is presented here, there are published work on other logical gates, such as NAND and NOR [9].

In general, all floating-gates suffer from leakage, some to more extent than other. It is a well-known phenomenon in the field of floating-gate that a frequent recharging strategy includes elements which would increase the leakage. The presented ULV gates are classified as semi-floating-gate (SFG) because of the direct connected recharge transistor. The leakage through the drain contact of the recharge transistor will set restrictions for the operating frequency both in terms of high cut-off and low cut-off. The leakage of the semi-floating-gate would also affect the inverters ability to reach the rails. Simulation results demonstrating the leakage as a function of the supply-voltage is given in **Figure 2** and a corresponding deviation from the rails in **Figure 3**. With these two simulation result the lowest operating frequency can be calculated by the formula:

$$f_{low} = \frac{leakage}{NM - deviation} \tag{1}$$

where *deviation* represents the amount of voltage deviation from the rails, *NM* represents the noise margin (typically 25% of V_{dd}) and *leakage* is the amount given in μV/ns.

3. Keeper Function

In order to face the problem with stability and leakage at the semi-floating-gate, that is to be able to reach the rails, a design solution is given in **Figure 4**. The inspiration may be claimed from the keeper function in domino logic. The additional transistors, labelled N_k and P_k, will at given time keep the charge on the semi floating-gate to a fixed potential. The behaviour during evaluation for a falling transition is given below:

- PER The semi floating-gates, nSFG and pSFG, are set to V_{dd} and Gnd, respectively. The recharge clock, ϕ, is turning off. The input signal, In, is at $V_{dd}/2$ and Out is $V_{dd}/2$.

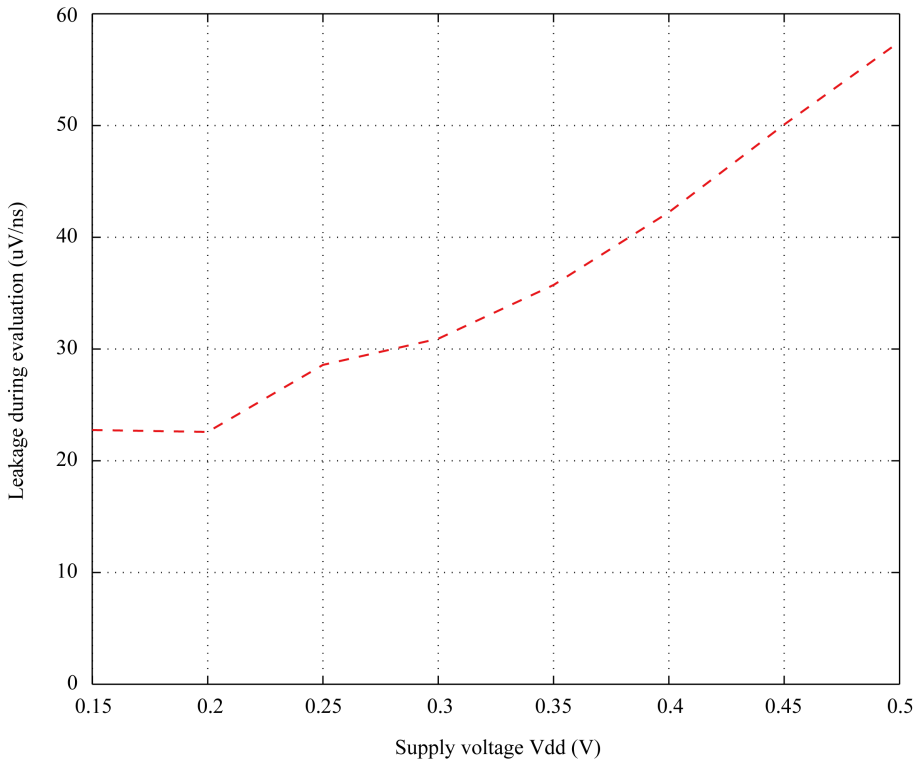

Figure 2. Simulation results show the leakage of the ULV gate during an evaluation period as a function of low supply-voltages. The leakage is given by μV/ns.

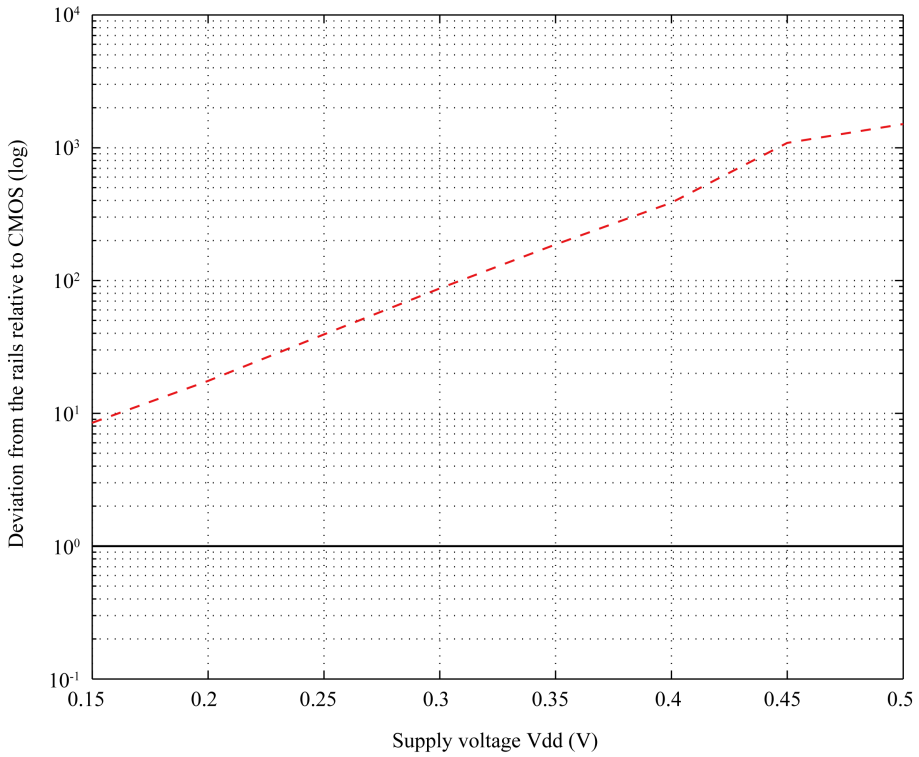

Figure 3. Simulation results demonstrating the amount of deviation relative to CMOS under given supply-voltages. This behaviour is expected due to the leakage through the diffusion contact of the recharge transistor.

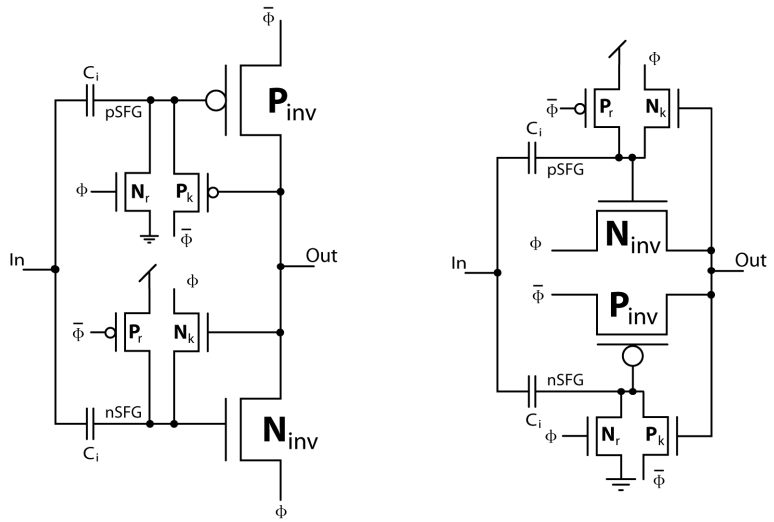

Figure 4. The ultra low voltage gate is modified by including a transistor which acts as an keeper. The keeper transistors are label N_k and P_k and would contribute to hold the semi- floating-gates potential, thus eliminating the leakage.

- DUR In starts on a falling transition. nSFG and pSFG see this change with an attenuation factor of C_i/C_{tot}, where C_{tot} is the total capacitance seen from the semi floating-gate. The output drivers, P_{inv} and N_{inv}, starts pulling the output node up. While evaluating, the semi floating-gates are leaking, for nSFG the leakage is from $(V_{dd} - \Delta V)$ to Gnd, while for pMOS it is (Gnd $- \Delta V$) to Gnd. The voltage change ΔV is as result of the transition at the input.

- POST When In has reached its rail (Gnd), the output drivers are still evaluating the change and try to pull up the output to the rail (V_{dd}). It is here the keeper steps in and holds the nSFG to Gnd and makes sure that the output is as close to the rail as possible and hold the value until next recharge period. Note that the N_k is active and not P_k, due to the falling transition.

Simulation results also verify the theoretical approach and further states the improved stability and lower the leakage due to the included keeper function. Nevertheless, experience with semi floating-gates show that designs with a logical depth of 2 or more, some problems concerning signal delay and clock synchronisation occurs. In that particular case it can actually in worst-case scenario lead to a lock down for the gate. The worst- case in a design, with a logical depth of 2 or more, is where one of the gates output, due to some unexpected reason, is shifted away from $V_{dd} = 2$. Even a small voltage change from $V_{dd} = 2$ at the output would lead to a lock down to either rails. The lock-down can be avoided if the keeper transistors are not connected to the same reference as the recharge. One very interesting gate to examine in more details are a differential design of the ULV gate with keeper. A differential ULV gate has not, to our knowledge, been published.

4. Differential ULV Inverter with Keeper

In a differential ULV gate, the keeper really gets to be used for more than its potential. The benefit of having the keeper is gained both through keeping a fixed potential for the semi floating-gate and to actually turn "more" off those transistors which should be off. The main benefit for having a differential design is that the opposite output signal is accessible and thus can be connected to the keeper transistors instead of a reference which could lead to a lock down. In **Figure 5**, a differential design of the ULV gate including keeper function is illustrated. From the simulation results presented in **Figure 6**, the keepers contribution in holding the nSFG down to Gnd is clearly visual. This differential design, called ULV-DIFF, would consume approximately the same amount of dynamic power as the ULV, but have the same static dissipation as CMOS. Furthermore, motivation for differential design can also be found in the context of power analysis, were one of the main countermeasure is to use differential design.

In the following the ULV-DIFF and the ULV are compared to standard CMOS. The simulation conditions has been the same for each logic style, though minimum matched output transistors. The recharge and keeper transistors are kept minimum and the input capacitance is 0.7fF and 1fF for nSFG and pSFG, respectively. **Figure 7** and **Figure 8** reinforce the real benefit of the stability and the leakage properties of the ULV-DIFF related to ULV. In **Figure 9** and **Figure 10**, the current dissipation is shown. We like to stress that the dissipation behaviour of the ULV-DIFF is gaining the best from both logic styles, ULV and CMOS. The improvement and as a

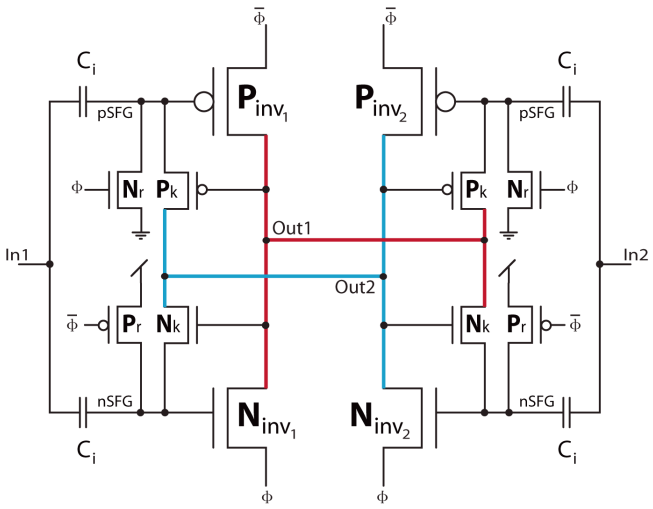

Figure 5. The ultra low voltage differential semi floating-gate inverter including a keeper function, P_k and N_k, is illustrated. Transistor sizes are kept minimum and matched, the input capacitance are scaled relative to obtain the same voltage attenuation for both nSFG and pSFG.

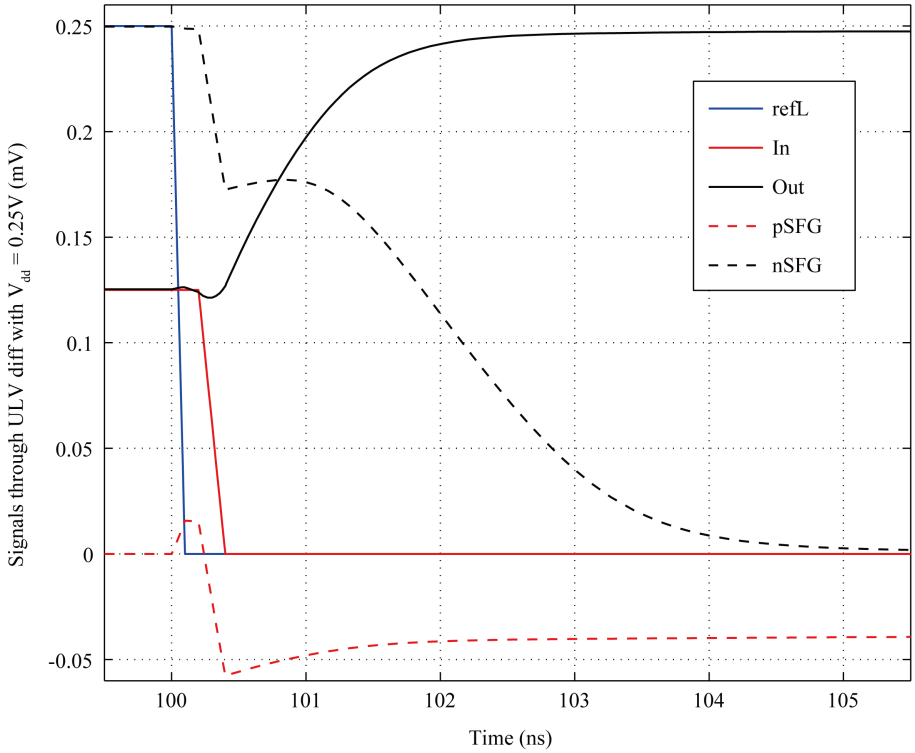

Figure 6. Simulation results showing all signals in the differential ULV gate during evaluation. As seen from the results the keeper functions steps in at approximately 101 ns and pulling the nSFG down to Gnd.

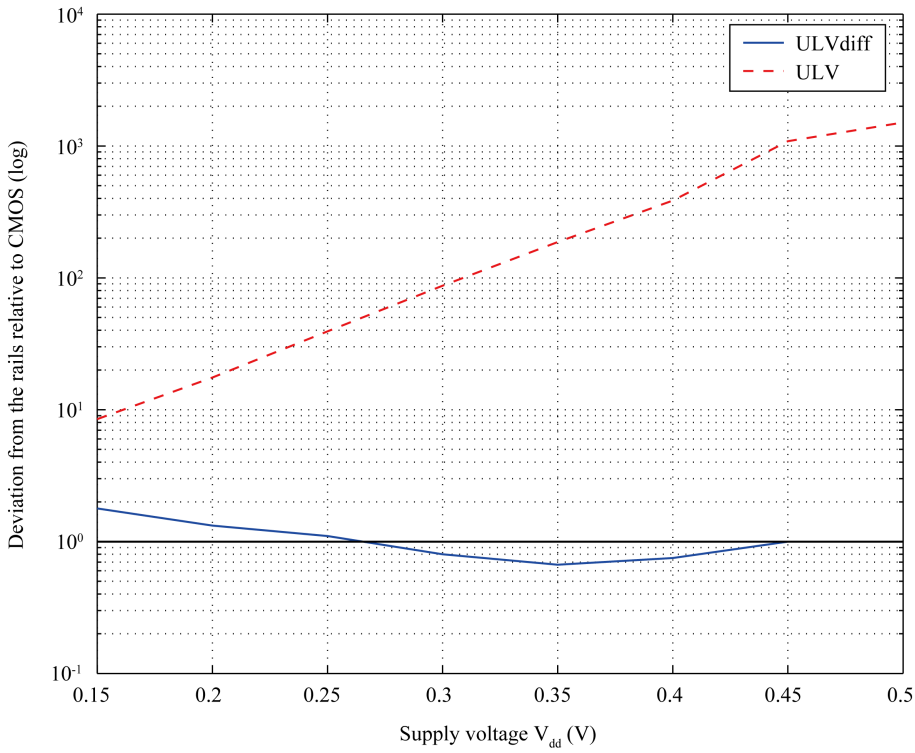

Figure 7. Simulation results showing the deviation for the ULV-DIFF and the ULV relative to CMOS.

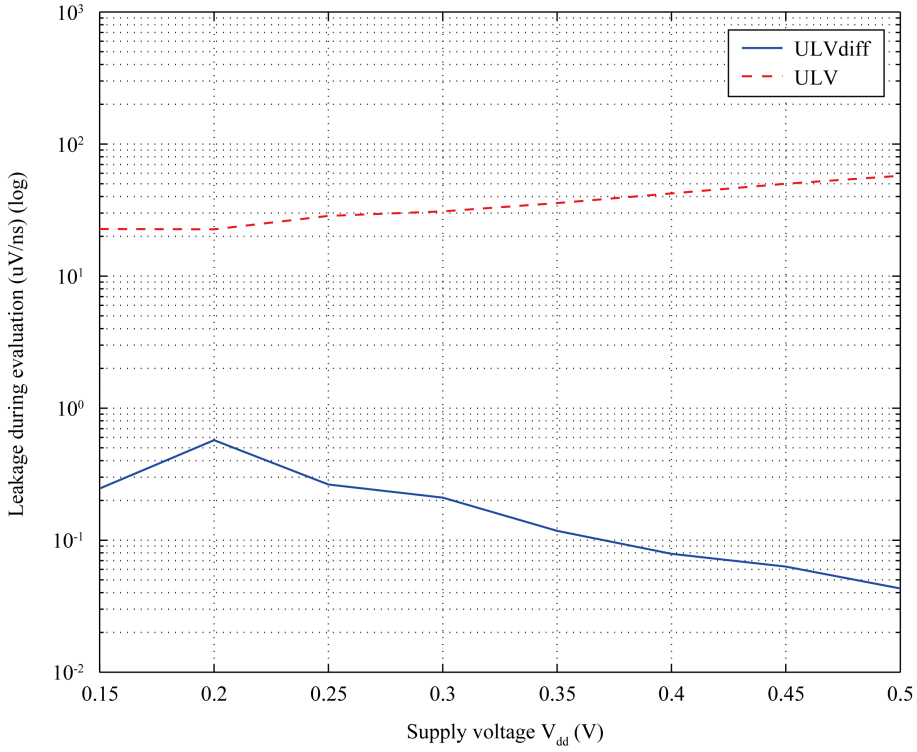

Figure 8. The leakage of the semi floating-gate affecting the output during the evaluation period.

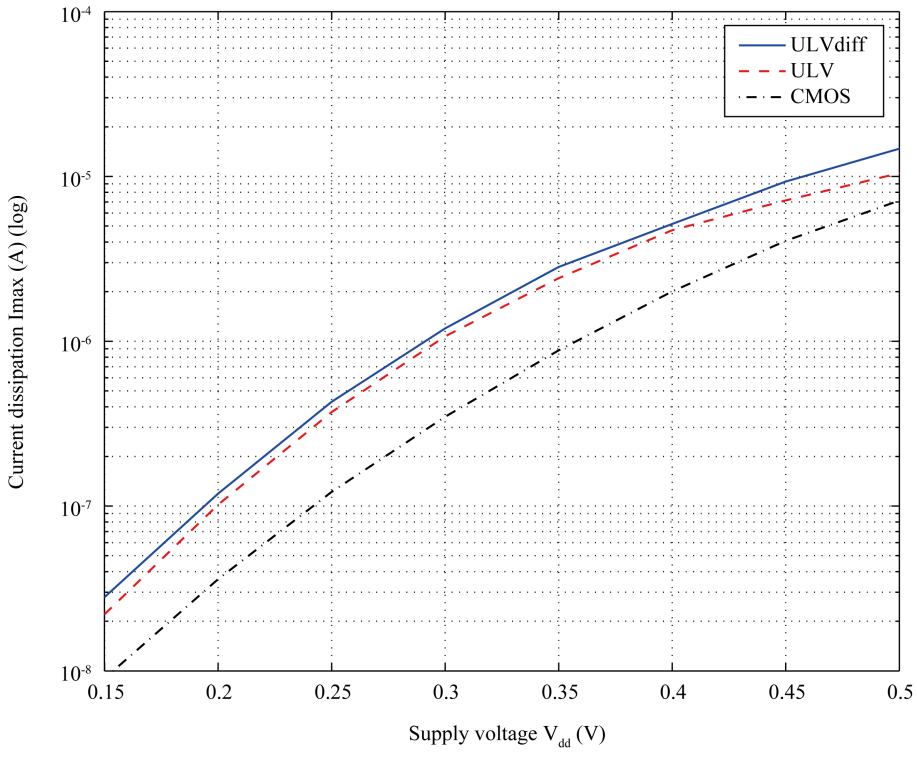

Figure 9. The maximum current dissipation (dynamic dissipation) for all three styles.

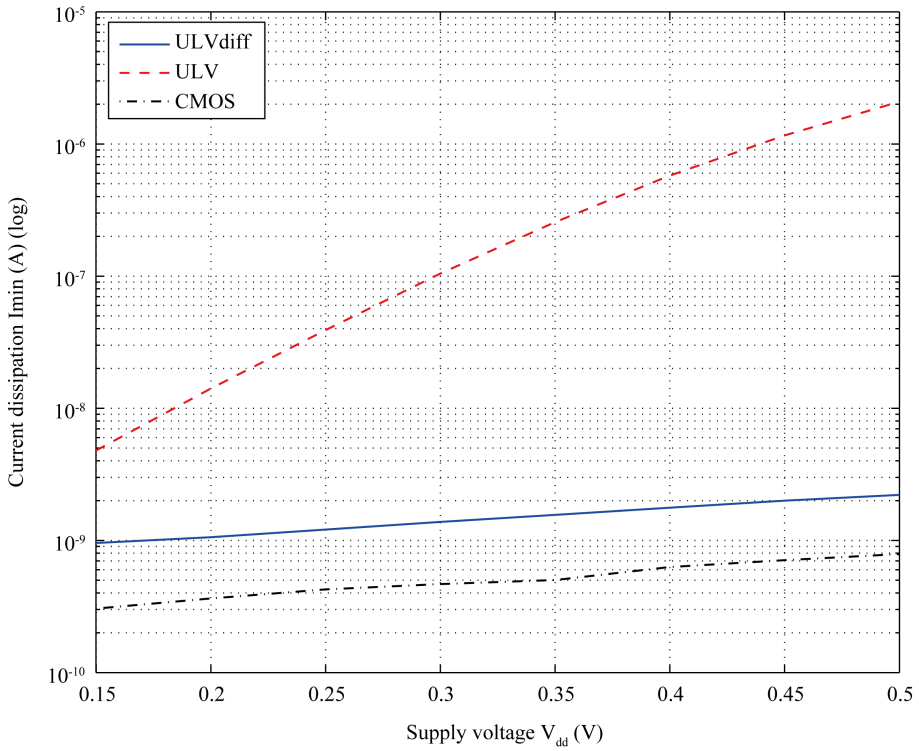

Figure 10. The minimum current dissipation (static dissipation) for all three logic styles.

figure of merit is the EDP for the ULV-DIFF and ULV relative to CMOS given in **Figure 11**. In order to include the stability factor and to have a more fair comparison, the deviation factor relative to CMOS is multiplied to the EDP. **Figure 12** shows the real improvement in ULV-DIFF compared to ULV. The interesting point to extract from all these data is that the optimal point is to have V_{dd} = 0.35 V and that gives a improvement of approximately 5 times better for ULV-DIFF than CMOS and approximately 100 times better for ULV-DIFF than ULV.

5. Reliability and Defect Tolerance

The basis of the results presented in the following are obtained through Monte-Carlo simulations including both process and mismatch variations. The data is collected through 100 runs and a parametric simulation of the supply-voltage V_{dd}. The supply-voltage is swept from 0.15 V - 0.5 V with common conditions and has shown a 100% yield for all three gates. There are three aspects which are of interest that comply after the 100% yield, namely, 1) *delay variation*, 2) *stability* and 3) *noise margin*. In **Figure 13**, the simulation results of a 100 run Monte-Carlo is presented and the fields of interest are commented. Contrary to the standard CMOS both ULV gates have a recharge period and the recharge level represents the gates equilibrium state. With the results in **Figure 13**, the mismatch variations of the transistors are evident and imply a direct consequence, which is altering the recharge level. Accordingly, the offset at the recharge level from $V_{dd}/2$ plays an important role for the succeeding gates. The fundamental behaviour of the floating-gate structures are based upon a input voltage transition from a specified level, in this case $V_{dd}/2$. An offset at the recharge level would decrease the voltage transition seen at the succeeding gates, and may at worst-case not be enough to represent an correct output. In other words, floating-gate structures which employ frequent recharge mechanism with a equilibrium state, $V_{dd}/2$, would complicate and may weaken the fault tolerance. In the light of Monte-Carlo simulation it is interesting to find out what the lowest voltage transition a differential ULV gate needs in order to be reliable also under such corner conditions. Data collected during the 100 runs have showed a maximum voltage deviation from the $V_{dd}/2$ at a V_{dd} = 0.2 V with a variation of $b \approx 30$ mV, which impose a 30% attenuation. **Figure 14** shows how the recharge level changes, using corner simulation, at worst case for different supply-voltages. The higher supply-voltage the more, in terms of mV, the equilibrium state is shifted, but the lower percentage relative to V_{dd}. The

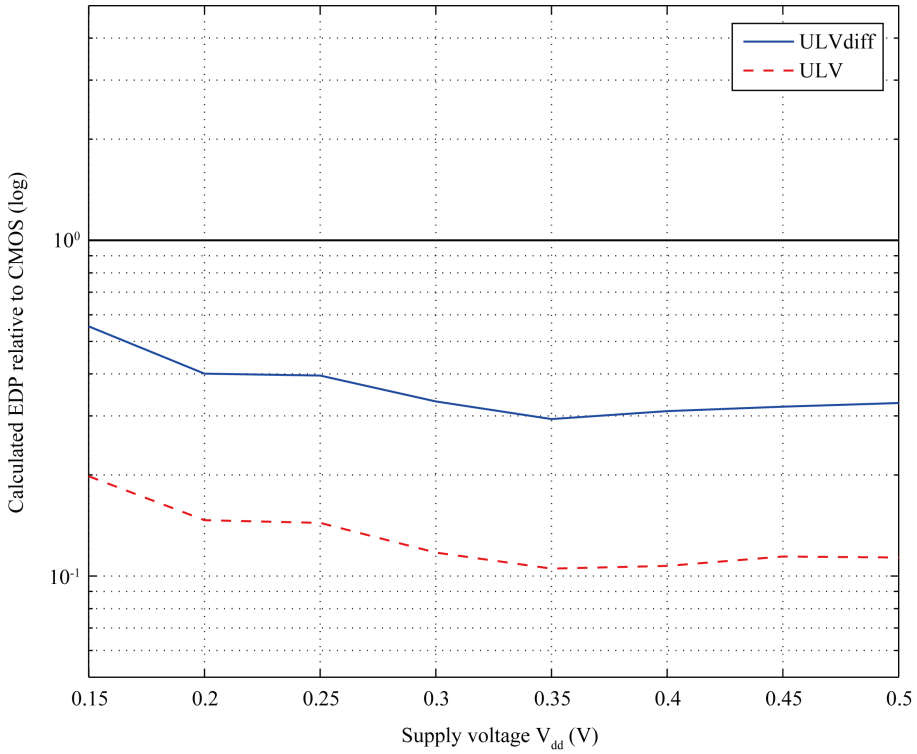

Figure 11. Simulation results for the EDP for the ULV-DIFF and the ULV relative to CMOS.

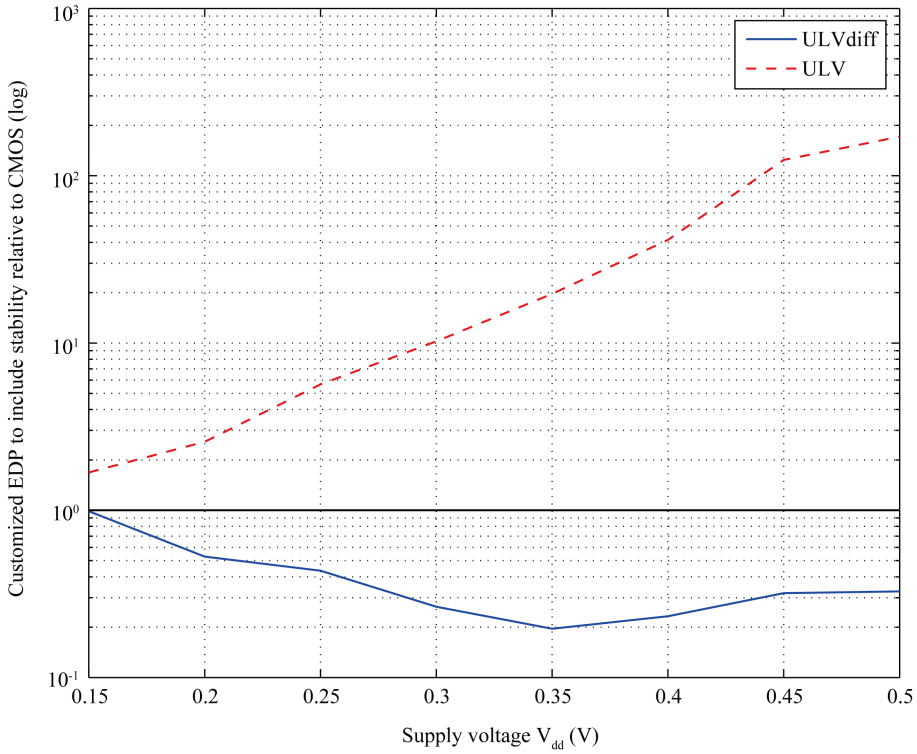

Figure 12. Simulation results for the EDP* stability for ULV diff and ULV relative to CMOS. The results show a optimum point at V_{dd} = 350 mV.

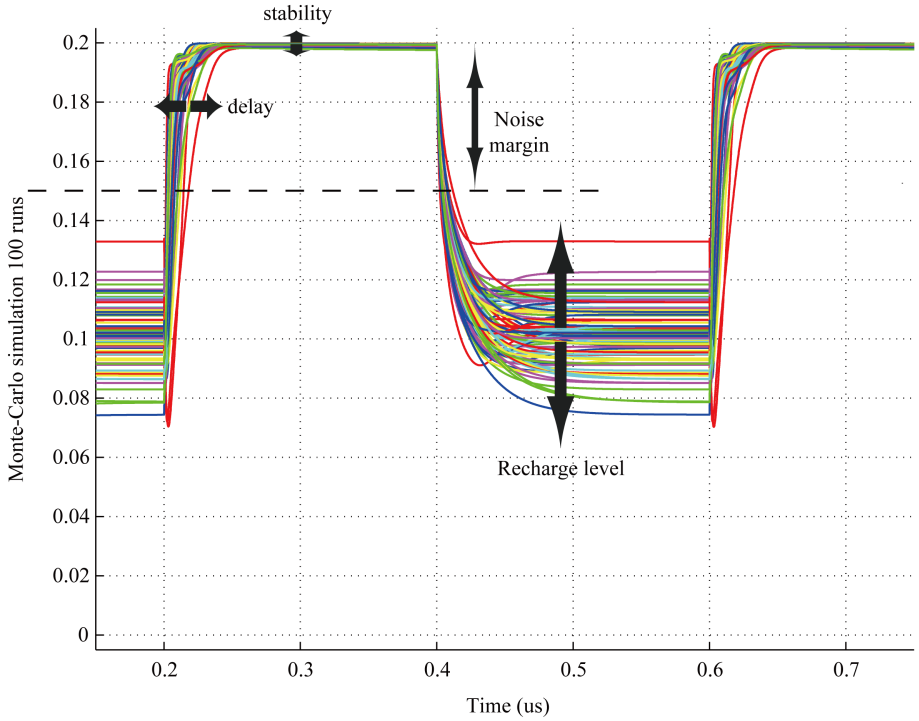

Figure 13. Simulation results for a Monte-Carlo corner simulation for 100 runs of the differential ULV gate shown in **Figure 5**. The environment is set to both process and mismatch variation. On the plot there are four commented areas to emphasise the discussion topics.

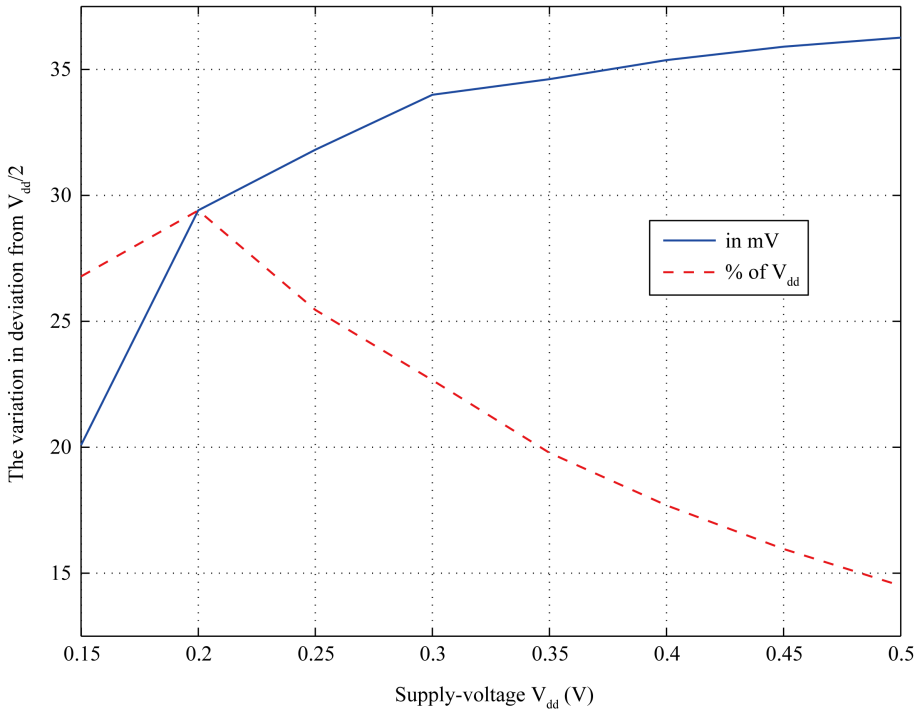

Figure 14. Simulation results have shown variation due to mismatch at the recharge level. The plot represents both the deviation from the optimal equilibrium state, $V_{dd}/2$, and the percentage within the supply-voltage V_{dd}.

plot in **Figure 14** shows an intersect at V_{dd} = 200 mV and an attenuation of 30%. Although an attenuation of 30% is quite much, the differential ULV gate has not shown any signs of malfunction. The differential ULV gate has, as **Figure 15** illustrates, been simulated with an input voltage transition which is attenuated 80% and still are able to output correctly and also to a very good stability. The main affect an attenuation would imply is the increase in delay, *i.e.* the more an input signal is attenuated the higher the evaluation delay would become. Furthermore, the attenuation is also a function of the relation to the capacitive ratio seen at the semi-floating-gates. The robustness to a large attenuation for the differential ULV gate should be credited to the keeper function. The keeper transistor would help to turn off the right transistor as long as there is a small change in the output. Actually, as long as the two differentiated output are shifting in the opposite direction from each other from the equilibrium state, the representative keeper transistors would help the output drivers to symmetrically pull their representative outputs to the rails. Therefore, the ULV gate which does not have the keeper function is not expected to sustain a corner situation where the recharge level is shifted and thus generating an attenuation of more than 30%. Furthermore, it is important to stress that the keeper function also provides high stability under any circumstances in terms of deviation from the rails.

The situation where worst case recharge level offset and the worst case mismatch of the transistors regarding delay arise on the same chip and for two succeeding gates is highly unlikely. In a simulation environment, such as Monte-Carlo, only one given aspects is examined. Referring back to **Figure 13**, the worst case of mismatch and process variation gives a change in the delay. The delay are measured based on a 50% to 50% input and output transition. The same conditions apply for all three designs. The maximum delay variation for a Monte-Carlo simulation with 100 runs is displayed in **Figure 16**. The delay variation would increase if the simulation environment has included a sweeping parameter to represent the offset at the recharge level. The need to easier evaluate and visualise the collected data and to lay a foundation for discussing the values relative to CMOS, the data is plotted in **Figure 17**. There is a minimum delay variation found at V_{dd} = 300 mV both for the ULV and the differential ULV.

Once the delay is considered, the next topic is the stability of the gates. The stability represents the deviation from the rails and can also be used to indicate the yield during corner simulation. Bear in mind that the data set

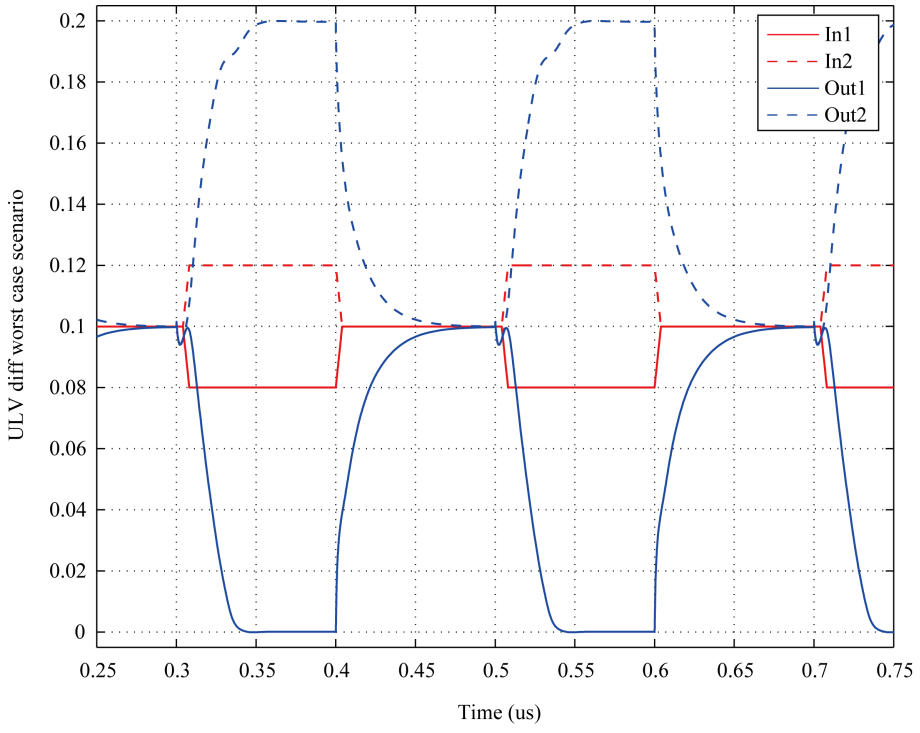

Figure 15. Simulation results for the differential ULV gate verifying the gates ability to operate on very high attenuation for the input signal. The simulated environment is reflecting an input transition which is attenuated 80% and the outputs are for a succeeding gate.

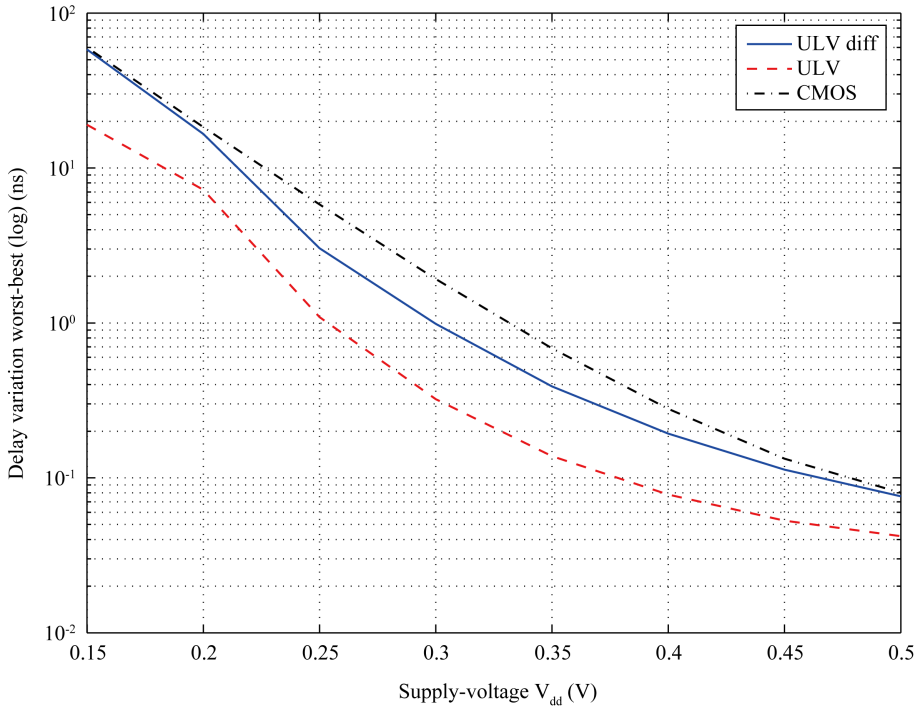

Figure 16. Corner simulations show a delay variation as a mismatch at the input capacitors and transistors. The delay variation is calculated from a 50% to 50% input and output transition.

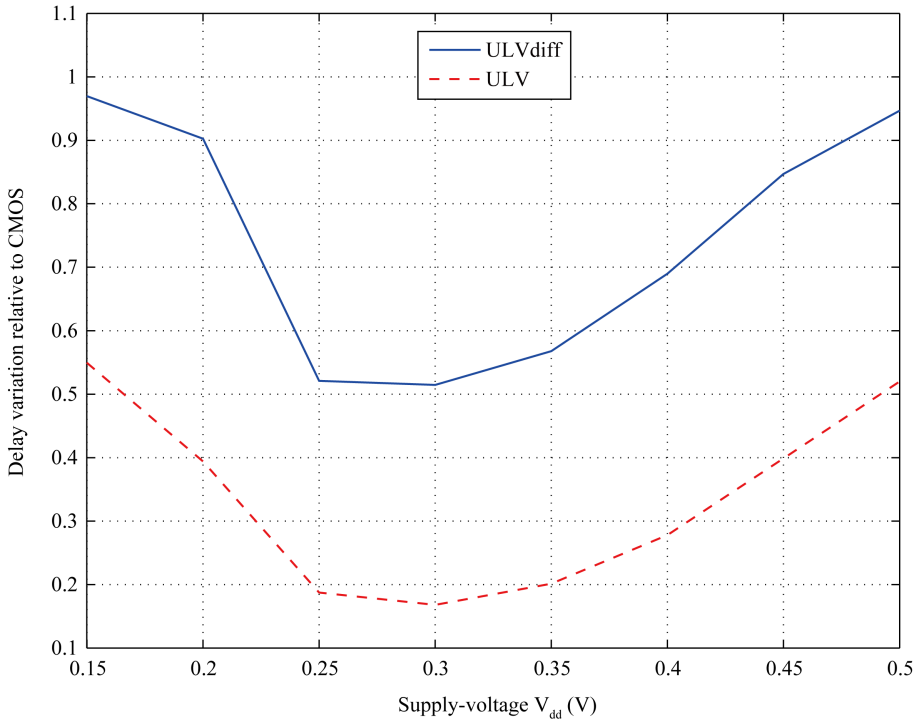

Figure 17. The delay variation obtained during Monte-Carlo simulation is plotted relative to CMOS. The main goal is to bring out the difference and the potential of the ULV gates. Both gates show a minima at V_{dd} = 300 mV.

used are for a V_{dd} ranging from 150 mV to 500 mV and that all gates have showed 100% yield. Previously, the

ULV were implied to have a lower yield due to the leakage at the semi-floating-gates. Although this statement has not been proved, the indications showed by **Figure 18** further strengthen the statement. The figure represents the stability variation relative to CMOS for different supply voltages. The stability variation is calculated as the difference between the best and worst stability during 100 runs.

6. Discussion

All the simulation results speak in the favour of the differential ULV gate. Firstly and the most beneficial aspect is the reliability the keeper function adds, even though the recharge levels are shifted. Secondly, the delay variations show an optimal point at V_{dd} = 300 mV. Considering the threshold voltage, V_{th}, which for a 90 nm process is approximately 270 mV, a general optimal point is expected to be around the V_{th}. Previous work on differential ULV gate has showed an optimal point for EDP to be at V_{dd} = 350 mV [11]. Referring to **Figure 17**, there is not much of a difference between 300 mV and 350 mV. Thirdly, the stability of the gates has demonstrated quite a large difference. The leakage at the semi floating-gate for the ULV gate really rules out its candidate. Fortunately, the keeper function at the differential ULV gate ensures that its candidate is present alongside standard CMOS. It can actually be found that the stability for the differential ULV gate is actually better than CMOS for V_{dd} from 230 mV to 430 mV, with a local minimum at 300 mV. Referring to **Figure 18**, the plot clearly demonstrates the difference of the stability relative to CMOS. Ones again the results from corner simulations show an optimal point at 300 mV. Last but not least, the discussion about the yield of the gates is presented in **Figure 19**. The plot shows that the ULV gate is barely surviving the lowest supply-voltage, while the differential ULV gate at worst case is within 80% of the noise margin. An interesting discussion of the results are that the differential ULV gate becomes more and more stable and closer to obtaining 100% within the noise-margin, while the same cannot be seen for the ULV gate. The data show that the ULV gate has a top peak at V_{dd} = 350 mV. From all these results, there is a reason to believe that the optimal V_{dd} should be around 325 mV, in order to achieve the best EDP, reliability and fault tolerance. Furthermore, the main credit should be given to the keeper function. The kee-

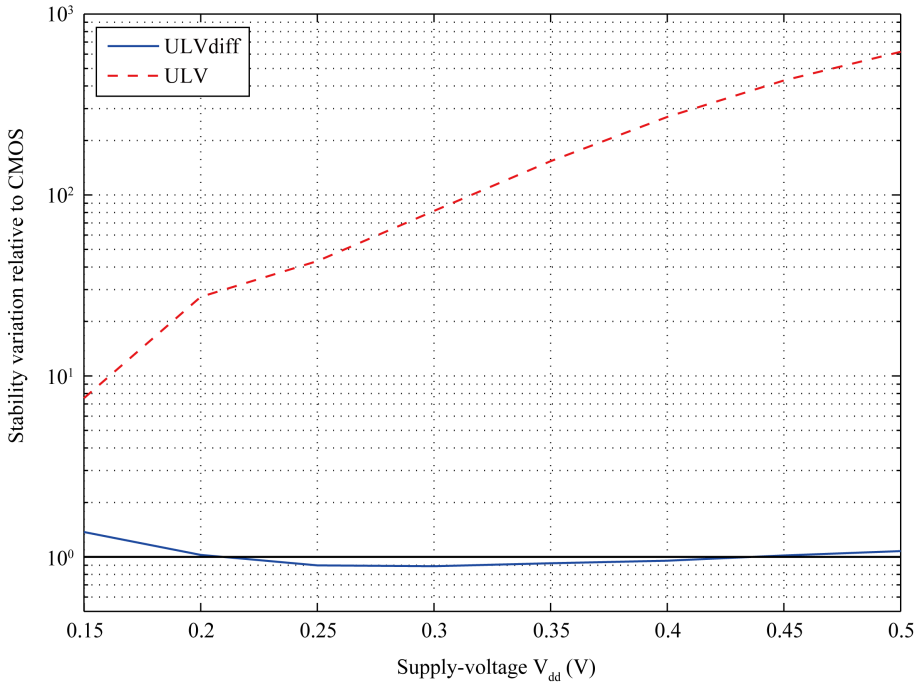

Figure 18. The stability variations during a Monte-Carlo simulation relative to CMOS are plotted. The ULV gates stability decreases as the stability variation increases as a function of V_d. The differential ULV gate shows an improvement of stability relative to CMOS for V_{dd} at the range 150 mV to 500 mV.

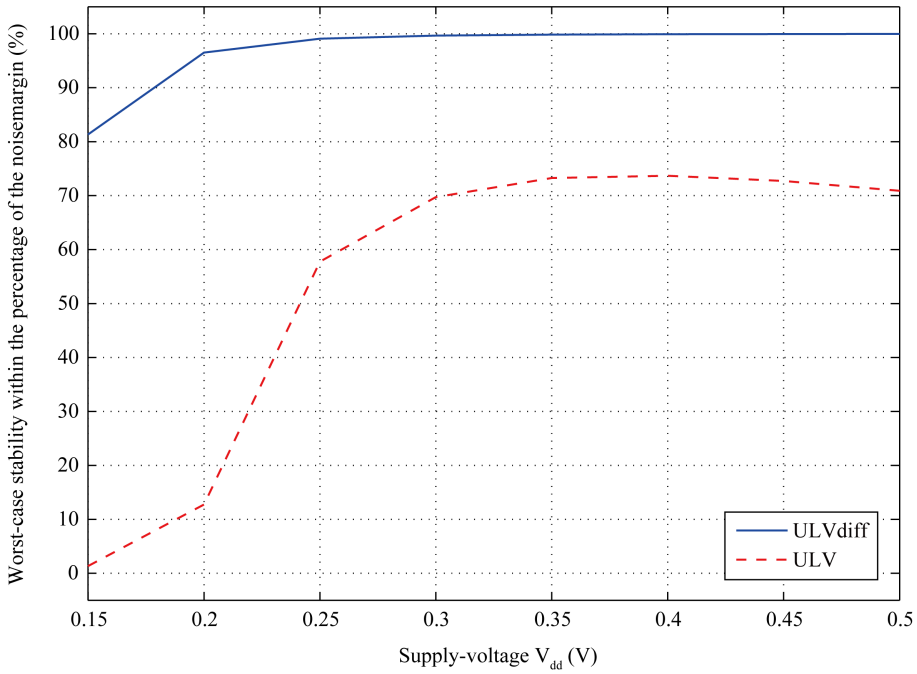

Figure 19. Simulation results for the lowest evaluation stability as percentage within the noise margin is presented. This plot can also be directly used to elaborate on the yield of the gates. In the V_{dd} range given, all gates have 100% yield, but the ULV is barely surviving corners as the V_{dd} decreases.

per function, as obtained from the results, can be regarded to protect the benefit, *i.e.* speed, of the ULV gate and to strengthen its weakness, *i.e.* stability, hence giving the differential ULV gates the best from both designs, ULV and standard CMOS.

Finally, the last aspect is the noise margin for the gates. The noise margin is actually closely linked to the yield. The data collected through corner simulation representing noise margin follow the formula below:

$$\frac{stability_{WC} - \left(V_{dd} \cdot 0.75\right)}{V_{dd} \cdot 0.25} \tag{2}$$

where is the lowest evaluation value through the 100 runs. The result will give a value which represents that the worst case stability is within the percentage of the noise-margin. The lower the result is, the closer the output is to the limits of the noise margin. In the context of yield, it can be used to denote that a result above 0 has a 100% yield. The result for corner simulation is given in **Figure 19**. As stated earlier for the ULV gate, the prediction for a 100% yield is diminishing. The result for a standard CMOS is very close to the differential ULV, as can be implied by **Figure 18**, and thus not been included in the plot of **Figure 19**.

References

[1] Verma, N., Kwong, J. and Chandrakasan, A. (1995) Nanometer MOSFET Variation in Minimum Energy Subthreshold Circuits. *IEEE Transactions on Electron Devices*, **55**, 847-854.

[2] Chandrakasan, A.P., Sheng, S. and Brodersen, R.W. (1992) Low-Power CMOS Digital Design. *IEEE Journal of Solid-State Circuits*, **27**, 473-484.

[3] Burr, J.B. and Peterson, A.M. (1991) Ultra Low Power CMOS Technology. *NASA VLSI Design Symposium*, Idaho, 30-31 October 1991, 4.2.1-4.2.13.

[4] Burr, J.B. and Shott, J. (1994) A 200 mV Self-Testing Encoder/Decoder Using Stanford Ultra Low-Power CMOS. *IEEE Solid-State Circuits Conference* (*ISSCC*), San Francisco, 16-18 February 1994, 84-85. http://dx.doi.org/10.1109/ISSCC.1994.344717

[5] Usami, K. and Horowitz, M. (1995) Clustered Voltage Scaling Technique for Low-Power Design. *Proceedings of the*

1995 *International Symposium on Low Power*, Dana Point, 23-26 April 1995, 3-8. http://dx.doi.org/10.1145/224081.224083

[6] Berg, Y., Wisland, D.T. and Lande, T.S. (1999) Ultra Low-Voltage/Low-Power Digital Oating-Gate Circuits. *IEEE Transactions on Circuits and Systems II*: *Analog and Digital Signal Processing*, **46**, 930-936.

[7] Berg, Y., Mirmotahari, O., Norseng, P.A. and Aunet, S. (2006) Ultra Low Voltage CMOS Gates. *IEEE International Conference on Electronics*, *Circuits and Systems* (*ICECS*), Nice, 10-13 December 2006, 818-821.

[8] Mirmotahari, O. and Berg, Y. (2009) Digital Ultra Low Voltage High Speed Logic. *Proceedings of the International MultiConference of Engineers and Computer Scientists*, Hong Kong, 18-20 March 2009, 1-1.

[9] Berg, Y., Mirmotahari, O., Lomsdalen, J. and Aunet, S. (2008) High Speed Ultra Low Voltage CMOS Inverter. *IEEE Computer Society Annual Symposium on VLSI*, Montpellier, 7-9April 2008, 122-127.

[10] Mirmotahari, O. and Berg, Y. (2008) Low Voltage Design against Power Analysis Attacks. *IEEE International Symposium on Electronic Design*, *Test and Applications* (*DELTA*), Hong Kong, 23-25 January 2008, 545-549.

[11] Mirmotahari, O. and Berg, Y. (2008) Ultra Low Voltage High Speed Differential CMOS Inverter. *IEEE PATMOS LNCS*, 10-12 September 2008, Lisbon, Portugal, 1-1.