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A Novel High-Performance Lekage-Tolerant, Wide Fan-In Domino Logic Circuit in Deep-Submicron Technology

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Abstract

As technology shrinks in modern era the demand on high speed, low power consumption and small chip area in microprocessors is come into existence. In this paper we have presented a new class of domino circuit design for low power consumption, faster circuit speed and high performance. Due to wide fan-in domino logic, its logic gate suffer from noise sensitivity, if we improve sensitivity, sub-threshold and gate oxide leakage current dominate in evaluation network, which increases the power consumption and reduces the performance of the circuit. The proposed circuit improves the dynamic power consumption and reduces the delay which improves the speed of the circuit. Simulation is performed in BISM4 Cadence environment at 65 nm process technology, with supply voltage 1 V at 100 MHz frequency and bottleneck operating temperature of 27˚C with C_L = 1 fF. From the result average power improvement by proposed circuit 1 & 2 for 8 input OR gate is 10.1%, 15.28% SFLD, 48.56%, 51.49% CKD, 55.17%, 57.71% HSD and improvement of delay is 1.10%, 12.76% SFLD, 19.13%, 28.63% CKD, 4.32%, 15.59% HSD, 19.138%, 44.25% DFD respectively.

Keywords

High Speed Integrated Circuit, Dynamic Logic Circuit, Unity Noise Gain (UNG), Domino Logic Circuit, Noise Immunity

1. Introduction

As technology scales down power consumption is dominant in deep sub-micron technology. Power consumption

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is divided into two parts static and dynamic circuit. When we talk about low power, high speed, we prefer dynamic logic instate of static CMOS circuits, by generating proper logic at output of the circuit. All these properties of the dynamic node make it high robust circuit, to generate proper logic in dynamic CMOS circuits, so to achieve high performance. Main limitations of dynamic logic occur during cascading of similar circuit during cascading of large circuit an erroneous state occurs in dynamic logic design; another problem which come into existence is charge sharing which reduces the voltage of dynamic node. So to overcome from the problem a week PMOS transistor (with a small (W/L) ratio) placed parallel to pre-charge transistor, which is feedback from the output, the output of the circuit is connected with inverter for reducing the cascading problem [1].

Domino logic circuit is also a kind of dynamic logic circuit which is used for the high speed and high performance application. Also the domino logic circuit plays a vital role where fan in are high in any circuit. Domino circuits are widely used in high performance microprocessors, register files, ALU, DSP circuits and priority encoders in content addressable memories, such as high fan-in multiplexer or comparator circuits. A basic footer less domino logic circuit is shown in **Figure 1** where in pre-charge phase (clk = 0) PMOS transistor ON and charge the dynamic node, during evaluation phase (clk = 1) the dynamic node discharge when any one of the input is ON, the output of the inverter is feed back to week keeper transistor so to maintain the charge on dynamic node.

In this paper, a new domino circuit for wide fan-in applications in ultra deep sub-micrometer technologies is proposed. The novelty of the proposed circuit is that our work simultaneously reduces the delay and leakage power consumption.

The rest of the paper is organized as follows. Section 1 explains some basics of domino logic circuits. Typical conventional approach has been discussed in Section 2. Section 3 gives the brief of proposed circuit for the betterment of the noise margin. Simulation result and conclusion are discussed in Section 4 and Section 5 respectively.

2. Literature Review

The most popular domino logic is the standard footless domino [2] circuit as shown in **Figure 1**. For enhance the performance of the microprocessor, modification is done on circuit level to increase the robustness of the circuit, without penalty of noise immunity, the keeper transistor is added. Keeper transistor is feedback from the output; keeper transistor *W*/*L* ratio is very low to maintain the charge in the dynamic node.

The keeper ratio *K* is defined as

$$K = \frac{\mu p\left(\frac{W}{L}\right)\text{Keeper} - \text{transistor}}{\mu n\left(\frac{W}{L}\right)\text{evaluation} - \text{network}} \tag{1}$$

where *W* and *L* denote the transistor size, and mobility of electron and hole is represented by μn and μp. However by inserting the keeper transistor performance of the circuit is degraded and power dissipation increases. Upsizing the keeper transistor is another solution for improves robustness but it result in higher power dissipation and delay [3]. Contention between evaluation network and keeper transistor, therefore size of the keeper transistor should be low to achieve high-speed in microprocessor. Thus, trade off exist between delay and power to improve noise and leakage immunity [4]. Several techniques introduce in this section to address this issue.

2.1. High Speed Domino Logic (HS)

High speed domino is another domino logic circuit. In domino logic circuit current drawn through the keeper transistor and pull down network NMOS transistors at the beginning of the evaluation phase, can be reduced by applying a clock delay in the circuit. That does not affect the leakage current in the circuit [5]. But apart from this the extra clock delay consumes extra area and power, which is a big drawback of the circuit as shown in **Figure 2**. In High speed domino logic circuit when clock becomes high, M_{n1} is still off and M_{p2} is still on. Therefore M_{p2} turns off the keeper transistor. After some delay of inverter M_{p2} becomes off. Hence at the beginning of evaluation phase dynamic node is afloat, so in the absence of keeper transistor, evaluation node may be discharged for any noise at the input section [7]. Also the voltage at the gate of the keeper transistor would be V_{DD}-V_{tMn1}. This would provide a dc current flow through the PMOS keeper transistor and the NMOS network.

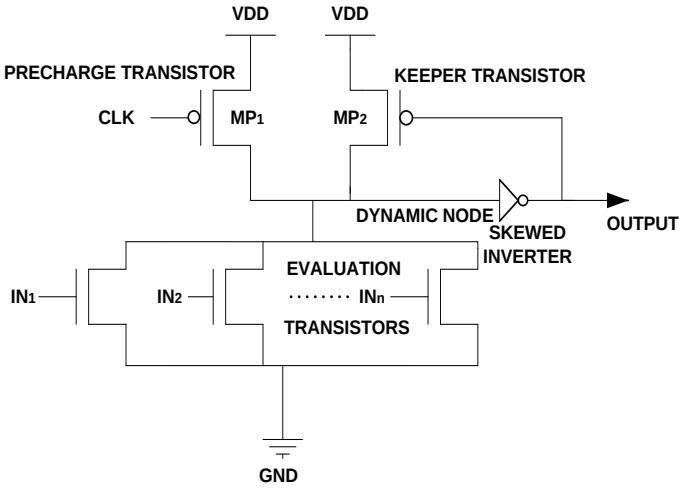

Figure 1. Standard footer less domino logic.

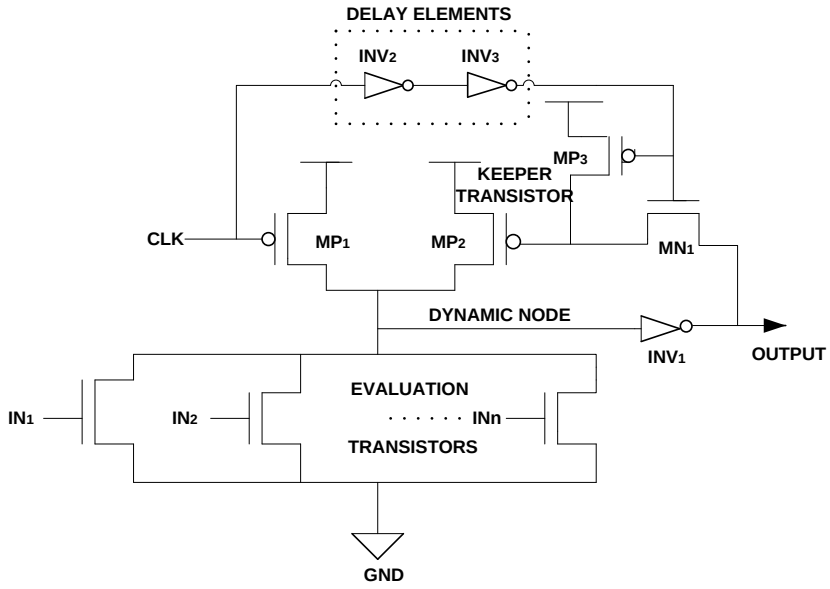

Figure 2. High speed domino logic.

2.2. Conditional Keeper Domino Logic (CKD)

The conditional keeper domino logic contains two PMOS transistor keeper circuit [6]. In which one is of smaller strength and other is of higher strength as shown in **Figure 3**. Now when the dynamic node is at high voltage M_{kp1} gets turn on to avoid voltage drop at the dynamic node. If the dynamic node is still high, then after a certain amount of delay, during the evaluation phase output of NAND gate becomes low which makes M_{k2} to turn on? For maintaining the state of dynamic node, is M_{k1} responsible during the beginning of evaluation phase and M_{k2} is responsible for the rest of the evaluation phase [7].

2.3. Diode Footed Domino (DFD)

In diode footed domino we modify the conventional domino circuit by adding an nMOS transistor M_1 in series with the foot of the evaluation network. This nMOS transistor is in diode configuration *i.e.* gate and drain terminals connected together. **Figure 4** [9] shows the Diode Footed Domino configuration. Stacking effect [10] occur because this transistor M_1 is connected in series with the evaluation network [12] [13]. Thus sub-threshold leakage current reduces as a result of stacking effect. DFD circuit works as follow:

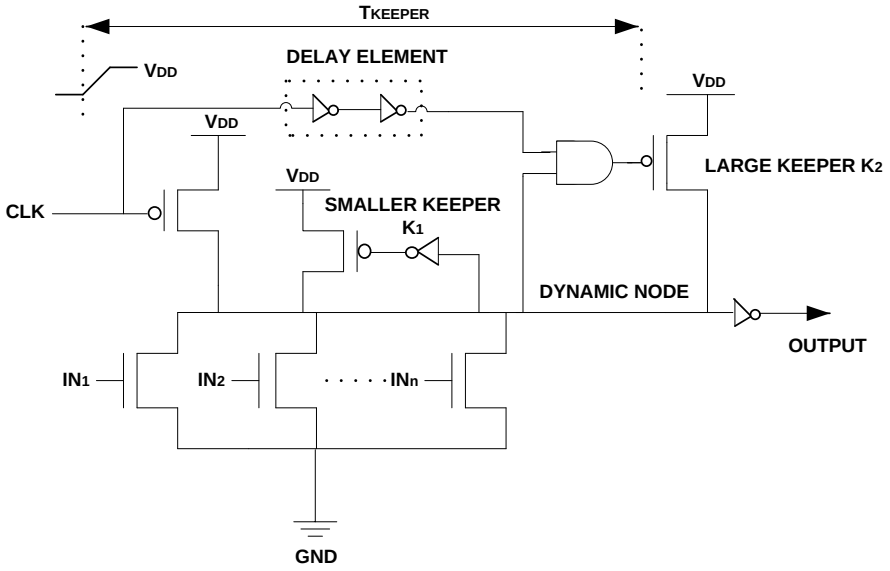

Figure 3. Conditional keeper domino logic.

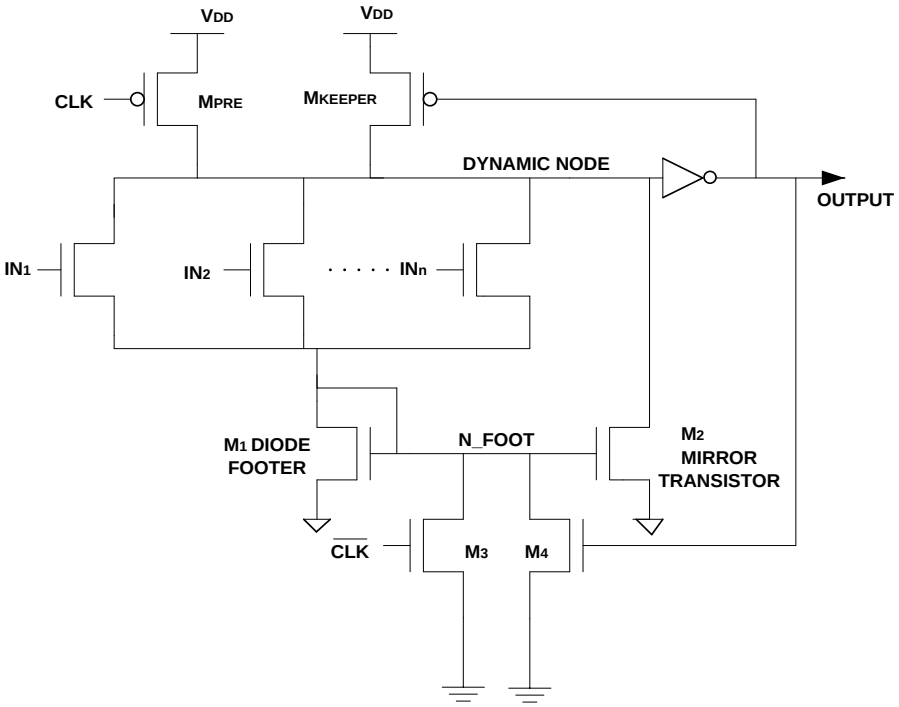

Figure 4. Diode footed domino logic.

The mirror ratio is defined as the ratio of the current drivability of the mirror transistor to that of the diode footer:

$$M = \frac{\left(\frac{W}{L}\right)_{\text{mirror transistor}}}{\left(\frac{W}{L}\right)_{\text{diode footer}}}$$

By increasing the mirror ratio, the performance can be increased.

3. Proposed Circuit

In conventional footer less circuit, during precharge phase (clk = 0), PMOS transistor ON and charge the dynamic node from V_{dd}, during evaluation phase (clk = 1), a dynamic node not able to maintain the constant because PMOS transistor rail OFF from $V_{dd,}$ only keeper Transistor connected to V_{dd} maintain the charge of dynamic node if all the transistor is OFF in evaluation network as shown in **Figure 5**. During evaluation phase when any one input is ON of NMOS block the dynamic node will discharge, which result in flow of sub-threshold and gate oxide leakage current which result in degradation of UNG of the circuit, for reduction of leakage current and enhance the noise immunity of the circuit we have proposed a circuit.

In proposed circuit modification is done in evaluation network, we have inserted two NMOS transistor between dynamic node and pull down network. To improve the efficiency of the proposed circuit and extra NMOS transistor is connected to the dynamic node to produce the proper stacking of the evaluation network, to increase the noise immunity of the circuit and reduces the leakage current of the circuit by providing half swing logic at the output node as sown in **Figure 6**. In footed portion we place NMOS transistor, during pre-charge phase footed transistor is OFF, during evaluation phase a charge discharge from dynamic node the two NMOS transistor provides the stacking effect for leakage reduction and high noise immunity. In proposed circuit 2 as shown in **Figure 7**. Input of footed transistor is connected to clock and three inverter for generation of delay in the footed transistor, the delay element is used for proper slower the gate and greater noise robustness. These approaches do not reduce the overall leakage current, but only the leakage current at the dynamic node that drives the final static inverter and is the critical node. Hence we have more degree of freedom for increasing speed or enhance noise immunity by reducing the leakage current.

4. Simulation Results and Comparison

The proposed circuit was simulated using BISM4 Cadence virtuoso schematic editor tool in the high-performance 65-nm predictive technology and at the temperature of 27˚C. The supply voltage used in the simulations is 1 V, for 8, 16 and 32 input OR gates as shown in **Tables 1-4**. Various parameters have been mitigated such as power dissipation, delay and UNG (Unit Noise Gain). **Table 4** calculate the standby leakage current at different temperature for 8, 16 and 32 inputs, operating frequency is 100 MHz with C_L = 1 pF of the circuit. Average power consumption of existing domino logic circuit and proposed circuit is shown in **Figure 8**. UNG graph is shown in **Figure 9**.

The noise-margin metric used in this paper is called the unity noise gain (UNG). For calculation of UNG [11], a pulse noise is applied to all inputs with amplitude which is a fraction of supply voltage and a pulse width equal to 30% of duty cycle. This noise amplitude is defined as

$$\mathrm{UNG} = \{\mathrm{Vin}, \mathrm{Vnoise} = \mathrm{Voutput}\}$$

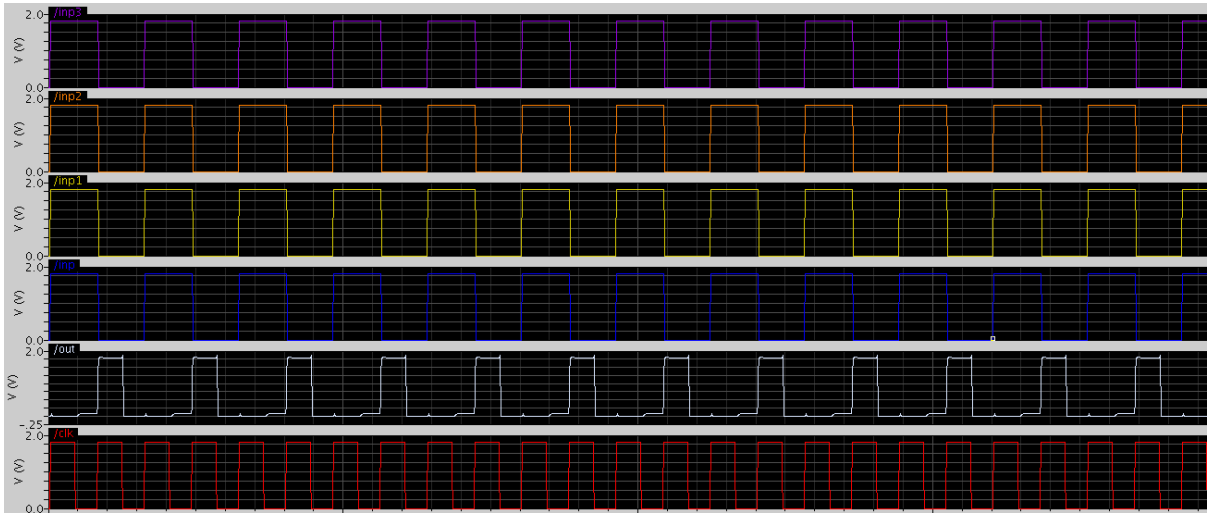

Figure 5. Output wave form of proposed circuit.

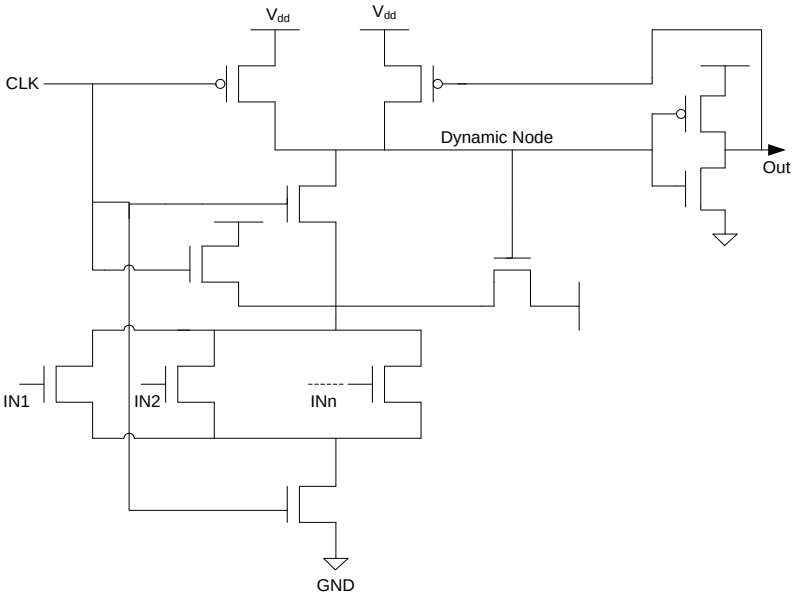

Figure 6. Proposed circuit 1.

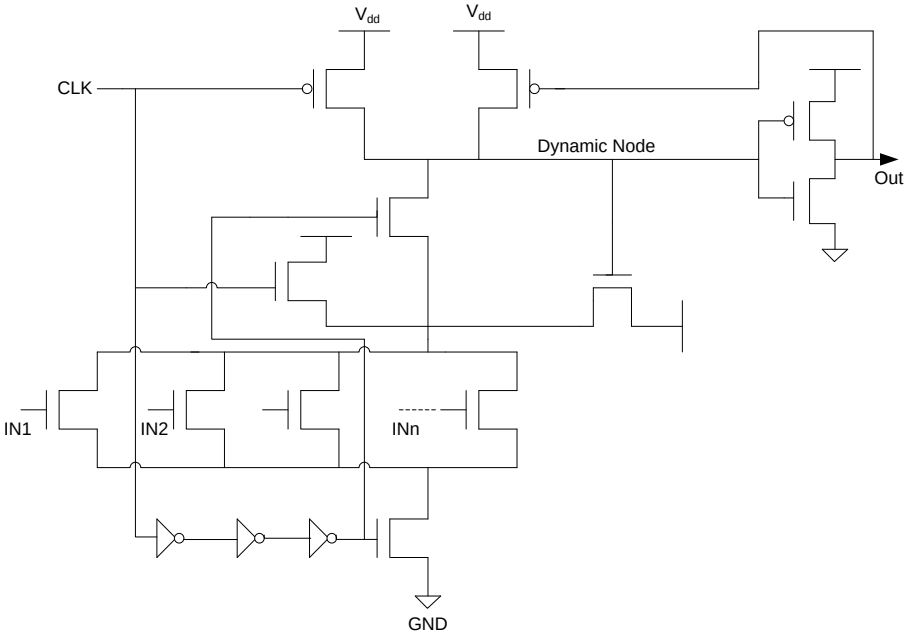

Figure 7. Proposed circuit 2.

Table 1. Comparison of power dissipation (μW).

S. No.	Logic Style	8 Input	16 Input	32 Input
1.	**SFLD**	2.611	4.234	7.632
2.	**CKD**	4.56	6.323	9.862
3.	**HSD**	5.231	8.214	10.12
4.	**DFD**	1.672	2.540	3.965
5.	**Proposed Circuit 1**	2.345	5.203	8.812
6.	**Proposed Circuit 2**	2.212	4.780	7.642

Table 2. Comparison of UNG (in Volt).

S. No.	Logic Style	8 Input	16 Input	32 Input
1.	**SFLD**	0.252	0.228	0.212
2.	**CKD**	0.264	0.225	0.199
3.	**HSD**	0.243	0.230	0.203
4.	**DFD**	0.274	0.256	0.2574
5.	**Proposed Circuit 1**	0.263	0.231	0.203
6.	**Proposed Circuit 2**	0.254	0.224	0.191

Table 3. Comparison of Delay (in ps).

S. No.	Logic Style	8 Input	16 Input	32 Input
1.	**SFLD**	13.102	18.435	28.59
2.	**CKD**	16.015	21.2	31.23
3.	**HSD**	13.541	18.32	28.43
4.	**DFD**	16.49	22.16	33.12
5.	**Proposed Circuit 1**	12.95	15.651	21.34
6.	**Proposed Circuit 2**	11.432	14.125	19.57

Table 4. Stand by leakage current of proposed circuit (in nA).

S. No.	Temperature	8 Input	16 Input	32 Input
1.	**27˚C**	262.25	308.79	401.11
2.	**50˚C**	364.12	411.34	505.45
3.	**110˚C**	700.24	754.23	851.34

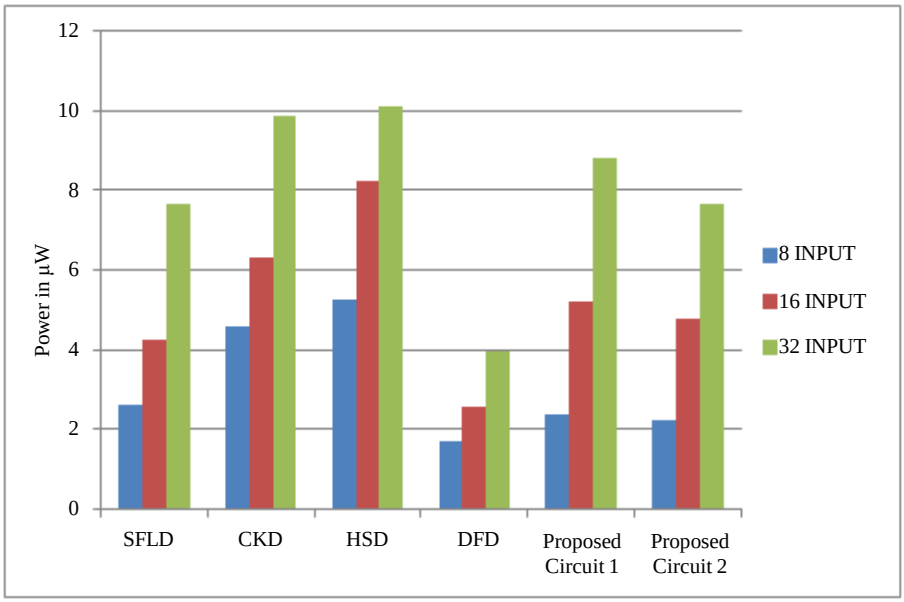

Figure 8. Comparison of average power.

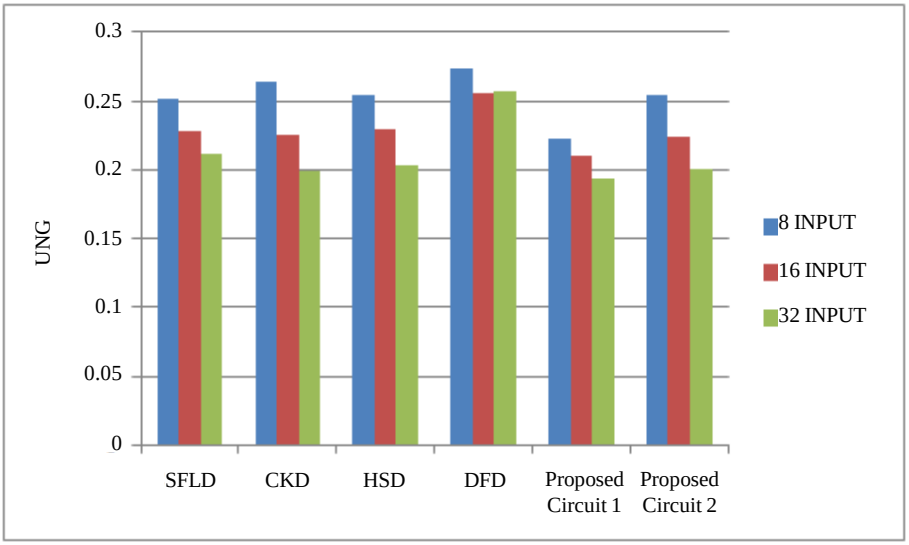

Figure 9. Comparison of UNG.

5. Conclusion

Domino logic dissipates very low standby power compare to static CMOS logic. The novelty of the proposed circuit is that domino circuit reduces the leakage power consumption by maintaining the same level of delay and UNG. In this paper our main objective was to improve the noise immunity and to reduce the average power consumed and delay associated with the circuit. The analysis shows that we get an appreciable improvement in the noise margin and power consumption and marginal improvement in delay. The whole comparison is based upon 65 nm CMOS technology using Cadence Virtuoso tool.

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