Circuits and Systems, 2015, 6, 60-69
Published Online March 2015 in SciRes. http://www.scirp.org/journal/cs
http://dx.doi.org/10.4236/cs.2015.63007

Design of Ultra-Low Power PMOS and NMOS for Nano Scale VLSI Circuits

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Received 22 September 2014; accepted 23 March 2015; published 25 March 2015

Abstract

CMOS devices play a major role in most of the digital design, since CMOS devices have larger density and consume less power. The integrated circuit performance mostly depends on the basic devices and its scaling methods, but in conventional CMOS devices in ultra deep submicron technology, leakage power becomes the major portion apart of dynamic power. The demerits of the conventional CMOS is less speed and, more leakage, for any digital design PDP is the figure of merit which can be used to determine energy consumed per switching event, hence we designed a NOVEL NMOS and PMOS which has superior performance than conventional PMOS and NMOS, the design and performance checked at 90 nm, 180 nm and 45 nm technology and calculate the performance values.

Keywords

Power Delay Product, Average Power, Static Power, Delay, Dynamic Threshold CMOS

1. Introduction

The need for low power chips is the increased marked demand for portable consumer electronics powered by the batteries, which have not experienced the similar rapid density growth compared to electronics circuits. It has been concluded that battery technology alone will not solve power problems in the near future. Therefore designing a chip with low power is becoming a major concern in the chip design industry. The different power reduction techniques from device level to circuit level and system level have been shown as a low power taxonomy [1].

In ultra-deep submicron technology especially below 45 nm technology, leakage power is becoming a major

How to cite this paper: Ch, A.B., Ravindra, J.V.R. and Lalkishore, K. (2015) Design of Ultra-Low Power PMOS and NMOS for Nano Scale VLSI Circuits. *Circuits and Systems*, **6**, 60-69. http://dx.doi.org/10.4236/cs.2015.63007

concern than the dynamic power. As the technology is going on scaling down, and we are now in 20 nm/15 nm/ 10 nm technology proper controlling of leakage power is becoming challenge factor.

Any power reduction techniques at device level will certainly lower the overall power consumption at system level (power reduction means it should be applicable from device level to system level, there is no guarantee that device level power reduction always applicable at system level) [2].

Related work: The existing numerous power reduction techniques in the field of VLSI are suitable for only 90 nm and above, but continuous scaling of the device in the present VLSI technology many of them may not be suitable. Moreover if the technique is suitable for power reduction than it fails for high speed, hence a new technique is required that is suitable for both power and speed [3].

Sources of power dissipations are

$$P_{\text{avg}} = P_{\text{static}} + P_{\text{dynamic}} + P_{\text{leakage}} + P_{\text{shortckt}}.$$

The major source in the overall power dissipation is the dynamic power

$$P_{\text{dynamic}} = \alpha \times V_{DD}^2 \times C_L \times f.$$

α = transition activity factor, V_{DD} = supply voltage, C_L = load capacitance, f = frequency of operation.

As the technology shrinks leakage power is to be dealt very carefully.

2. Taxonomy of Low Power

In **Figure 1** different power dissipation and power reduction techniques are clearly shown, all these techniques are applicable in low power design [4].

3. Problem Statement

Here an attempt has been made to control leakage power by proposed PMOS and NMOS, the fundamental limit of conventional PMOS and NMOS is higher leakage and lower sped in deep submicron technology sine power

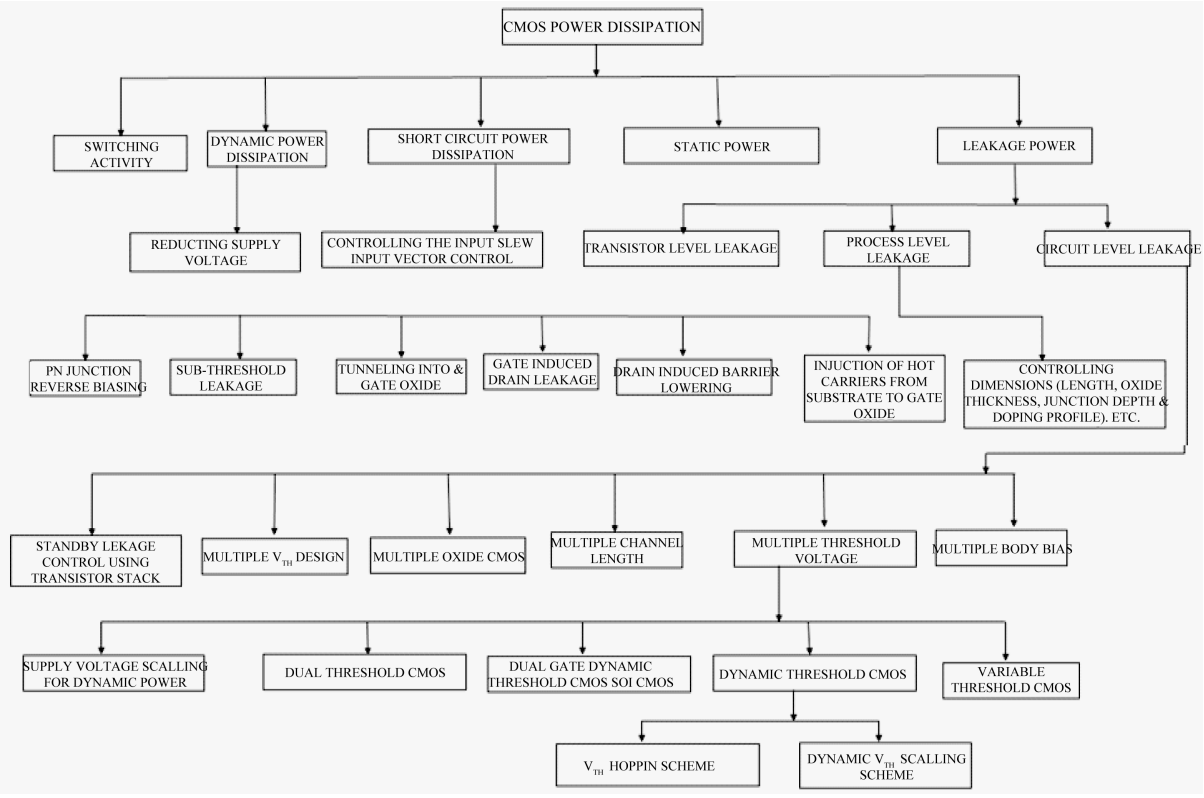

Figure 1. Taxonomy of low power.

supply reduction lowers three times the threshold voltage will degrade the speed of the circuit considerably, as we are striving forward to higher level of integration, area is not having that much of concern, now we are in position to keep millions of transistors in a single die, the other performance parameters like power, speed and delay moreover power delay product are important parameters which can decide the role of the device in nano scale regime [5]. In design abstraction we are approaching bottom up design as shown in the below **Figure 2**, basically CMOS device level analysis is done and comparative study is done among different MOS devices.

Demerits of Conventional PMOS & NMOS

Figure 3(a) and **Figure 3(b)** show the conventional PMOS and NMOS and having the following demerits.

- Lower speed.
- Higher leakage in deep submicron technology.

Figure 4 in DT PMOS and DT NMOS body is connected to gate terminal of the MOS device and as the gate voltage is changing body biasing takes place.

Working of proposed PMOS and NMOS: in **Figure 5** for top transistor (PM0) a reference voltage of 0.8 V is applied, and input is applied to the gate terminals of bottom transistor (PM2) and output is taken across the drain terminals of the right transistor (PM1) [6].

Both the conventional PMOS and NMOS, DT PMOS, DT NMOS and proposed PMOS and proposed NMOS are implemented using 45 nm technology and all are simulated using Cadence Virtuoso Design Environment and simulated and results are shown **Table 1**. From **Table 1** the proposed PMOS and NMOS have low PDP value.

Comparison table for the conventional PMOS and NMOS, DT PMOS, DT NMOS and proposed PMOS and proposed NMOS are implemented using 90 nm technology and all are simulated using Cadence Virtuoso Design Environment and simulated and results are shown **Table 2**.

Comparison table for the conventional PMOS and NMOS, DT PMOS, DT NMOS and proposed PMOS and proposed NMOS are implemented using 180 nm technology and all are simulated using Cadence Virtuoso Design Environment and simulated and results are shown **Table 3**.

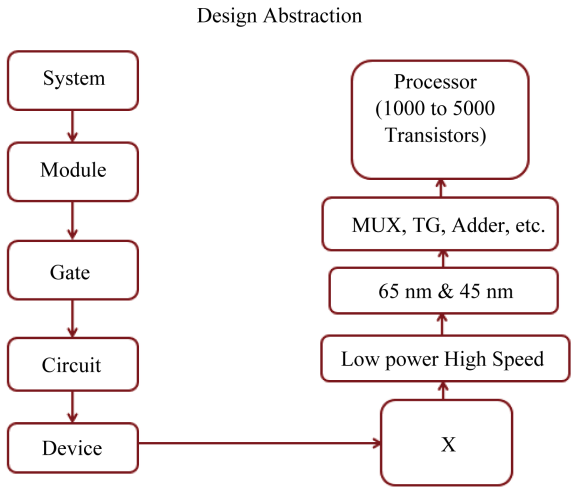

Figure 2. Design abstraction.

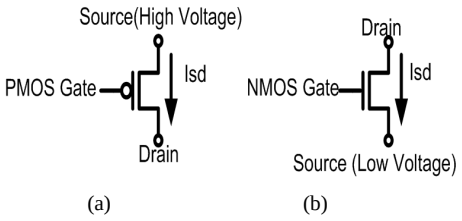

Figure 3. Conventional PMOS (a) & NMOS (b).

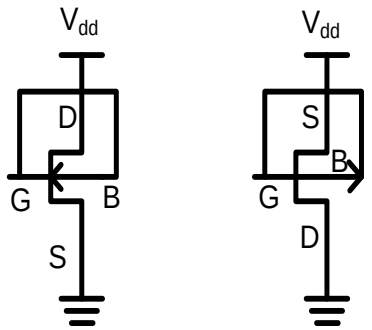

Figure 4. DT PMOS and DT NMOS.

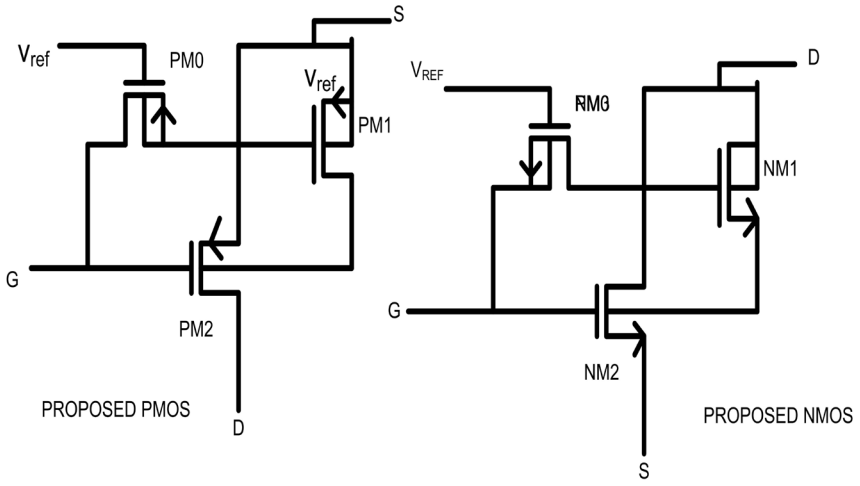

Figure 5. Proposed PMOS and NMOS.

Table 1. 45 technology.

Device	Output max value	Out min value	Avg. power	Delay	Static power		PDP
					V_{IN} = 0 V	V_{IN} = 1.1 V	
PMOS	1.1 V	0.323 V	5.37×10^{-9}	16 ps	116×19^{-15}	481×10^{-24}	8.59×10^{-20}
DTMOS	0.805 V	0.217 V	5.85×10^{-3}	4 ns	588×10^{-63}	11.26×10^{-3}	2.34×10^{-14}
NOVEL PMOS	1.1 V	0.250 V	1.71×10^{-9} V	4 ps	1.443×10^{-12}	822.5×10^{-15}	6.84×10^{-21}
NMOS	0.79	0	4.412×10^{-9}	13 ps	0	101.1×10^{-15}	5.73×10^{-20}
DTMOS	0.885 V	0.277 V	2.906×10^{-3}	4 ns	6.24×10^{-3}	48×10^{-27}	2.6154×10^{-14}
PROPOSED NMOS	0.818 V	0 V	6.29×10^{-9}	9 ps	151.8×10^{-15}	268.8×10^{-15}	5.661×10^{-20}

The PMOS and NMOS are good transfer of 1 and good transfer of 0, the comparative study is done on various types of MOS devices like PMOS, DTMOS and proposed MOS devices, the average power, delay and PDP is calculated by using the cadence virtuoso design environment tool for 45 nm, 90 nm, 180 nm technology [7].

4. Conventional CMOS Inverter

Figure 6 shows a conventional CMOS inverter which is simulated using Cadence Virtuoso Design tool and simulated outputs are shown in **Figure 7**, **Figure 8** shows CMOS output when all Zero's Applied and **Figure 9** shows CMOS output when All one's Applied.

Table 2. 90 nm technology.

Device	Output max value	Out min value	Avg. power	Delay	Static power		PDP
					V_{IN} = 0 V	V_{IN} = 1.1 V	
PMOS	1.2 V	0.233 V	13.26×10^{-9}	5 ps	1.3×10^{-15}	774×10^{-27}	663×10^{-20}
DTMOS	0.618 V	0.142 V	10.59×10^{-3}	6 ps	275.7×10^{-45}	20.28×10^{-3}	6.35×10^{-14}
NOVEL PMOS	1.2 V	0.158 V	10 nw	3 ns	15.60×10^{-15}	3.052×10^{-12}	3×10^{-17}
NMOS	1.08 V	0 V	8.245×10^{-9}	2 ns	1.404×10^{-24}	1.306×10^{-15}	1.6×10^{-17}
DTMOS	1.15 V	0.55 V	17.18×10^{-3}	4 ns	37.32×10^{-3}	959.1×10^{-30}	6.87×10^{-11}
PROPOSED NMOS	1.16 V	0 V	5.39×10^{-9}	0.0092 ns	45.24×10^{-12}	3.12×10^{-15}	4.3×10^{-21}

Table 3. 180 nm technology.

Device	Output max value	Out min value	Avg. power	Delay	Static power		PDP
					V_{IN} = 0 V	V_{IN} = 1.1 V	
PMOS	1.8 V	0.674	1.086×10^{-6}	0.1215 ns	23.46×10^{-15}	32.74×10^{-30}	2.25×10^{-6}
DTMOS	0.6182	0.2942	991.40×10^{-3}	40 ps	0	1.8×10^{-3}	3.96×10^{-11}
NOVEL PMOS	1.8 V	0.450 V	1.08×10^{-6}	10 ps	46.96×10^{-15}	23.46×10^{-15}	108×10^{-17}
NMOS	1.22 V	0 V	0.398×10^{-6}	5×10^{-3}	522.8×10^{-48}	467.7×10^{-18}	199×10^{-9}
DTMOS	1.54 V	1 V	37.69×10^{-3}	10 ns	81.7×10^{-3}	106.2×10^{-30}	3.769×10^{-10}
PROPOSED NMOS	1.435 V	0 V	1.08×10^{-6}	6 ps	487.7×10^{-18}	$935.3 \times {}^{10-18}$	648×10^{-18}

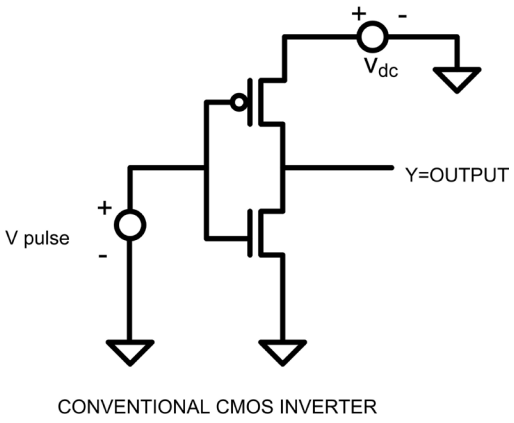

Figure 6. Conventional CMOS inverter.

5. Inverter with Proposed PMOS and NMOS

From the **Figure 10**, V_{dc} = 1.1 v and V_{ref} 0.8 v is applied to the transistors PM0 and NM3 and v_{in} = 0 v is applied to the transistors NM2 and PM2 PM2 becomes ON and NM2 becomes OFF, output will be 1 v, when v_{in} = 1 v applied to the transistors NM2 and PM2, NM2 ON and PM2 OFF output becomes 0 v [6]. And output results are shown in **Figures 11-13**.

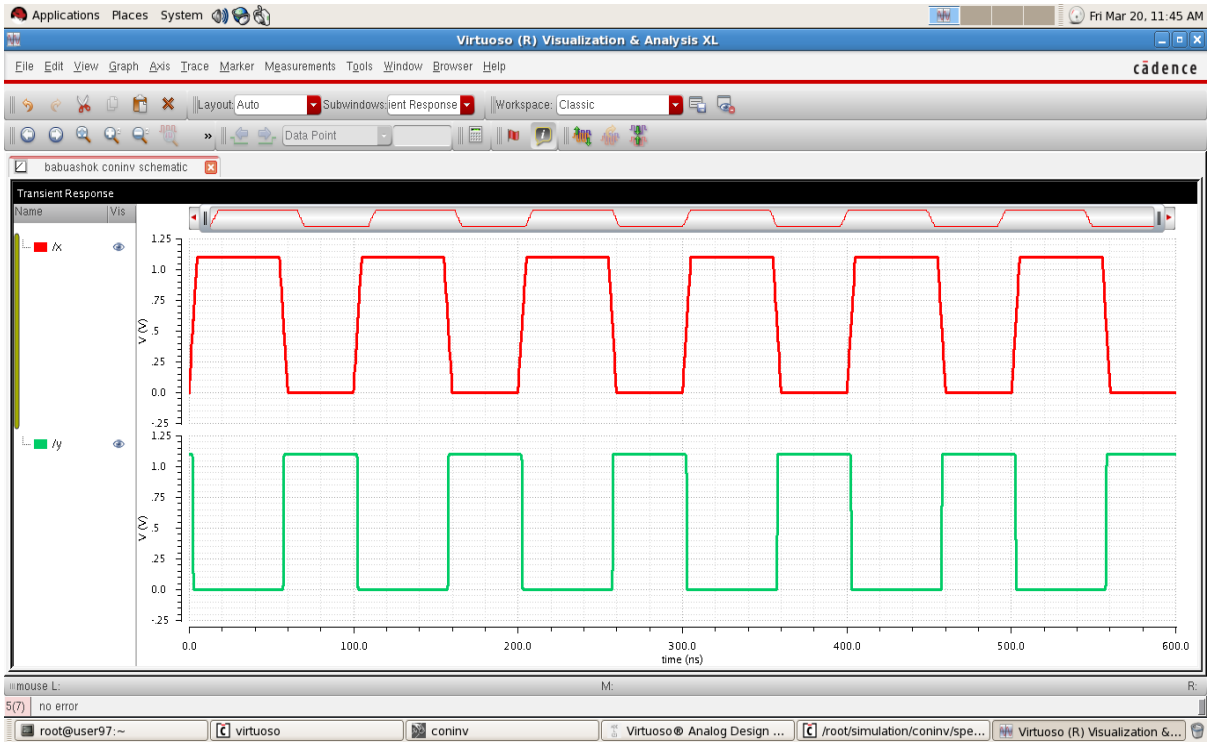

Figure 7. Conventional CMOS inverter output.

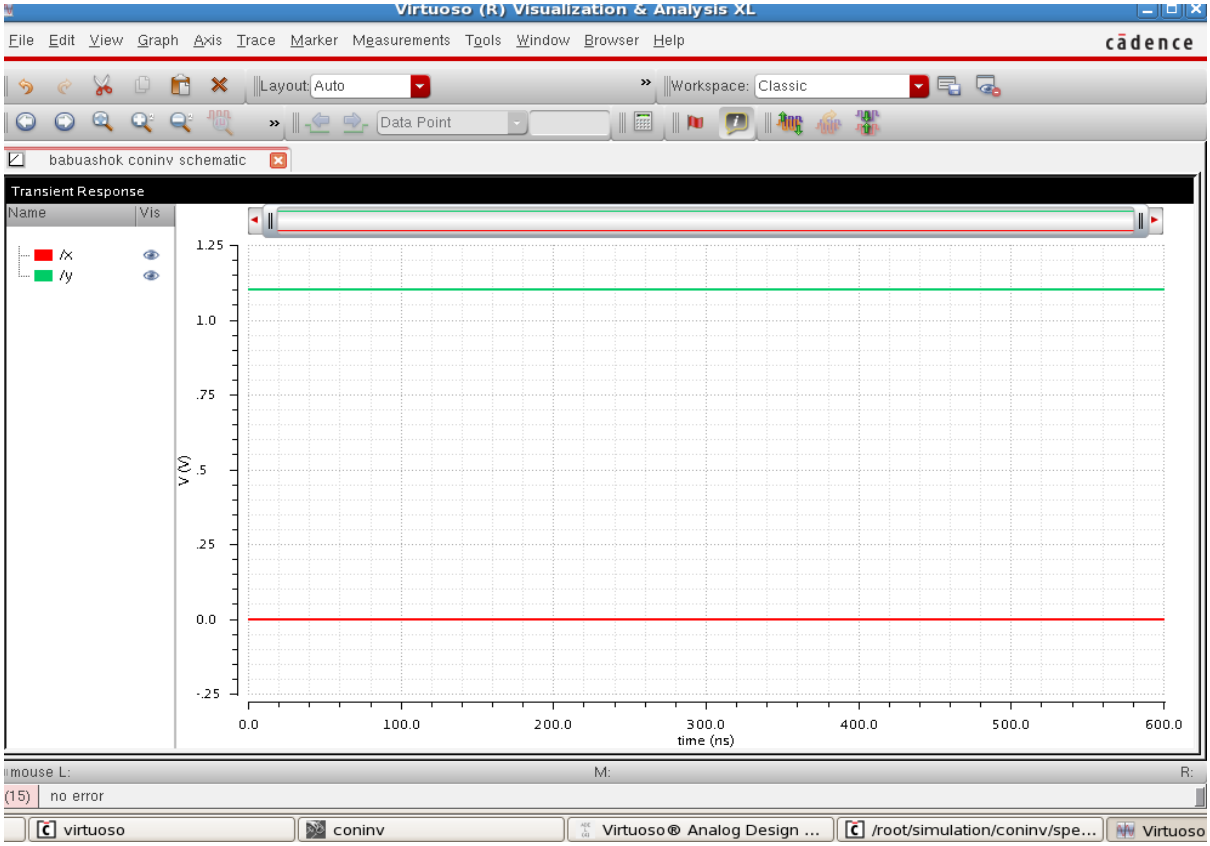

Figure 8. CMOS output when all zero's applied.

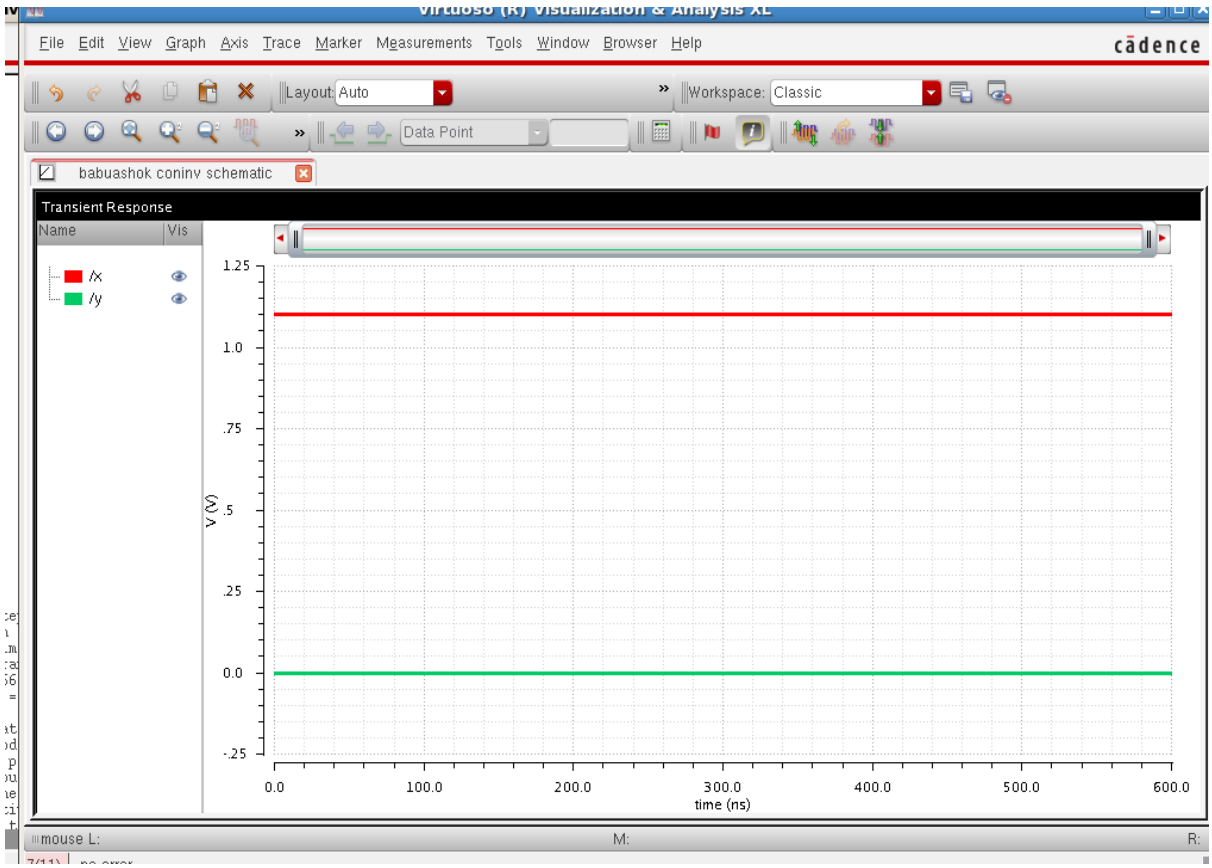

Figure 9. CMOS output when all one's applied.

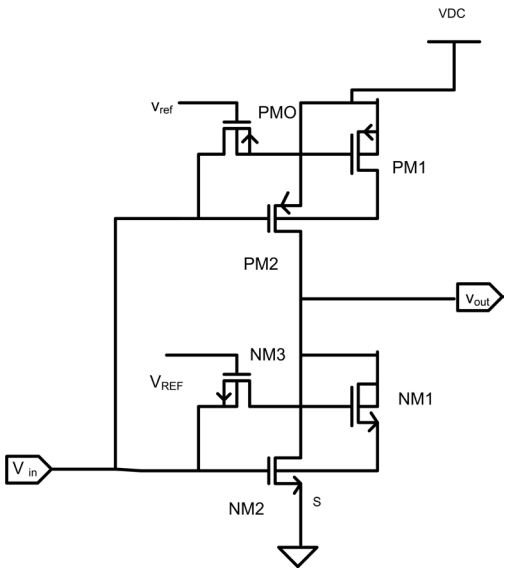

Figure 10. Proposed CMOS inverter.

There may be an area overhead but this circuit is certainly suitable for high speed and low leakage in deep submicron technology, as area is not a problem since we are in a position to keep millions of transistors in single die, performance parameters like speed will increase and leakage will decrease [9].

Hence an attempt has been made with proposed MOS devices to improve the performances.

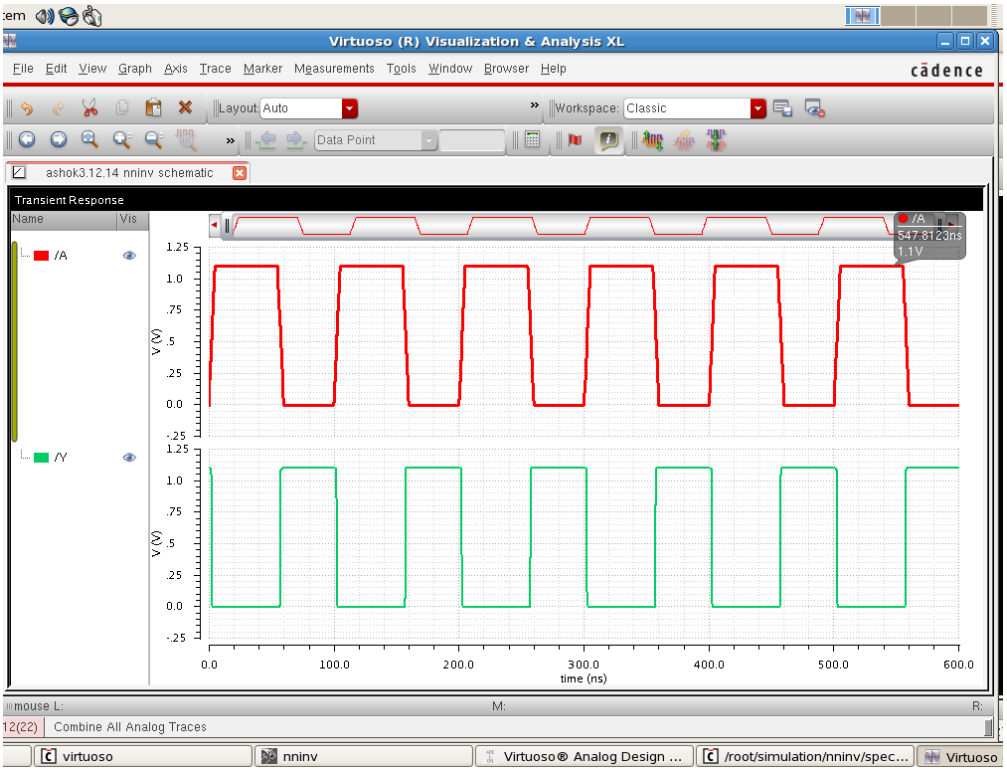

Figure 11. Proposed CMOS inverter output.

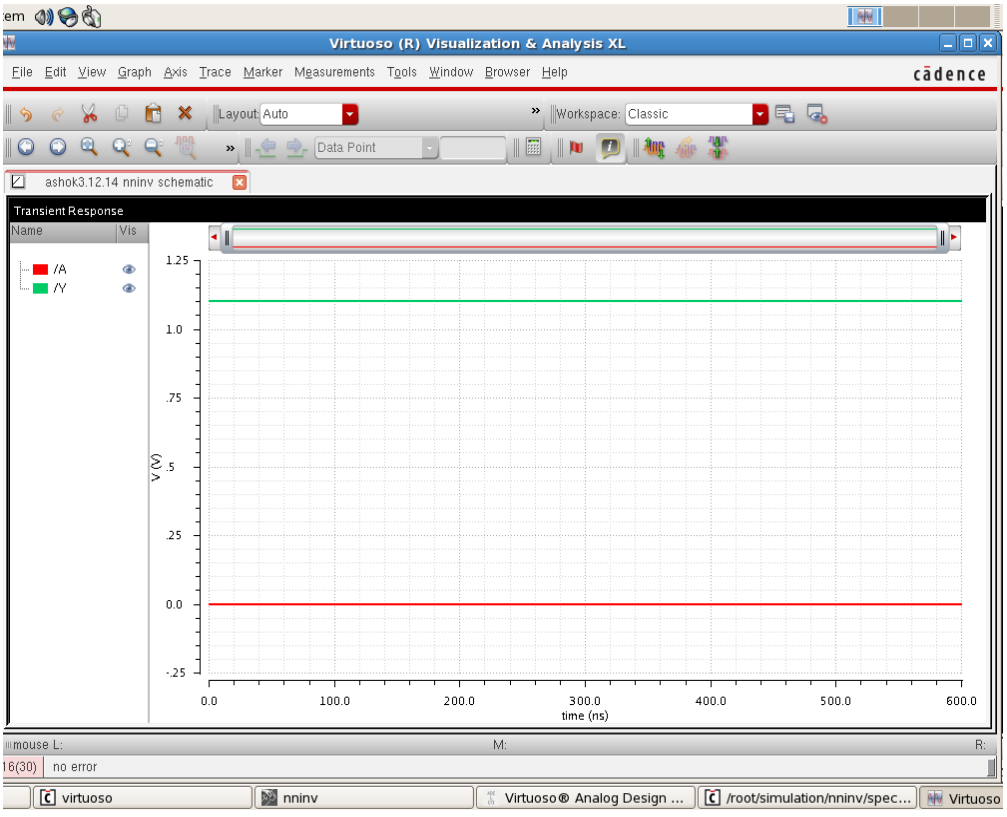

Figure 12. Proposed CMOS output for all zero's.

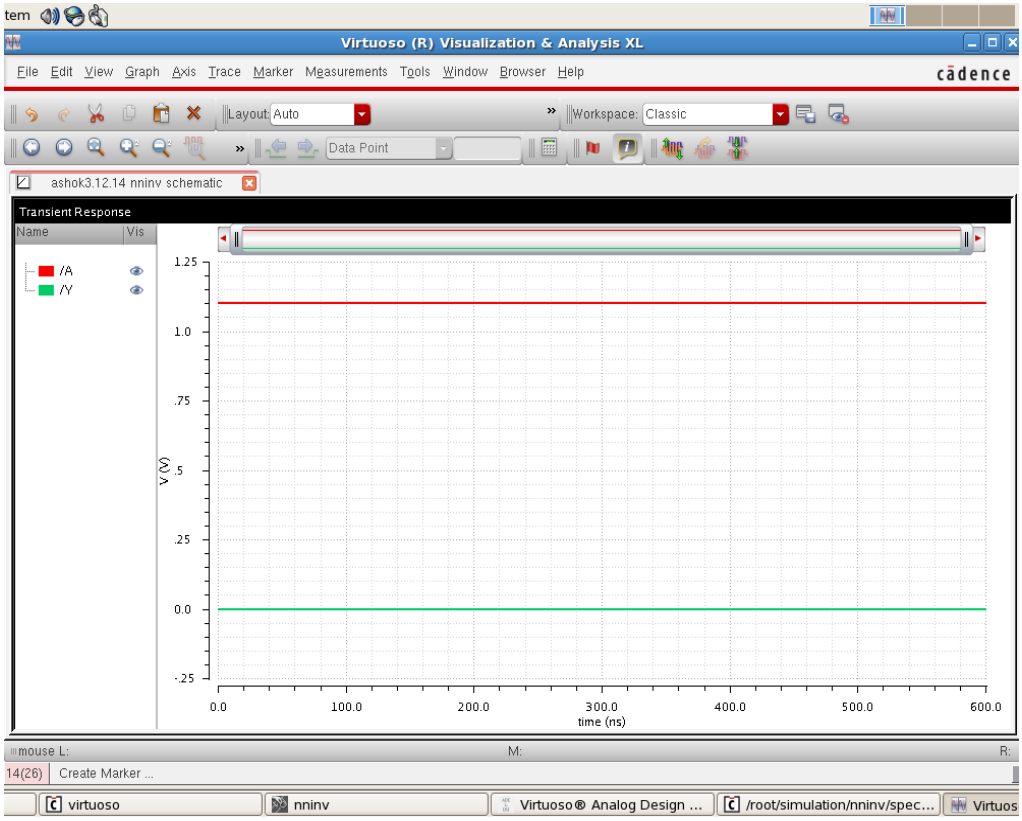

Figure 13. Proposed CMOS output for all one's.

6. Leakage Current Mechanism

Reverse biased junction leakage and subthreshold leakage have very much similar characteristics both will be in order of pico amperes per device and very sensitive to process variations. Leakage current cannot be ignored in deep submicron region and leakage current is the beyond the digital designer control [10]. In large scale high performance digital chips performing operations with high frequency. In ultra submicron region leakage power is playing a major contribution apart of dynamic power [11].

Subthreshold channel leakage: the subthreshold conduction current is given by $I_{sub} = I_0 e^{v_{gs} - v_t / \alpha v_{th}}$ where alpha is parameter depends on fabrication process v_{th} is the threshold voltage, v_{th} is the thermal voltage, even though a transistor is logically turned off there may be non zero leakage current through the channel this current is known as Subthreshold leakage current Since it occurs below threshold voltage [12].

7. Calculation of Leakage Power in CMOS Inverter and Proposed CMOS Inverter at 45 nm Technology

7.1. Normal CMOS Inverter Leakage Power

- Power: 6.937×10^{-9}, delay: 0.05×10^{-9}.
- When all ones applied power is 4.917×10^{-12}.
- When all zeros applied power is 5.018×10^{-12}.
- Total power for all ones and all zeros is $4.97 \times 10^{-12} + 5.018 \times 10^{-12} = 9.935 \times 10^{-12}$.
- Leakage power = $6.937 \times 10^{-9} - 9.935 \times 10^{-12} = 6927 \times 10^{-12}$.

7.2. Novel CMOS Inverter Leakage Power

- AVG power $P = 6.849 \times 10^{-9}$, delay = 0.18 ns.
- Power when all ones applied = 6.655×10^{-12}.

- Power when all zeros applied = 11.44×10^{-12}.
- All ones + all zeros power = $6.655 \times 10^{-12} + 11.44 \times 10^{-12} = 1.8095 \times 10^{-11}$.
- Leakage power = $6.849 \times 10^{-9} - 1.8095 \times 10^{-11} = 6830 \times 10^{-12}$ w.

The difference of leakage between conventional CMOS and Proposed CMOS power is

$$6927 \times 10^{-12} - 6830 \times 10^{-12} = 97 \times 10^{-12}.$$

8. Conclusion

We designed a Novel PMOS and NMOS which could give superior performance in deep submicron technology. The MOS devices like PMOS, DTMOS, and Novel MOS are studied and PDP is comparatively calculated. The leakage power is calculated for normal CMOS inverter and Novel CMOS inverter and it is observed that Novel CMOS inverter has less leakage power compared to Normal CMOS inverter. There may be area overhead but performance is better. It is concluded that Novel PMOS and NMOS are certainly suitable for low leakage and low power in ultra-deep submicron technology [13].

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