

Single VDVTA-Based Voltage-Mode Biquad Filter

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Received 19 February 2015; accepted 19 March 2015; published 20 March 2015

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Abstract

In this paper, an application of voltage differencing voltage transconductance amplifier (VDVTA) in the realization of voltage-mode (VM) multi-input single output (MISO) type biquad is presented. The proposed topology uses one VDVTA as an active element, two capacitors and a grounded resistor. The configuration realizes low pass (LP), high pass (HP), band pass (BP) and notch (BR) filters without the requirement of any matching condition. The natural frequency (ω_0) and bandwidth (BW) are independently controllable. The proposed circuit offers low active and passive sensitivities of ω_0 . The operation of the proposed circuit has been verified through SPICE simulation with TSMC CMOS 0.18 μm process parameters.

Keywords

Voltage Differencing Voltage Transconductance Amplifier, Analog Filter, LP, HP, BP, BR, Voltage Mode

1. Introduction

A number of VM MISO biquads utilizing different active elements have been proposed by the various researchers employing single active device [1]-[11]. MISO-type biquads are especially versatile because the same topology can be utilized through proper selection of input signal(s) to realize different filter functions. Such filters may be used in the implementation of touch tone telephone systems, FM stereo demodulators, phase locked loop etc. [12]. A number of new active elements have been presented in [13]. Recently Shaktour in [14] has used VDVTA in the formation of first order all pass (AP) filter. In this communication, we propose another applica-

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tion using single VDVTA for the realization of MISO-type biquad using three inputs and one output with two capacitors and one grounded resistor. The proposed circuit realizes four basic filter functions, namely LP, HP, BP and BR. In the case of LP filter, the structure enjoys an extra advantage of having both the capacitors grounded as preferred for integration point of view [15]. The circuit offers the advantage of independent control of ω_0 and $\frac{\omega_0}{Q_0}$. SPICE simulation results using TSMC CMOS 0.18 μm process and ± 0.9 V DC power supply voltages verify the theoretical prediction.

2. The Proposed Circuit Topology

The block diagram of the VDVTA is shown in **Figure 1**, where V_P , V_N and V are input terminals and Z , X^+ and X^- are output terminals. All terminals of VDVTA exhibit high impedance values [14]. The VDVTA can be characterised by the following terminal equations:

$$I_Z = g_{m_1} (V_{V_P} - V_{V_N}), \quad I_{X^+} = g_{m_2} (V_Z - V_V) \quad \text{and} \quad I_{X^-} = -g_{m_2} (V_Z - V_V). \quad (1)$$

The circuit analysis of **Figure 2** yields the following output equation in terms of input signals:

$$V_0 = \frac{s^2 V_3 + s \left(\frac{g_{m_2}}{C_2} \right) V_2 + \left(\frac{g_{m_1} g_{m_2}}{C_1 C_2} \right) V_1}{s^2 + s \left(\frac{\frac{1}{R_1} + g_{m_2}}{C_2} \right) + \left(\frac{g_{m_1} g_{m_2}}{C_1 C_2} \right)}. \quad (2)$$

Through proper selection of input signal(s) from Equation (2), **Figure 2** realizes the following filter functions:
 1) LPF; if $V_1 = V_{in}$ and $V_2 = V_3 = 0$ i.e.,

$$\frac{V_0(s)}{V_{in}(s)} = T_1(s) = \frac{g_{m_1} g_{m_2}}{C_1 C_2} \cdot D(s). \quad (3)$$

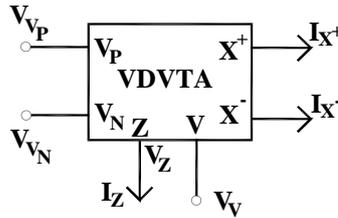


Figure 1. The symbolic notation of VDVTA.

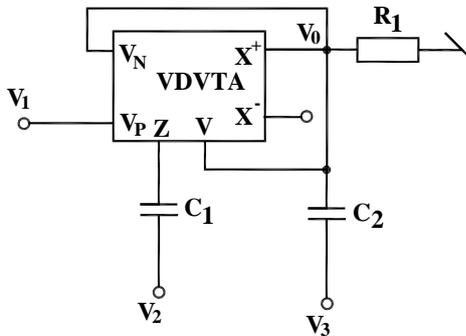


Figure 2. The proposed VM MISO-type configuration.

2) BPF; if $V_2 = V_{in}$ and $V_1 = V_3 = 0$ i.e.,

$$\frac{V_0(s)}{V_{in}(s)} = T_2(s) = \frac{s \left(\frac{g_{m_2}}{C_2} \right)}{D(s)}. \quad (4)$$

3) HPF; if $V_3 = V_{in}$ and $V_1 = V_2 = 0$ i.e.,

$$T_3(s) = \frac{V_0(s)}{V_{in}(s)} = \frac{S^2}{D(s)}. \quad (5)$$

4) BRF; if $V_1 = V_3 = V_{in}$ and $V_2 = 0$ i.e.,

$$T_4(s) = \frac{V_0(s)}{V_{in}(s)} = \frac{\left(S^2 + \frac{g_{m_1} g_{m_2}}{C_1 C_2} \right)}{D(s)} \quad (6)$$

from Equations (3)-(6), it is clear that there is no requirement of any matching condition.

Where

$$D(s) = s^2 + s \left(\frac{\frac{1}{R_1} + g_{m_2}}{C_2} \right) + \left(\frac{g_{m_1} g_{m_2}}{C_1 C_2} \right).$$

The natural frequency ω_0 , $BW = \left(\frac{\omega_0}{Q_0} \right)$ and quality factor Q_0 are given by:

$$\omega_0 = \sqrt{\frac{g_{m_1} g_{m_2}}{C_1 C_2}} \quad (7)$$

$$BW = \left(\frac{\frac{1}{R_1} + g_{m_2}}{C_2} \right) \quad (8)$$

$$Q_0 = \frac{\sqrt{\frac{g_{m_1} g_{m_2} C_2}{C_1 \left(\frac{1}{R_1} + g_{m_2} \right)^2}}}{\sqrt{C_1 \left(\frac{1}{R_1} + g_{m_2} \right)^2}} \quad (9)$$

The sensitivities of ω_0 with respect to passive components are found to be:

$$S_{g_{m_1}}^{\omega_0} = \frac{1}{2}, \quad S_{g_{m_2}}^{\omega_0} = \frac{1}{2}, \quad S_{C_1}^{\omega_0} = -\frac{1}{2}, \quad S_{C_2}^{\omega_0} = -\frac{1}{2}$$

which are all low.

3. Simulation Results

To verify the theoretical prediction, the proposed circuit was simulated using CMOS VDVTA (with minor changes as shown in **Figure 3**) from [16]. The passive components of the proposed circuit were selected as $C_1 = 0.02$ nF, $C_2 = 0.01$ nF and $R_1 = 100$ k Ω . The transconductances of VDVTA were controlled by bias currents. **Figure 4** shows the simulated filter responses of LP, BP, HP and BR. These simulation results, thus, confirm the validity of the MISO-type proposed biquad. The comparison of proposed biquad with other available MISO-type VM-biquads with a single active element is summarized in **Table 1**.

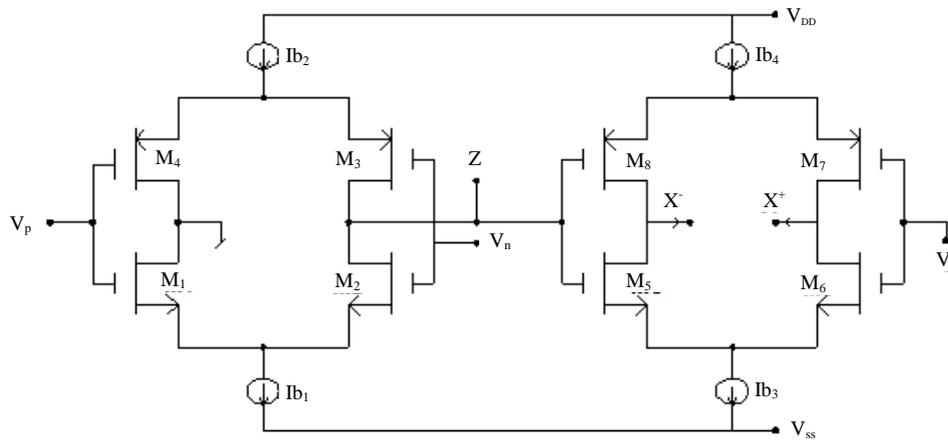


Figure 3. CMOS VDVTA [16].

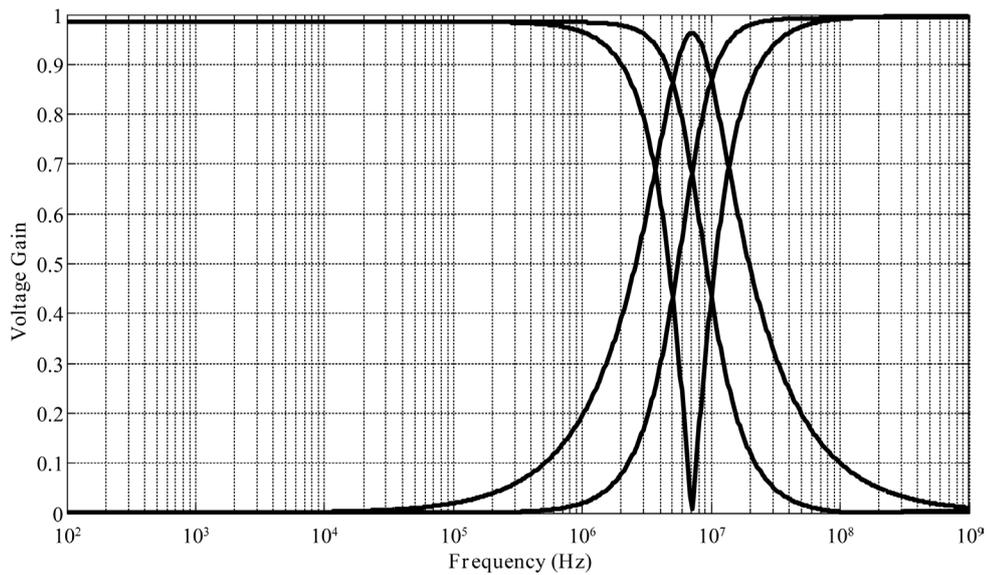


Figure 4. Frequency response.

Table 1. Comparison of proposed biquad with other available MISO-type VM-biquads using a single active device.

Reference	Number of resistors used	Number. of capacitors used	Whether all five filter functions are realized?	Requirement of matching conditions/constraints
[1]	3/2	2/3	No	No
[2]	5	2	No	Yes
[3]	1	2	Yes	No
[4]	2	2	Yes	Yes
[5]	3	2	Yes	Yes
[6]	4	4	Yes	Yes
[7]	2	2	Yes	Yes
[8]	2	2	Yes	Yes
[9]	2	2	Yes	Yes
[10]	2	2	No	No
[11]	3	2	No	Yes
Proposed	1	2	No	No

4. Conclusion

In this paper, an application of VDFTA is proposed in the form of VM-MISO-type biquad using three passive components. The proposed filter can realize the second-order LP, BP, HP and BR responses without changing the circuit topology and without any matching constraint(s). The LP filter response enjoys an additional advantage of having both the capacitors grounded as preferred for integration point of view [15]. The circuit offers low active and passive sensitivities. The SPICE simulation results using TSMC CMOS 0.18 μm process confirm the workability of the proposed structure.

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