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A Single Resistor Tunable Grounded Capacitor Dual-Input Differentiator

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Abstract

A new current feedback amplifier (CFA) based dual-input differentiator (DID) design with grounded capacitor is presented; its time constant (τ_o) is independently tunable by a single resistor. The proposed circuit yields a true DID function with ideal CFA devices. Analysis with nonideal devices having parasitic capacitance (C_p) shows extremely low but finite phase error (θ_e); suitable design θ_e could be minimized significantly. The design is practically active-insensitive relative to port mismatch errors (ε) of the active element. An allpass phase shifter circuit implementation is derived with slight modification of the differentiator. Satisfactory experimental results had been verified on typical wave processing and phase-selective filter design applications.

Keywords

CFA, Tunable Differentiator, Dual-Input Differentiator, Wave Shaper

1. Introduction

Differentiator and integrator functional blocks find a variety of applications in signal conditioning, wave processing and shaping, as process controller, phase compensator, and as pre-emphasis unit in radio engineering [1]. A high-quality (q) differentiator with true differential input capability is useful for enhanced signal handling characteristics. The literature shows a number of single-input differentiator circuit design schemes using various types of active building blocks, such as voltage operational amplifier (VOA) [2]-[4], current conveyor [5] and CFA [6]-[9].

A new grounded capacitor single resistor tunable true dual-input differentiator design using the CFA-844 building block is presented in this work. The CFA device is essentially a current mode element with improved

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features compared to the ubiquitous VOA [10]-[12]. The CFA provides unity current gain whereby both voltage-source and current-source output nodes are available such that cascadability for either type of signals is readily realizable. Other versatile properties [12]-[14] of the device relative to analog signal processing functional design, are improved slew-rate, accuracy and effective bandwidth that is nearly gain-independent. Since such a design is not yet reported, it therefore appears appropriate to propose a true dual-input high-***q*** differentiator circuit design based on the CFA device—leading to the motivation of this research work.

Analysis is carried out with both ideal and nonideal models of the device wherein the effects of the finite errors $\left(|\varepsilon| \ll 1\right)$ in port transfer ratios and parasitic shunt r_pC_p arms appearing at the current source *z*-node are examined. As per databook [15], typical values of these shunt components are in the range of $2\ \text{M}\Omega \le r_p \le 5\ \text{M}\Omega$ and $3\ \text{pF} \le C_p \le 6\ \text{pF}$ at $V_{cc} = 0 \pm 12$ V.d.c. Albeit effects of ε are seen to be insignificant that of the parasitics introduce finite phase error $\left(\theta_e\right)$ which tend to limit the higher side of the usable frequency range. By appropriate design of nominal passive components, the phase error could be minimized without affecting the single tunability feature. The nominal values of circuit resistors are chosen in $\text{K}\Omega$ range such that their ratios relative to r_p are extremely small, and hence may be neglected. The practical performance of the proposed DID had been verified satisfactorily with both PSPICE Macromodel [16] simulation and by hardware tests.

2. Analysis and Design

The CFA based proposed DID topology is shown in **Figure 1**. The nodal relations of the AD-844 CFA element is $I_z = \alpha I_x, V_x = \beta V_y, V_o = \delta V_z$ and $I_y = 0$; where α, β and δ denote the port transfer ratios. These are usually expressed by some small error $\left(|\varepsilon| \ll 1\right)$ terms [8] [17] as $\alpha \approx \left(1-\varepsilon_i\right), \beta \approx \left(1-\varepsilon_v\right)$ and $\delta \approx \left(1-\varepsilon_o\right)$. For an ideal device these errors vanish leading to unity transfer ratios. We now present the analysis of the DID circuit assuming $\varepsilon \ne 0$; the voltage transfer relation is

$$V_o = \left(\alpha_1\delta_1\alpha_2\beta_2\delta_2\right)\left(\beta_1 V_1 - V_2\right)sk\tau_o \tag{1}$$

where $k = R_1/R_2$ and $\tau_o = CR_o$. Writing $V_i \equiv \left(V_1 - V_2\right)$ and assuming ideal devices, we get the transfer from Equation (1) as

$$F \equiv V_o/V_i = sk\tau_o. \tag{2}$$

Note that no component matching constraint is needed to derive the transfer function in Equation (2) of the DID; time constant τ_o may be tuned independently by the grounded resistor (R_o) while additional variation may also be conveniently achieved by ratio-*k*. With nonideal devices, Equation (1) modifies to

$$V_o' = sk\tau_o'\left\{\left(1-\varepsilon_{v1}\right)V_1 - V_2\right\} \tag{3}$$

where $\tau_o'/\tau_o = \left(1-\varepsilon_t\right); \varepsilon_t \approx \left\{\varepsilon_{i1} + \varepsilon_{i2} + \varepsilon_{o1} + \varepsilon_{o2} + \varepsilon_{v2}\right\} \ll 1$. Also the noninverting input signal is slightly reduced by the factor $\left(1-\varepsilon_{v1}\right)$. Literature [8] [13] [17] indicates that error magnitudes are quite low in a typical range of $0.01 \le \varepsilon \le 0.04$, *i.e.*, hence V_1 input signal degeneration is negligible. The active sensitivity is $S^{\tau o} \approx \varepsilon/\left(1-\varepsilon_t\right) \ll 1$.

3. Effects of Parasitic Components

Re-examination of the circuit in **Figure 1**, assuming finite parasitic shunt— r_pC_p components at current source *z*-nodes of the CFAs, yields the following normalized transfer function

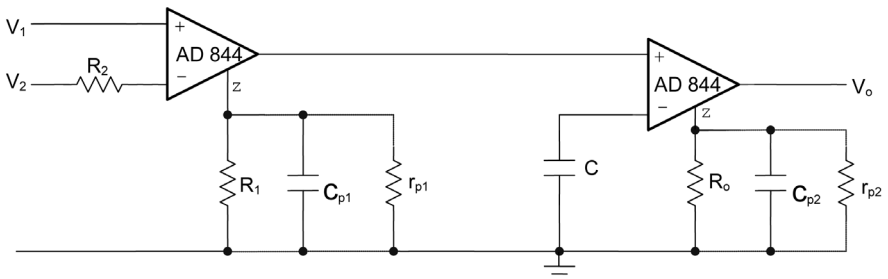


Figure 1. DID topology with grounded capacitor.

$$F'/F = \frac{1}{(1+\mu+s\tau_{p1})(1+\sigma+s\tau_{p2})} \tag{4}$$

where $\mu = R_1/r_1, \sigma = R_o/r_2, \tau_{p1} = R_1C_{p1}$ and $\tau_{p2} = R_oC_{p2}$. Since the ratios of nominal resistors with respect to parasitic ones are extremely low, these are neglected $(\mu, \sigma \ll 1)$. The total phase shift (θ) in frequency-response domain of the DID is therefore

$$\theta = 0.5\pi - \theta_e \tag{5}$$

where $\theta_e = \arctan u_1 + \arctan u_2$; $u_1 = \omega/\omega_{p1}$ and $u_2 = \omega/\omega_{p2}$ assuming $\omega_{p1,2} = 1/\tau_{p1,2}$. Values of parasitic capacitances are in pF range (say 4 - 5 pF) and nominal resistance values are in KΩ range (say 2 KΩ), by which we may estimate the higher end of usable frequency as $f_{p1} \approx f_{p2} \approx 20$ MHz.

The differentiator quality fator (q) is estimated by writing $F(j\omega) = A + jB$ which defines $q = B/A$. From Equation (4) we derive

$$q \approx (1-u^2)(\omega_{p1}/\omega)/\{1+(\omega_{p1}/\omega_{p2})\}. \tag{6}$$

Equation (6) may be simplified to obtain a practical value of q after assuming $u \ll 1$ and $\omega_{p1} \approx \omega_p \approx \omega_{p2}$; this yields $q \approx \omega_p/\omega \gg 1$. The proposed DID therefore offers high-quality feature within a stipulated frequency-range and the design is practically active-insensitive to port errors (ε).

4. Design Application

As an application of the differentiator, we now present the design of a first order allpass (AP) function realization. The differentiator circuit is slightly modified to derive the AP filter as shown in **Figure 2**; analysis shows constant gain-magnitude (H_o) with variable phase (ψ), given by

$$H(s) \equiv V_o/V_i = H_o[1-s\tau(\lambda-1)]/(1+s\tau) \tag{7}$$

where $\tau = RC$ and gain $H_o = R_2/R_1$; these parameters are independently tunable.

With $\lambda = 2$, one gets the non-minimum phase function $H(s) = H_o(1-s\tau)/(1+s\tau)$ which yields the phase

$$\psi = -2\arctan(\omega\tau); \quad 0 \le \psi(lag) \le \pi. \tag{8}$$

Effects of parasitic capacitances are examined next; re-analysis yields the modified transfer function as

$$H = \left\{\frac{H_0}{[(s/\omega_e)+1]}\right\}\left\{\frac{(s/\omega_\mu)^2 - as\tau + 1}{(s/\omega_\mu)^2 + bs\tau + 1}\right\} \tag{9}$$

where $\omega_e = 1/R_2C_{p2}$, $\omega_\mu = 1/R\sqrt{(2C_{p1}C)}$, $a = 1-(2C_{p1}/C)$ and $b = 1+(2C_{p1}/C)$. Thus even with finite parasitic capacitances, the circuit provides a non-minimum phase function. Since $C_{p1,2} \ll C$, we get $a = 1 = b$,

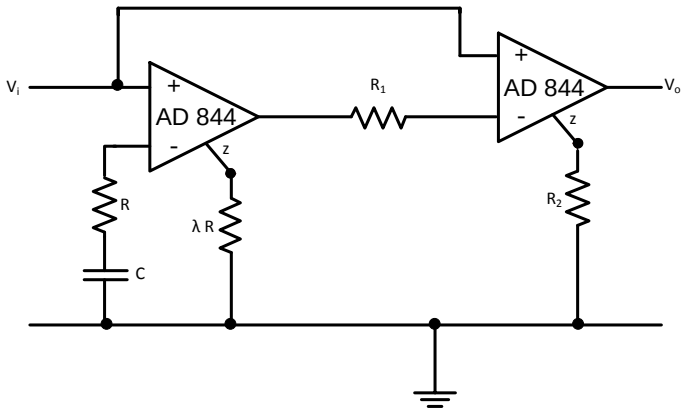


Figure 2. AP filter design.

hence the phase components of numerator and denominator polynomials in Equation (9) are symmetrical. Writing $\eta = \omega/\omega_\mu \ll 1$ and $\omega/\omega_e \ll 1$, we get the slightly altered phase response as

$$\psi' = -\arctan(\omega/\omega_e) - 2\arctan\left\{(\omega\tau)/(1-\eta^2)\right\} \approx \psi. \quad (10)$$

The phase response is therefore tunable in the nominal range and is seen to be practically unaffected by $C_{p1,2}$. The flat-gain is slightly attenuated at higher frequencies due to the parasitic pole at ω_{p2} which may extend upto about 20 MHz as discussed in the earlier section.

5. Experimental Results

Practical responses of both the DID and phase-selective AP filter had been measured using hardware circuit design employing readily available AD-844 type CFA device, and by PSPICE macromodel simulation; these are shown in **Figure 3**. The DID is tested in time-domain by applying equal but antiphase triangular-wave input signals while its phase-response is observed in frequency-domain, so as to measure θ_e at appropriately chosen values of CR_o; these are shown in **Figure 3(a)** and **Figure 3(b)**. The common mode characteristics of the DID is observed by applying equal amplitude sinusoid inputs while the CMRR had been measured experimentally as equal to 55 dB at 100 KHz and 48 dB at 1 MHz; deviation of the CMRR at higher end of frequency is owing to the noise accentuation property [1] [18] of differentiation function. Measured test response of the AP filter in **Figure 3(c)** indicates a phase deviation of $\psi_e \approx 1.8^\circ$ only at the select frequency of 500 KHz.

Next error estimation is carried out on the magnitude response of the DID for triangular to square wave conversion; these are listed in **Table 1** below which shows error on measured output voltage as $V_e \le 5\%$ with τ_o being independently tuned by R_o.

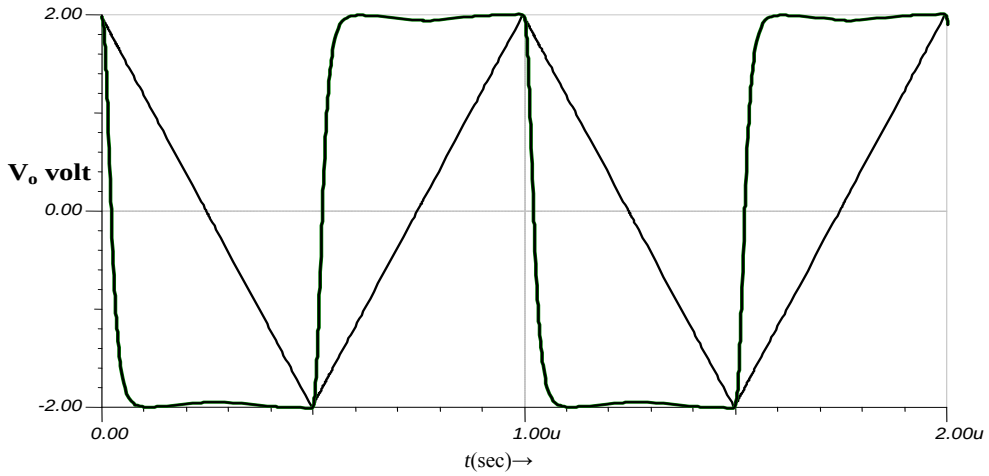
6. Conclusion

A new CFA based dual-input high-quality active dual-input differentiator (DID) circuit realization scheme is presented. The advantages of the proposed design are true differentiation function implementation using a grounded capacitor while the time constant is tunable by a single resistor—features suitable for microminiaturization. The gain factor of the circuit may also be conveniently adjusted by a resistor ratio. CFA-based DID design is not readily available in the literature. Such dual-input differentiators are conveniently used as the error-subtractor cum rate controller in a process control loop. All the tunability features of the DID here are independently controllable without requiring any component matching constraint. Analysis with nonideal devices has been carried out which exhibits practically active-insensitive nature of the design. Investigation assuming finite device parasitic indicates certain phase deviation $(\theta_e \le 4.8^\circ)$ at higher ends of usable frequency range of about 1 MHz. The proposed DID structure is utilized here in the design of a first-order phase-selective allpass function with high input impedance. The phase variation is in the range of $0 \le \psi(lag) \le \pi$ which is tunable by a resistor at constant gain magnitude (H_o) adjustable by another resistor ratio. Test response indicates a phase deviation of

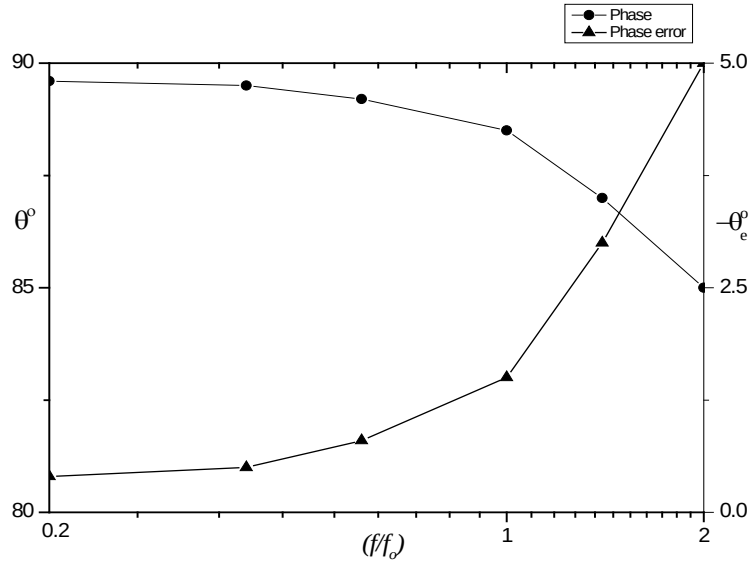
Table 1. Measured response of DID for error (%V_e) estimation.

$\tau_o = CR_o$ (μs)		Square-wave V_{opp} (volt)			%V_e	
R_o (KΩ)						
	C = 100 pF	Theoretical	Hardware	Simulation	Hardware	Simulation
1.0	0.10	1.6	1.53	1.55	4.3	3.1
1.5	0.15	2.4	2.36	2.35	1.7	2.1
2.0	0.20	3.2	3.10	3.05	3.1	4.6
2.5	0.25	4.0	3.80	3.90	5.0	2.5
3.0	0.30	4.8	4.70	4.75	2.1	1.1
3.5	0.35	5.6	5.40	5.50	3.5	1.8

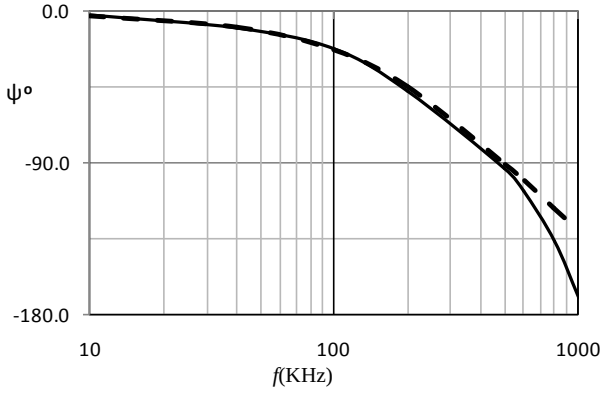
Anti-phase triangular wave input signals $V_1 = -V_2 = 2$ volt(pp) at 1 MHz with $k = 1$.



(a)



(b)



(c)

Figure 3. Responses of DID and AP filter. (a) Triangular wave to output square wave (V_o) conversion with antiphase input signals $V_1 = -V_2 = 2$ $V(pp)$ at $f = 1$ MHz and $C = 100$ pF, $R_o = 2.5$ KΩ, $k = 1$; $f_o = 0.16/CR_o$; (b) DID phase response; (c) AP phase response tested with $R = 2$ KΩ, $C = 160$ pF, $\lambda = 2$, $C = 160$ pF, $C_p \approx 5.7$ pF (measured) and $H_o = 1$; dotted curve: theoretical; solid curve: practical.

$\psi_e \approx 1.8^\circ$ due to the device parasitics at the select frequency of 500 KHz. All these responses have been verified experimentally.

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