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A New Structure of Multilevel Inverter with Reduced Number of Switches for Electric Vehicle Applications

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Abstract

Both Hybrid Electric Vehicles (HEVs) and Electric Vehicles (EVs) need a traction motor and a power inverter to drive the traction motor. The requirements for the power inverter include high peak power, optimum consumption of energy, low output harmonics and inexpensive circuit. In this paper, a new structure of multilevel inverter with reduced number of switches is proposed for electric vehicle applications. It consists of an H-bridge and an inverter in each phase which produces multilevel voltage by switching the dc voltage sources in series. As the number of switches are reduced, both conduction and switching losses will be decreased, which leads to increase the efficiency of converter. The size and power consumption of driving circuits are also reduced. The proposed three phase inverter can produces more number of voltage levels in the same number of the voltage source and reduced number of switches compared to the conventional inverters. This structure minimizes the total harmonic distortion (THD) of the output voltage waveforms. The structure of proposed multilevel inverter, modulation method, switching losses, THD calculation and simulation results with PSCAD/EMTDC software are shown in this paper.

Keywords: Cascaded H-Bridge, Electric Vehicles (EVs), Hybrid Modulation, Inverters, Traction Motors

1. Introduction

During the past few years, power electronic engineers have paid great attention to multilevel inverters as a new kind of power converter. Multilevel inverters can be divided into three remarkable topologies: diode- clamped [1-3], flying capacitors [4], and cascade H-bridge cells with separate dc sources [5-8]. The basic motivation for the use of these multilevel inverters is the reduction of voltage stress on the switching devices.

Multilevel inverters are used to drive many electrical machines such as EVs and HEVs [9-11]. The main advantages of using multilevel converters for the main traction drive in EVs include:

1) They are suitable for large VA-rated motor drives, and traditional 230 V or 460 V motors can be used.

2) Higher efficiency is expected for these multilevel converter systems because higher voltages can be utilized and the switching frequency of the devices is at a minimum.

3) Low voltage switching devices can be used.

4) No electromagnetic interference (EMI) problem or common-mode voltage/current problem exists.

5) No charge unbalance problem results from either charge mode or drive mode.

Development of the electric drive trains for these large vehicles will result in increased fuel efficiency, lower emissions, and likely better vehicle performance (acceleration and braking). One of the important issues in the mentioned machines is optimum consumption of energy. For this reason, power consumption of driving circuits of machines driving inverter should be reduced. On the other hand, when inverter switches sustain high voltage, their switching frequency is restricted. In this state, the output waveform of inverter is distorted and the reliability of the motor is reduced. Therefore, in order to overcome to the problem, voltage of switches must be decreased.

There are several methods to reduce the devise voltage. One of them is dc-dc converters, which divides the voltage by the capacitors connected in series [12]. For instance, in this method, when three capacitors are connected in series, the voltage of each capacitor becomes one third. The other method to reduce the devise voltage is cascade H-bridge (CHB) inverter, which increase the number of output voltage levels by increasing the num-

ber of H-bridges. In this method, when the number of output voltage levels is increased, the number of switches is also increased. Therefore, in two mentioned methods, increase of the number of output voltage levels makes both multilevel inverter and converter more complicated. Another method to reduce the voltage stress on the switching device that proposed recently is a multilevel inverter that uses dc voltage sources by switching them in series and in parallel [13].

In this paper, a new structure of multilevel inverter with reduced number of switches for electric vehicle applications is proposed. The proposed structure has been reduced the size and power consumption in the driving circuits. The same number of voltage sources is needed to output the same number of voltage levels compared to the conventional CHB inverters. Since, output voltage waveforms of inverter which are produced by switching the dc voltage sources in series by this conversion, the voltage of switches are decreased. Therefore, switching frequency is not restricted. Then, this inverter is best choice to use in high speed switching devices such as traction motor drives. The harmonics of the output voltage waveforms are also reduced. Capacitors, batteries, and other dc voltage sources can be used as the voltage sources of the proposed multilevel inverter.

2. Structure of the Proposed Multilevel Inverter

Figure 1 shows a single-phase structure of the proposed three phase multilevel inverter. As shown in **Figure 1**, each phase of inverter is constructed of two parts. Part one is an H-bridge with dc voltage source equal, V_0 and part two is inverter with dc voltage sources equal $V_k\ (k=1, 2, \cdots, n)$. DC voltage sources $V_0 \sim V_n$ are independent each other, and $V_0 : V_k = 1:2\left(k=1, 2, \cdots, n\right)$ is assumed. The voltage sources of part two can make using the manner of the switched capacitor. As a result, the $(k-1)$ number of voltage sources can be as capacitors. This means simple circuits are required in front of the multilevel inverter for the voltage sources. Switches $S_{a1} \sim S_{an-1}$ and $S_{b1} \sim S_{bm-1}$ are the switches that switching the dc voltage sources in series in each phase. The proposed inverter is driven by the hybrid modulation (HM) method [3,14].

Figure 2 shows the series conversion of the dc voltage sources of the proposed 15-level $(n=3)$ inverter in phase *a*. When the switch S_{b1} becomes ON, the current flows in the switch S_{b1}, which connect the voltage source V_1 to input of lower H-bridge (**Figure 2(a)**). As a result, the voltage V_{AB} between the point A and the point B in **Figure 2(a)** becomes $V_{AB}=V_1$. On the other hand, when the switches S_{a1} and S_{b2} become ON and the other switches become OFF, the current flows in switches S_{a1} and S_{b2}, which connect the voltage sources V_1 and V_2 in series and $V_{AB}=V_1+V_2$ (**Figure 2(b)**). Finally, when the switches S_{a1} and S_{a2} become ON and other switches become OFF, the current flow in switches S_{a1} and S_{a2}, which connect the voltage sources $V_1 \sim V_3$ in series and $V_{AB}=V_1+V_2+V_3$ (**Figure 2(c)**). Using this series conversion of dc voltage sources, the lower H-bridge outputs v_{bus2} in $2n+1$ levels, while the upper H-bridge outputs $v_{bus1}=V_0$. The each phase of the proposed multilevel inverter outputs $4n+3$ levels by $v_{bus1}+v_{bus2}$ or $v_{bus2}-v_{bus1}$.

If the conventional CHB inverter is driven by hybrid modulation method, then 12 switching devices are need for 11 levels, and 16 switching devices are needed for 15 levels [5]. But, the proposed inverter requires 10 devices for 11 levels and 12 devices for 15 levels. In addition, when the ratio of the voltage of the sources $V_0 : V_k = 1:3$ is assumed, the proposed inverter requires 10 devices for 15 levels and 12 devices for 21 levels. Therefore, the proposed inverter can increase the number of output voltage levels by changing the ratio of the voltage of the sources like conventional CHB inverter. Consequently, the more output levels make the larger difference between the required number of switching devices for proposed multilevel inverter and the conventional CHB inverter.

Then, the proposed inverter can be smaller than the conventional inverters. It leads to the simplicity in structure of inverter and also improved the reliability of system.

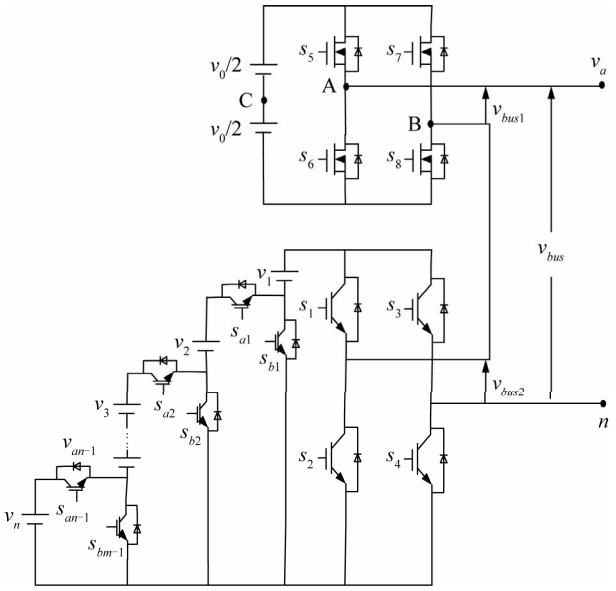


Figure 1. Single-phase structure of the proposed 4*n* + 3 levels inverter.

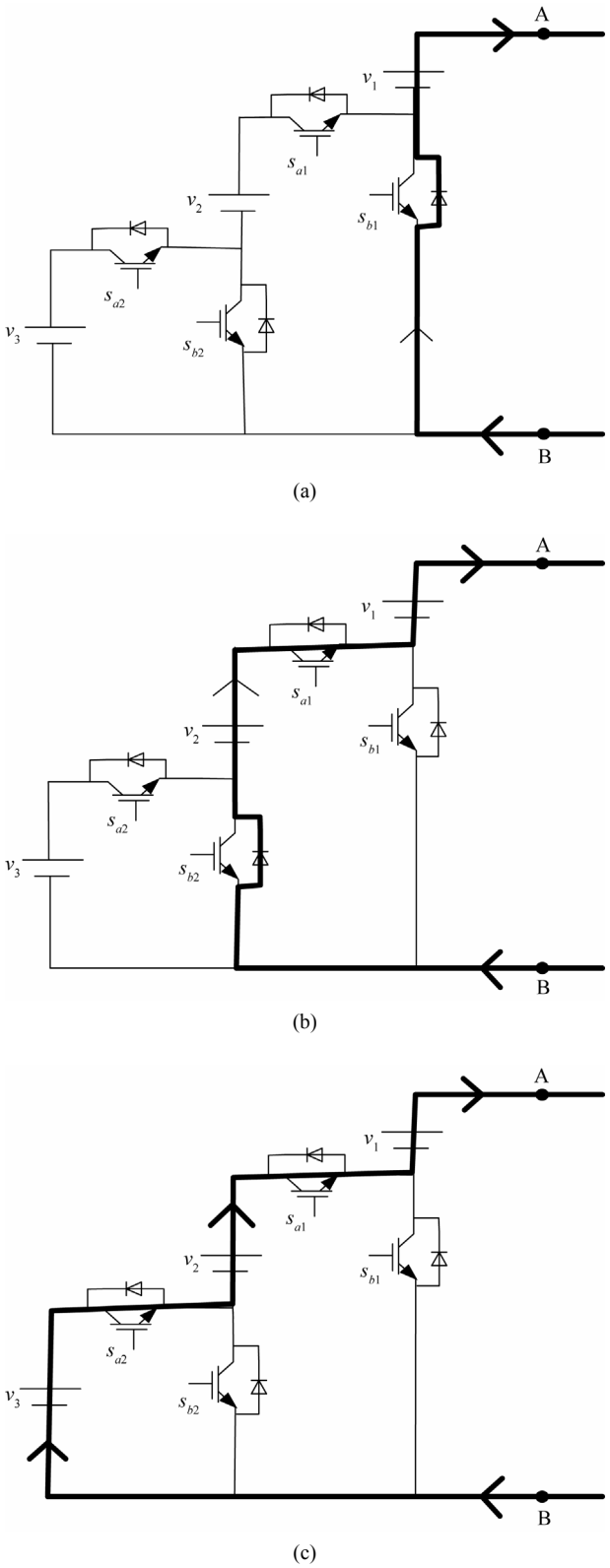


Figure 2. Current flow of the proposed 15-level inverter by series conversion, (a) V_1 connected via the switch S_{b1}; (b) V_1 and V_2 are connected in series; (c) V_1, V_2 and V_3 are connected in series.

For high power performance, the dc voltage sources can be switched in series and in parallel. For example, in this case, 14 switching devices are needed for 15 levels. In other conventional inverters such as Switched-Capacitor (SC) inverters a similar scheme that used in proposed inverter is also used [14]. However, the SC inverters require 28 switching devices for 11 levels and 36 switches for 15 levels. Therefore, the proposed multilevel inverter requires the less number of switching devices than Switched-capacitor inverters.

When the proposed inverter is applied to some application without reverse power flow, switches $S_{b1} \sim S_{bm-1}$ in each phase can be replaced by diodes. More number of the switching devices can be reduced in this case. For example, when a three phase resistive load is connected to the output of the proposed inverter, the output current phases are accorded with the voltage phases and directions of the currents don't become reverse to the power sources.

3. Modulation Method

In this section, the modulation method of the proposed inverter is explained on the 11-level inverter. **Figure 3** shows the modulation method of the proposed 11-level inverter. As shown in **Figure 3**, the upper H-bridge of proposed inverter is driven by pulse width modulation (PWM) method, while the lower H-bridge is driven by discontinuous reference waveform. **Figure 4** shows the bus voltage waveform when the proposed 11-level inverter is driven by the modulation method as shown in **Figure 3**.

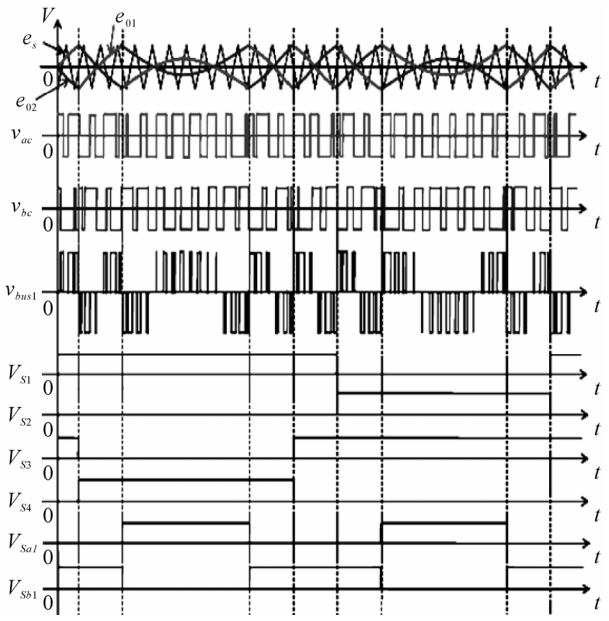


Figure 3. Modulation method of the proposed inverter.

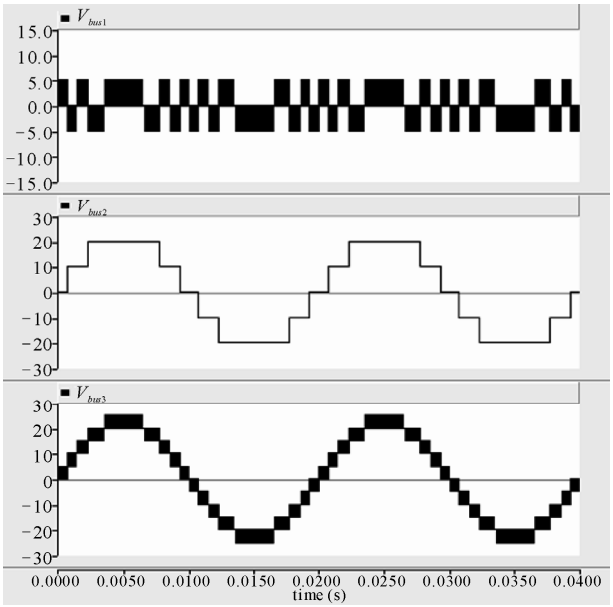


Figure 4. Voltage waveforms of the phase *a* bridge.

The reference waveform is made by cutting on the amplitude of the carrier waveform as shown in **Figure 5**. The carrier waveform used here, is a triangle waveform. The modulation index M is defined as,

$$M = A_{e0}/5A_{es} \tag{1}$$

where A_{e0} and A_{es} are the amplitude of the reference and the carrier waveforms, respectively. Switches S_5 and S_6 are driven by comparing the reference waveform e_{01} with the carrier waveform e_s. As a result, the voltage v_{ac} between the point A and the point C in **Figure 1** appears as shown in **Figure 3**. Switches S_7 and S_8 are driven by comparing the reference waveform e_{02} with the carrier waveform e_s. As a result, the voltage v_{bc} between the point B and the point C in **Figure 1** appears as shown in **Figure 3**. Therefore, as shown in **Figure 3**, the output voltage waveform of the upper H-bridge v_{bus1} can be obtained as:

$$v_{bus1} = v_{ac} - v_{bc} \tag{2}$$

Switches S_{a1}, S_{b1} and $S_1 \sim S_4$ are switched ON/OFF when the reference waveform e_{01} becomes discontinuous as shown in **Figure 3**. When S_{a1} is OFF, S_{b1} is ON, and S_1, S_4 are ON, the output voltage of the lower H-bridge v_{bus2} becomes:

$$v_{bus2} = V_1 = 2V_0 \tag{3}$$

When S_{a1} is ON, S_{b1} is OFF, and S_1, S_4 are ON, v_{bus2} becomes:

$$v_{bus2} = V_1 + V_2 = 4V_0 \tag{4}$$

When S_{a1} is OFF, S_{b1} is ON, and S_2, S_3 are ON, v_{bus2} becomes:

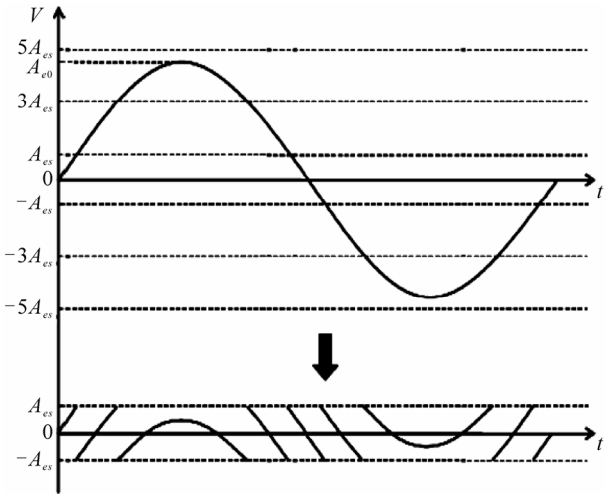


Figure 5. Reference waveform.

$$v_{bus2} = -V_1 = -2V_0 \tag{5}$$

When S_{a1} is ON, S_{b1} is OFF, and S_2, S_3 are ON, v_{bus2} becomes:

$$v_{bus2} = -(V_1 + V_2) = -4V_0 \tag{6}$$

Therefore, the output voltage waveform of the lower H-bridge v_{bus2} appears as shown in **Figure 4**. The proposed inverter outputs the 11-level voltage waveform by adding v_{bus1} and v_{bus2}.

4. Calculation of the Conduction and Switching Losses

The switching loss of each switching device is calculated from:

$$P_s = C_{ds}\, f_s\, V_s^2 \tag{7}$$

where C_{ds}, f_s, and V_s mean the capacitance of the switch, the frequency of the switch and the voltage of each switching devices, respectively. Therefore, for calculation of switching losses, both voltage and frequency of switches must be calculated.

The voltages of each device are different in proposed inverter. The voltages of the switches $S_{a1} \sim S_{an-1}$ in each phase during their OFF state are $V_{Sa1} \sim V_{San-1}$, which satisfy:

$$V_{Sa1} = V_{Sa2} = \cdots = V_{San-1} = \frac{2}{2n+1}\sum_{k=0}^{n} V_k \tag{8}$$

The voltage of these switches becomes smaller and smaller compared to the output voltage when the number of the levels is increased. The switching frequency of these switches is twice of the frequency of the reference waveform. The voltages of the switches $S_{b1} \sim S_{bm-1}$ in each phase during their OFF state are $V_{Sb1} \sim V_{Sbm-1}$,

which satisfy:

$$V_{Sbm-1} = \sum_{k=m+1}^{n} V_k,\ m = 1,2,\cdots,n \tag{9}$$

The voltages of the switches $S_1 \sim S_4$ during their OFF state are $V_{S1} \sim V_{S4}$, which satisfy:

$$V_{S1} = \cdots = V_{S4} = \sum_{k=1}^{n} V_k \tag{10}$$

The voltage of these switches becomes almost equal to the output voltage. On the other hand, the switching frequency of these switches becomes the same frequency of the reference waveform. Therefore, an IGBT is suitable for these switches. The voltages of the switches $S_5 \sim S_8$ during their OFF state are $V_{S5} \sim V_{S8}$, which satisfy:

$$V_{S5} = \cdots = V_{S8} = \frac{1}{2n+1}\sum_{k=1}^{n} V_k \tag{11}$$

The voltage of these switches becomes smaller and smaller compared to the output voltage when the number of the levels is increased. On the other hand, the switching frequency of these switches is the carrier frequency. Then, a MOSFET is suitable for these switches. Consequently, the voltage of the switches driven at high frequency is low.

The switching losses are calculated from following expressions. According to (7), the switching loss P_{S1} of the switches $S_{a1} \sim S_{an-1}$ and $S_{b1} \sim S_{bm-1}$ is:

$$P_{s1} = 16(m-1)C_{ds} f_{ref} V_0^2 + C_{ds} f_{ref}\left(\sum_{m+1}^{n} V_k\right)^2 \tag{12}$$

where f_{ref} mean the frequency of the reference waveform. The switching loss P_{S2} of the switches $S_1 \sim S_4$ is:

$$P_{s2} = 4C_{ds} f_{ref}\left(\sum_{k=1}^{n} V_k\right)^2 \tag{13}$$

The switching loss P_{S3} of the switches $S_5 \sim S_8$ is:

$$P_{s3} = 4C_{ds} f V_0^2 \tag{14}$$

where f means the frequency of the carrier waveform. Furthermore, when $V_1 \sim V_n$ are connected in series, the conduction loss P_{cser} is calculated from the following expression:

$$P_{cser} = 2R_{on}I^2 + (n+1)R_{ion}I^2 \tag{15}$$

In (15), R_{on}, R_{ion}, and I mean the internal resistance of MOSFET, the internal resistance of IGBT, and the current flowing in the switches. The first and the second terms express the conduction loss of the upper H-bridge, and the conduction loss of the lower H-bridge of proposed inverter, respectively.

The total conduction loss P_c is calculated from the following expression:

$$P_c = \sum_{k=1}^{n}\left[(n-k+3)R_{ion}I^2 + 2R_{on}I^2\right] - R_{ion}I^2 \tag{16}$$

In comparison of conventional multilevel inverters, both switching and conduction losses are decreased that this is important in EV applications. Especially, the mentioned losses are smaller than the losses of multilevel inverter that has a similar structure and use the dc voltage sources by switching them in series and in parallel.

5. Calculation of Total Harmonic Distortion

For calculation of the total harmonic distortion (THD) in the proposed multilevel inverter, the amplitude of the harmonics in the output voltage waveforms of the inverter must be calculated. For this case, sing Fourier analysis to calculate the amplitude of these harmonics. Based on **Figure 6**, the amplitude of the nth-harmonic in the 11-level output b_{11n} can be obtained as:

$$b_{11n} = \frac{2}{n\pi}\sum_{k=0}^{4}\left[\cos\left\{n\sin^{-1}\left(\frac{k}{5M}\right)\right\} - \cos\left\{n\pi - n\sin^{-1}\left(\frac{k}{5M}\right)\right\}\right] \tag{17}$$

The amplitude of the nth-harmonic in the 15-level output b_{15n} also can be obtained as:

$$b_{15n} = \frac{2}{n\pi}\sum_{k=0}^{6}\left[\cos\left\{n\sin^{-1}\left(\frac{k}{7M}\right)\right\} - \cos\left\{n\pi - n\sin^{-1}\left(\frac{k}{7M}\right)\right\}\right] \tag{18}$$

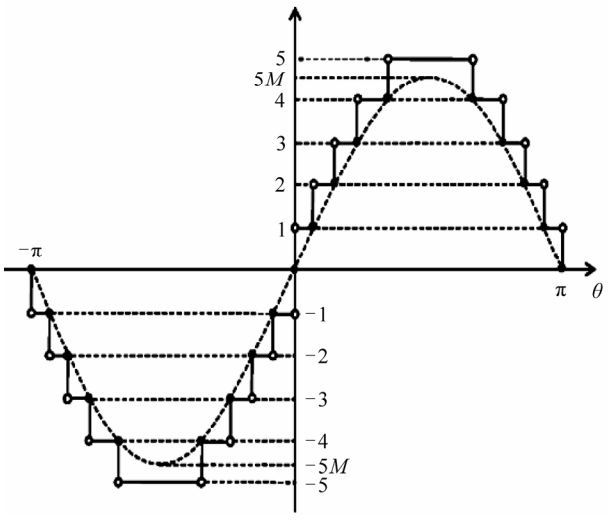


Figure 6. The output voltage waveform.

Table 1 shows the calculated (THD) in 11-level, 15-level and 23-level from expression (17) and (18) with the switching frequency equal 40 kHz. From Table 1, it is obvious that the more number of the voltage levels becomes the less quantity of THD.

6. Simulation Results

In this section, the simulation results of the 11-level and 15-level proposed multilevel inverter carried out using PSCAD/EMTDC is presented to verify the capabilities of the proposed topology in generating the desired output voltage. The condition of $V_0 = 5V$, $V_1 \sim V_n = 10$ V, M = 0.9, the internal resistance of MOSFET $R_{on} = 0.54\,\Omega$, and switching frequency f = 40 kHz are applied to proposed inverter.

Figure 7 shows the bus voltage waveforms of the proposed three phase 15-level inverter when the inverter fed an induction motor with two-pole 460-V 50-Hz 3-hp that used as traction motor in EVs. In addition, inverter one is loaded with $R = 50\,\Omega$ and the other one is loaded with an inductive load composed of $L_R = 2.5$ mH and $R = 50\,\Omega$ in series. **Figure 8** shows the bus voltage waveforms of the proposed 11-level and 15-level inverter for phase *a*. **Figure 9** shows the output voltage waveforms of the proposed 11-level and 15-level inverter when the filter inductance L and the filter capacitance *C* are $L = 560\,\mu\text{H}$ and $C = 0.5\,\mu\text{F}$. From **Figure 9**, the sinusoidal output voltage waveform is confirmed.

If the ideal switches are used, the amplitude of the proposed 11-level inverters output voltage waveform A_{11} becomes:

$$A_{11} = M\left(V_0 + V_1 + V_2\right) = 22.5[V] \tag{19}$$

The amplitude of the proposed 15-level inverters output voltage waveform A_{15} becomes:

$$A_{15} = M\left(V_0 + V_1 + V_2 + V_3\right) = 31.5[V] \tag{20}$$

From expressions (19), (20), and **Figure 9**, it is confirmed that the amplitude of calculated output voltage waveform in the simulation accorded with the theoretical amplitude.

Figure 10 shows the output voltage waveforms of the proposed 11-level and 15-level inverters when the inverter loaded with an inductive load composed of

Table 1. Comparision of the calculation THD.

The number of output voltage levels	THD [%]
11-level	4.57
15-level	3.50
23-level	2.70

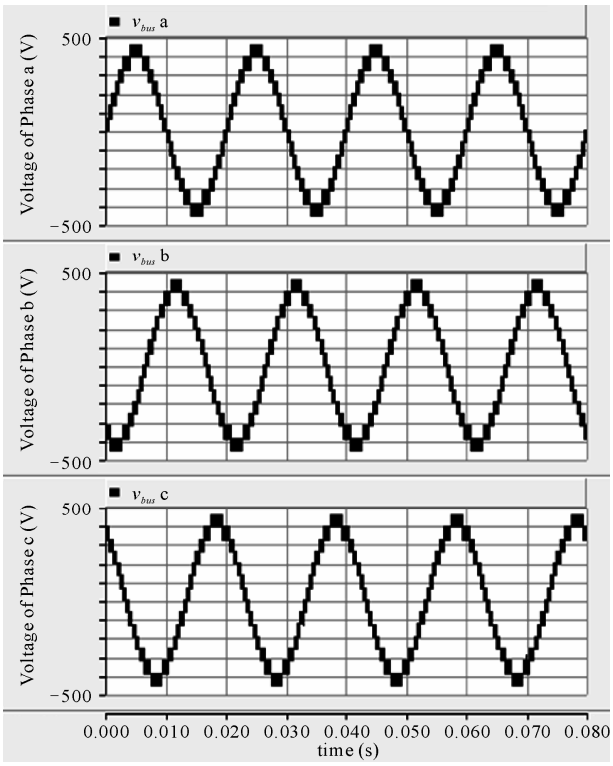
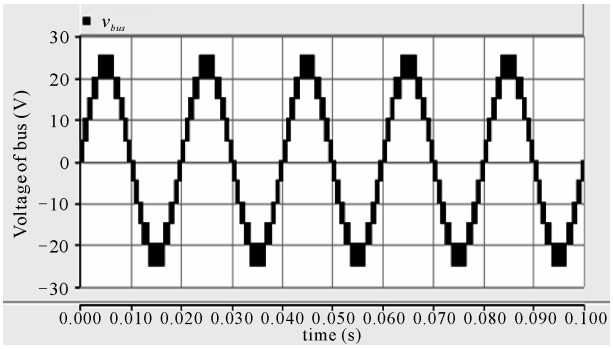
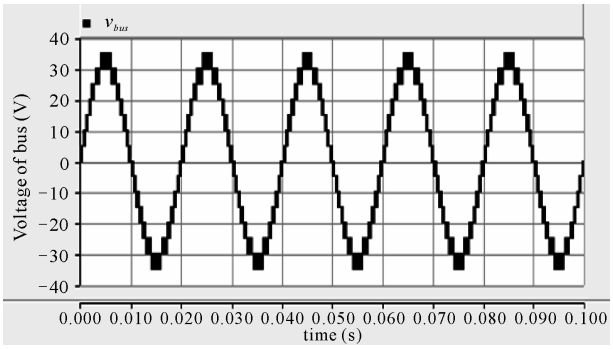


Figure 7. Three phase voltage waveforms of 15-level inverter fed induction motor.

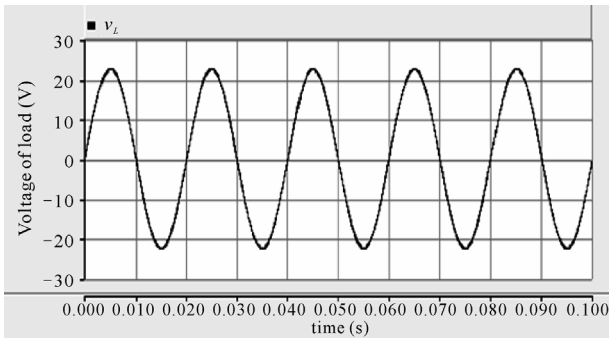


(a)

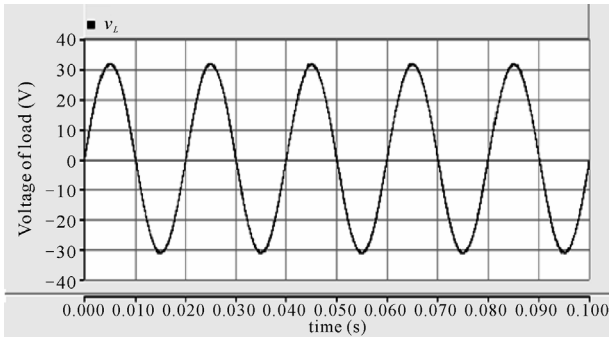


(b)

Figure 8. Calculated bus voltage waveform v_{bus} loaded with R, (a) 11-level; (b) 15-level.

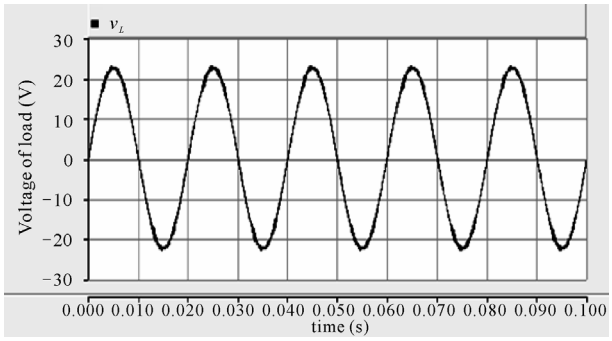


(a)

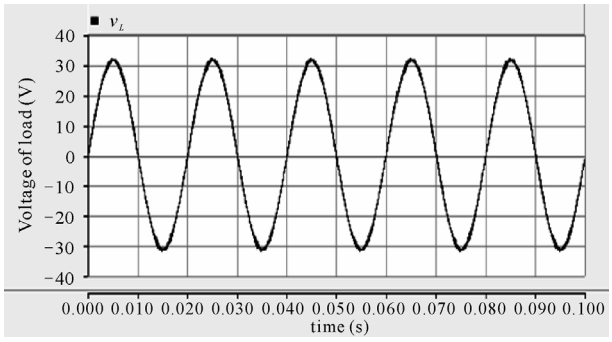


(b)

Figure 9. Calculated output voltage waveform v_{0ut} loaded with R, (a) 11-level; (b) 15-level.



(a)



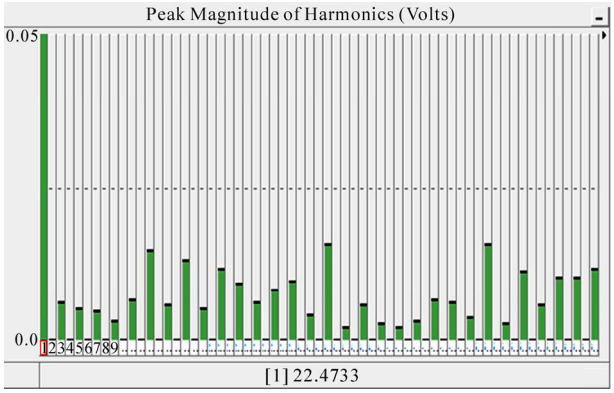
(b)

Figure 10. Calculated output voltage waveform v_{0ut} loaded with an inductive load, (a) 11-level; (b) 15-level.

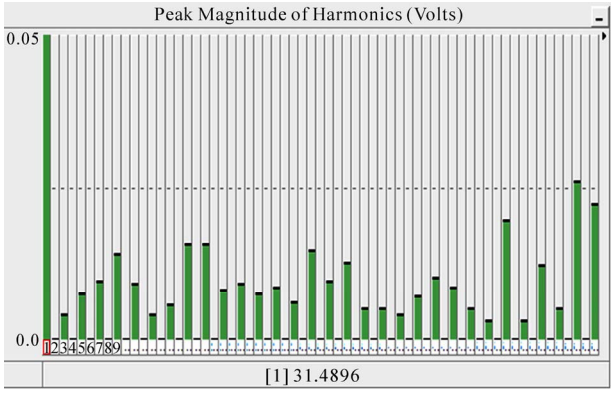
$L_R = 2.5$ mH and $R = 50\Omega$ in series. From Figure 10, the sinusoidal output voltage waveform is also confirmed. FFT analysis for both 11-level and 15-level bus voltage waveforms are shown in **Figure 11**. As shown in **Figure 11**, the amplitude of lower harmonics is very small.

7. Conclusions

A new structure of multilevel inverter with reduced number of switches for EV applications is proposed. The proposed inverter can produces more number of voltage levels in the same number of the voltage source and reduced number of switches compared to the conventional inverters. Therefore, the size and power consumption of driving circuits of inverter is reduced. The modulation method and the analysis of the harmonics in output voltage waveforms of inverter are shown. Both conduction and switching losses of proposed inverter are calculated. The proposed inverter can also reduce the THD of output voltage waveforms. In addition, since the inverter losses and voltage stress on the switching devices are low, the efficiency of proposed inverter becomes higher and switching frequency is not restricted. Therefore, this



(a)



(b)

Figure 11. FFT analysis for bus voltage waveforms v_{bus}, (a) 11-level; (b) 15-level.

inverter is best choice to use in high speed switching devices such as traction motor drives.

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