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A Scalable Model of the Substrate Network in *Deep N-Well* RF MOSFETs with Multiple Fingers

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Abstract

A novel scalable model of substrate components for *deep n-well* (*DNW*) RF MOSFETs with different number of fingers is presented for the first time. The test structure developed in [1] is employed to directly access the characteristics of the substrate to extract the different substrate components. A methodology is developed to directly extract the parameters for the substrate network from the measured data. By using the measured two-port data of a set of nMOSFETs with different number of fingers, with the *DNW* in grounded and float configuration, respectively, the parameters of the scalable substrate model are obtained. The method and the substrate model are further verified and validated by matching the measured and simulated output admittances. Excellent agreement up to 40 GHz for configurations in common-source has been achieved.

Keywords: *Deep N-Well* (*DNW*), RF Mosfets, Substrate Network, Scalable Model

1. Introduction

THE incorporation of a *Deep N-Well* (*DNW*) implantation into a standard CMOS technology has become a popular choice for reducing undesired interference in CMOS mixed-signal/RF SoC designs [2-6]. Substrate network parameters are of the utmost importance in accurately modeling the output admittance of RF MOSFETs. For mixed-signal/RF SoC design, a scalable model of RF MOSFETs is useful. Many papers have reported about scalable models of substrate network components [7-13]. However, there are few detailed works on scalable models with substrate network components in *DNW* RF MOSFETs with different number of fingers. In contrast to the RF MOSFET without *DNW* implantation (as seen from the nMOSFETs in **Figure 1**), the *DNW* actually partitions the substrate of a *DNW* RF MOSFET into three parts [1]: The *DNW* itself, the p-well in the *DNW*, and the original substrate where the *DNW* is formed. The *DNW* layer forms a capacitive coupling path in the substrate, which exists no matter what the electrical configuration is. Furthermore, most previous works [7-19] dealt with substrate parasitic effects in RF MOSFETs by using resistance networks only. The capacitive coupling effect, which is physically in existence, is always neglected. All of these make the previously reported substrate models less physically reasonable to use for accurately extracting the substrate network components of *DNW* RF MOSFETs.

In this paper, a compact, physically based substrate network is proposed targeted specifically at *DNW* RF MOSFET modeling. A novel test structure proposed in [1] is expanded and employed in deriving and extracting the N_f- dependent equations involving substrate components in multi-finger *DNW* RF MOSFETs. The geometric effects such as shallow trench isolation (STI), which have never been considered in previous reported works, are accurately modeled. The results show that the substrate components within the p-well and the capacitances caused by the *DNW* are strongly dependent on N_f, while the parasitic components in the original p-substrate have a slight dependence on N_f in multi-finger devices.

To verify the validity of the derived scalable model of the substrate network components, a macro-model consisting of the BSIM3v3.2 model core with the proposed substrate-network based on the extracted parameters, is simulated in Agilent Advanced Design System (ADS). Excellent agreement between the simulated and measured output admittance for a set of devices with different number of fingers up to 40 GHz validated the accuracy of the methodology proposed for *DNW* RF-MOSFET modeling in this paper.

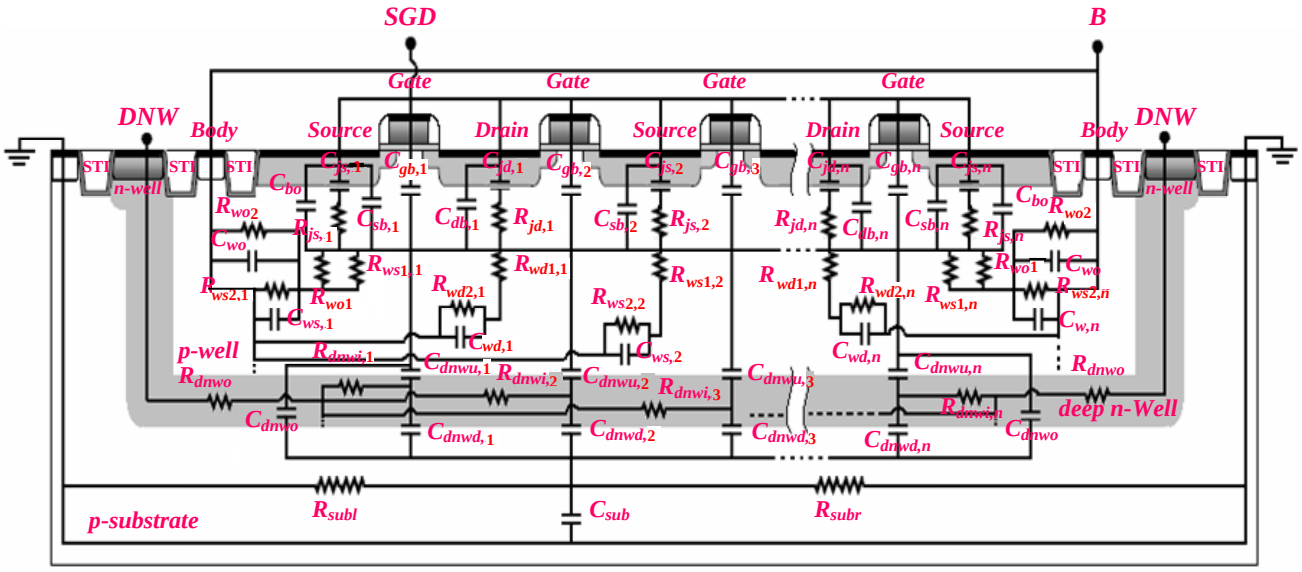


Figure 1. Equivalent circuit for the substrate resistance and capacitance networks of multi-finger (*Nf*) *DNW* RF MOSFET with all the source (*S*), drain (*D*) and gate (*G*) terminals for different fingers connected together. Source, drain, and gate resistances are ignored for their slight contribution to the output impedance.

2. Analysis of the Substrate Network and the Scalable Model Derivation

A multi-finger *DNW* RF MOSFET with the test configuration proposed in [1] is investigated. All of the source (*S*), drain (*D*) and gate (*G*) terminals for different fingers are connected together and used as port one, while the body (*B*) terminal is port two, and the p-substrate is grounded, for two-port measurement. **Figure 1** shows the substrate network when the junction diodes are turned off. In **Figure 1**, $C_{js,i}$, $C_{jd,i}$ are each *S/D* junction region capacitors, $R_{js,i}$, $R_{jd,i}$ are each *S/D* junction resistors. C_{dnwo}, which combined with C_{wo}, C_{bo}, R_{wo1}, R_{wo2} and R_{wo}, is used to capture the difference between the inner and outer *S/D* regions in this work. $C_{dnwu,i}$ and $C_{dnwd,i}$ represent the p-well-to-*DNW* and the *DNW*-to-p-substrate capacitors under each finger region. $C_{ws,i}$ and $C_{wd,i}$ are each finger capacitors from the bottom of the *S/D* regions to *B* within the *Deep N-Well*. $R_{ws1,i}$, $R_{wd1,i}$, $R_{ws2,i}$ and $R_{wd2,i}$ represent the single finger resistors between the bottom of the *S/D* region and *B*. $C_{sb,i}$, $C_{db,i}$ and $C_{gb,i}$ are the *S*-to-*B*, *G*-to-*B* and *D*-to-*B* capacitors of each finger region, R_{subl}, R_{subr} and C_{sub} are the capacitor and the resistor of the p-substrate, $R_{dnw,i}$ represent the resistors of the *DNW* under each finger region. R_{dnwo} represents the n-well ring resistor.

Based on the equivalent circuits identified in **Figure 1**, a simplified substrate network, as shown in **Figure 2**, with the following relationships can be obtained for any number of fingers:

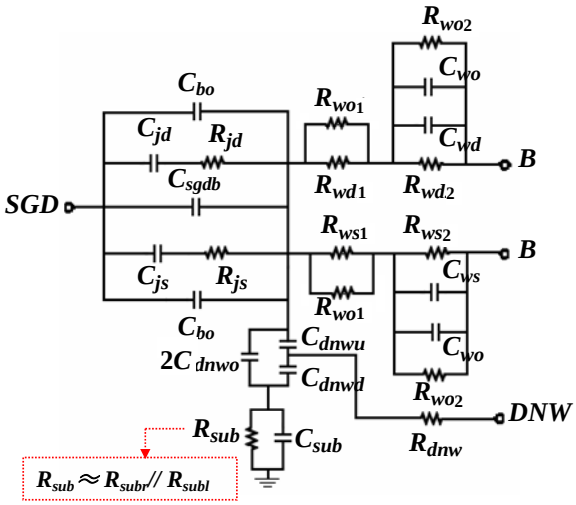


Figure 2. Equivalent circuit of multi-finger *DNW* RF MOSFETs with *S*/*G*/*D* terminals connected together.

$$C_{js/jd} = \sum_{i=1}^{N_{s/d}} C_{js/jd,i} \quad (1a)$$

$$R_{js/jd}^{-1} = \sum_{i=1}^{N_{s/d}} R_{js/jd,i}^{-1} \quad (1b)$$

$$C_{sgdb} = \sum_{i=1}^{N_f} \left[C_{sb,i} + C_{gb,i} + C_{db,i} \right] \quad (1c)$$

$$C_{ws/wd} = \sum_{i=1}^{N_{s/d}} C_{ws/wd,i} \quad (1d)$$

$$R_{ws1/wd1}^{-1} = \sum_{i=1}^{N_{s/d}} R_{ws1/wd1,i}^{-1} \quad (1e)$$

$$R_{sub}^{-1} = R_{subI}^{-1} + R_{subr}^{-1} \quad (1f)$$

$$R_{ws2/wd2}^{-1} = \sum_{i=1}^{N_{s/d}} R_{ws2/wd2,i}^{-1} \quad (1g)$$

$$C_{dnwu} = \sum_{i=1}^{N_f} \left[C_{dnwu,i} \right] \quad (1h)$$

$$C_{dnwd} = \sum_{i=1}^{N_f} \left[C_{dnwd,i} \right] \quad (1i)$$

$$R_{dnw} = 2R_{dnwo} + \left[\sum_{i=1}^{N_f} \left[R_{dnw,i}^{-1} \right] \right]^{-1} \quad (1j)$$

where, C_{js}, C_{jd} represent the total *S/D* junction region capacitances, R_{js}, R_{jd} represent the total *S/D* junction resistances, R_{sub} represents the total resistance of the p-substrate, C_{dnw} represents the total capacitance caused by the *DNW*, C_{ws}, C_{wd} are the total capacitances from the bottom of the *S/D* regions to *B* within the *Deep N-Well*, $R_{ws1/wd1}$ and $R_{ws2/wd2}$ are the total resistances between the bottom of the *S/D* regions and *B* within the *Deep N-Well* and N_s and N_d represent the numbers of source and drain diffusion regions, respectively. In the model, when the number fingers is odd, $N_s = N_d = (N_f + 1)/2$. $N_s = N_f/2 + 1$ and $N_d = N_f/2$ when the number of fingers is even.

Assuming that there are no differences in the inner *S/D* regions, the above equations, (1a)-(1h), can be formed as follows:

$$C_{js/jd} = N_{s/d} C_{j,i} \quad (2a)$$

$$R_{js/jd} = R_{j/i} / N_{s/d} \quad (2b)$$

$$C_{sgdb} = N_f \left[2C_{sdb,i} + C_{gb,i} \right] \quad (2c)$$

$$C_{ws/wd} = N_{s/d} C_{w,i} \quad (2d)$$

$$R_{ws1/wd1} = \frac{R_{w1,i}}{N_{s/d}} \quad (2e)$$

$$R_{ws2/wd2} = \frac{R_{w2,i}}{N_{s/d}} \quad (2f)$$

$$C_{dnwu} = N_f C_{dnwu,i} \quad (2g)$$

$$C_{dnwd} = N_f C_{dnwd,i} \quad (2h)$$

$$R_{dnw} = 2R_{dnwo} + \frac{R_{dnwi}}{N_f} \quad (2i)$$

where

$$C_{j,i} = C_{js,i} = C_{jd,i},\ R_{j,i} = R_{js,i} = R_{jd,i},\ C_{sdb} = C_{sb,i} = C_{db,i}$$

$$C_{w,i} = C_{ws,i} = C_{wd,i},\ R_{w1,i} = R_{ws1,i} = R_{wd1,i}$$

and $R_{w2,i} = R_{ws2,i} = R_{wd2,i}$.

In this paper, the following equations are used to empirically model the N_f- dependence of R_{sub} and C_{sub}:

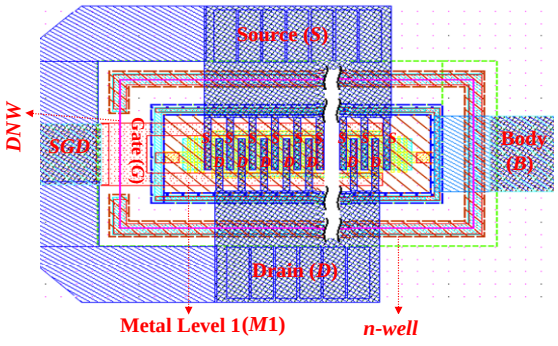
$$R_{sub} = R_{subI} + N_f R_{subunit} \quad (2j)$$

$$C_{sub} = C_{subI} + N_f C_{subunit} \quad (2k)$$

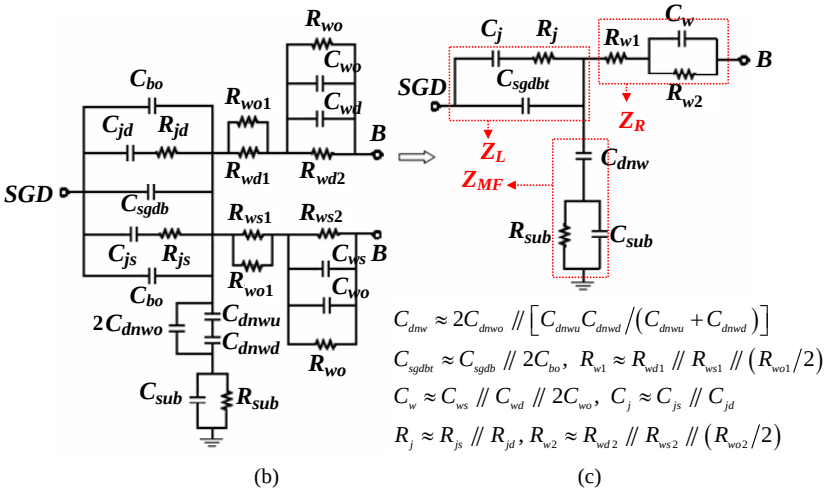
where R_{subI} and C_{subI} represent the p-substrate resistance and capacitance of a one-finger device, $R_{subunit}$ and $C_{subunit}$ are used to explain the increase in R_{sub} and C_{sub} with the increase in the number of gate fingers.

3. Scalable Model Parameter Extraction

In order to accurately predict the scalability of the substrate elements, a direct parameter extraction methodology is of the utmost importance. In this work, two different test configurations are used. One has the *DNW* floating (as shown in **Figure 3(a)**) and the other has the *DNW* grounded (as shown in **Figure 4(a)**). In each case, all *S/D/G* terminals for different fingers are connected together as port one, the *B* terminal is port two, and the p-substrate grounded. The equivalent circuits shown in **Figure 3(b)** and **Figure 4(b)** can easily be derived from the complete equivalent circuit shown in **Figure 2**, for

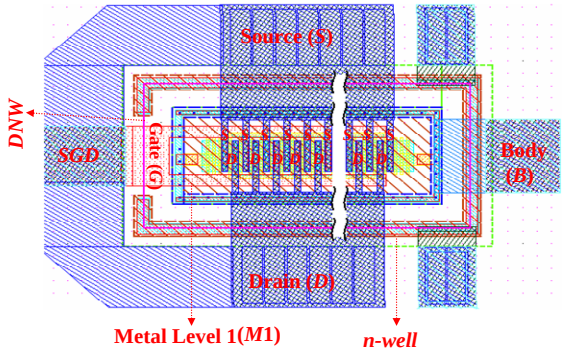


(a)

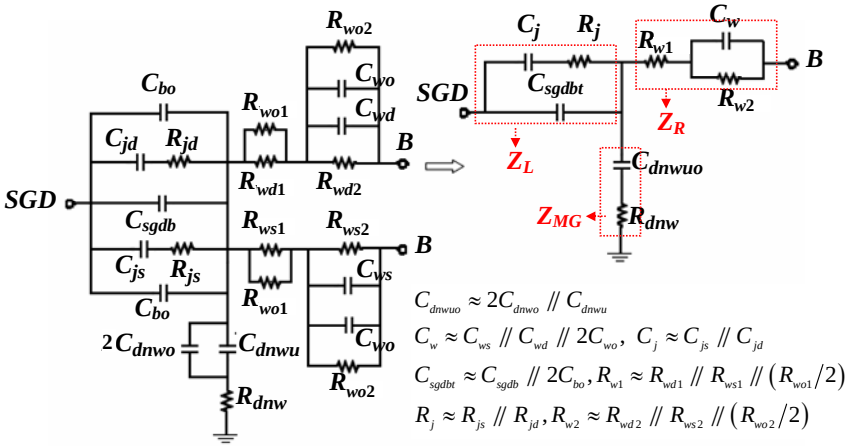


(b) (c)

Figure 3. (a) Simplified layout plane figure of *DNW* RF-MOSFETs with *S*/*G*/*D* terminals connected together, while the *DNW* is floating. (b) Equivalent circuit model for the device shown in Figure 3(a). R_{dnw} is ignored for its slight influence on two-port measurement. (c) Simplified equivalent circuit for parameter extraction.



(a)



(b) (c)

Figure 4. (a) Simplified layout plane figure of *DNW* RF-MOSFETs with *S*/*G*/*D* terminals connected together, with the *DNW* grounded. (b) Equivalent circuit model for device shown in Figure 4(a). Since R_{dnw} is much smaller than R_{sub}, the contribution of C_{dnwd}, R_{sub} and C_{sub} to *Z*-parameters becomes so slight that it can be ignored. (c) Simplified equivalent circuit for parameter extraction.

modeling the above two test structures (e.g., with the *DNW* in grounded or float configuration, respectively).

As seen from **Figure 3(b)** and **Figure 4(b)**, since the topologies from *S* to *B* are the same as that from *D* to *B*, both of the equivalent circuits shown in **Figure 3(b)** and **Figure 4(b)** can be reduced to *T*-networks by using simple approaches as shown at the bottom of **Figure 3(c)** and **Figure 4(c)**. Based on (2a)-(2i) and the approaches used to simplify **Figure 3(b)** and **Figure 4(b)** to **Figure 3(c)** and **Figure 4(c)**, respectively, the elements of the two *T*-networks shown in **Figure 3(c)** and **Figure 4(c)** can be calculated with the following equations:

$$C_j = \left(N_f + 1\right) C_{j,i} \tag{3a}$$

$$R_j = R_{j,i} \Big/ \left(N_f + 1\right) \tag{3b}$$

$$C_w = 2C_{wo} + \left(N_f + 1\right) C_{w,i} \tag{3c}$$

$$R_{w1} = \frac{0.5R_{wo1}R_{w1,i} \Big/ \left(N_f + 1\right)}{0.5R_{wo1} + R_{w1,i} \Big/ \left(N_f + 1\right)} \tag{3d}$$

$$R_{w2} = \frac{0.5R_{wo2}R_{w2,i} \Big/ \left(N_f + 1\right)}{0.5R_{wo2} + R_{w2,i} \Big/ \left(N_f + 1\right)} \tag{3e}$$

$$C_{sgdbt} = 2C_{bo} + N_f \left[2C_{sdb,i} + C_{gb,i}\right] \tag{3f}$$

$$C_{dnwuo} = 2C_{dnwo} + N_f C_{dnwu,i} \tag{3g}$$

$$C_{dnw} = 2C_{dnwo} + N_f C_{dnw,i} \tag{3h}$$

where

$$C_{dnw,i} = \frac{C_{dnwu,i}C_{dnwd,i}}{C_{dnwu,i} + C_{dnwd,i}} \tag{3h.1}$$

Using (3h.1), $C_{dnw,i}$ can be calculated as follows:

$$C_{dnwd,i} = \frac{C_{dnwu,i}C_{dnw,i}}{C_{dnwu,i} - C_{dnw,i}} \tag{3h.2}$$

(2c), (2g)-(2k) and (3a)-(3h) give the N_f-dependent equations of the equivalent circuit in **Figure 2**. This enables the direct identification of the scalability of the substrate components. This will be shown later in this section.

As the Z_L and Z_R of the *T*-network shown in **Figure 4(c)** are the same as the Z_L and Z_R shown in **Figure 3(c)**, with the ground terminal as reference, the *Z*-parameters of the T-networks shown in **Figure 3(c)** and **Figure 4(c)** can be calculated approximately with the following equations:

$$\begin{aligned}\left[Z_L\right]^{-1} &= \left[Z_{dnw\_floating,11} - Z_{dnw\_floating,12}\right]^{-1} \\ &= \left[Z_{dnw\_grounded,11} - Z_{dnw\_grounded,12}\right]^{-1} \\ &= \frac{\omega^2 C_j^2 R_j}{1+\omega^2 C_j^2 R_j^2} + j\frac{\omega C_j}{1+\omega^2 C_j^2 R_j^2} + j\omega C_{sgdbt}\end{aligned} \tag{4a}$$

$$\begin{aligned}Z_R &= Z_{dnw\_floating,22} - Z_{dnw\_floating,12} \\ &= Z_{dnw\_grounded,22} - Z_{dnw\_grounded,12} \\ &= R_{w1} + \frac{R_{w2}}{1+\omega^2 R_{w2}^2 C_w^2} - j\omega\frac{R_{w2}^2 C_w}{1+\omega^2 R_{w2}^2 C_w^2}\end{aligned} \tag{4b}$$

$$\begin{aligned}Z_{MF} &= Z_{dnw\_floating,12} = \frac{R_{sub}}{1+\omega^2 R_{sub}^2 C_{sub}^2} \\ &\quad - j\omega\frac{R_{sub}^2 C_{sub}}{1+\omega^2 R_{sub}^2 C_{sub}^2} - j\frac{1}{\omega C_{dnw}}\end{aligned} \tag{4c}$$

$$Z_{MG} = Z_{dnw\_grounded,12} = R_{dnw} + \frac{1}{j\omega C_{dnwuo}} \tag{4d}$$

where $Z_{dnw\_floating}$ and $Z_{dnw\_grounded}$ are measured *Z*-parameters of *DNW* RF MOSFETs with *S/G/D* terminals connected together, when the *DNW* is floating or grounded, respectively.

Further, the real and imaginary parts of the above *Z*-parameter expressions can be rearranged as follows:

$$\frac{\omega^2}{\mathrm{Re}\left\{\left[Z_L\right]^{-1}\right\}} = \omega^2 R_j + \frac{1}{C_j^2 R_j} \tag{5a}$$

$$C_{sgdbt} = \omega^{-1}\left\{\mathrm{Im}\left\{\left[Z_L\right]^{-1}\right\} - \frac{\omega C_j}{1+\omega^2 C_j^2 R_j^2}\right\} \tag{5b}$$

$$-\frac{\omega}{\mathrm{Im}\left[Z_R\right]} = \omega^2 C_w + \frac{1}{R_{w2}^2 C_w} \tag{5c}$$

$$R_{w1} = \mathrm{Re}\left[Z_R\right] - \frac{R_{w2}}{1+\omega^2 R_{w2}^2 C_w^2} \tag{5d}$$

$$\left\{\mathrm{Re}\left[Z_{MF}\right]\right\}^{-1} = R_{sub}^{-1} + \omega^2 R_{sub} C_{sub}^2 \tag{5e}$$

$$C_{dnw} = -\left\{\omega\left[\mathrm{Im}\left[Z_{MF}\right] + \omega R_{sub}^2 C_{sub} \Big/ \left(1+\omega^2 R_{sub}^2 C_{sub}^2\right)\right]\right\}^{-1} \tag{5f}$$

$$R_{dnw} = \mathrm{Re}\left[Z_{MG}\right] \tag{5g}$$

$$\left[-\mathrm{Im}\left(Z_{MG}\right)\right]^{-1} = \omega C_{dnwuo} \tag{5h}$$

Using (5a) and (5c), R_j and C_w can be extracted from the slopes of the linear regression curves of the experimental $\omega^2 \Big/ \mathrm{Re}\left\{\left[Z_L\right]^{-1}\right\}$ and $-\omega \Big/ \mathrm{Im}\left[Z_R\right]$ versus ω^2, respectively. (5a) and (5c), after subtracting R_j and C_w, give C_j and R_{w2}. Further, (5b) and (5d) give C_{sgdbt} and R_{w1}. Using (5e), R_{sub} and C_{sub} can be determined from the intercept of the linear regression curve of the experimental $1/Re\left[Z_{MF}\right]$ versus ω^2, and the slope gives C_{sub} after subtracting R_{sub}. After subtracting R_{sub} and C_{sub}, (5f) gives C_{dnw}. Using (5h), C_{dnwuo} can be extracted from the slope of the linear regression curve of the experimental

$\mathrm{Im}(Z_{MG})$ versus ω, while (5g) gives R_{dnw} directly. Thus, all elements of the equivalent circuit of **Figure 3(c)** and/or **Figure 4(c)** are extracted.

For extracting the values of the derived scalable model parameters in (2c), (2g)-(2k) and (3a)-(3h), two different test structures for nine devices with different number of fingers (N_f of each device is 1, 2, 4, 8, 16, 24, 32, 48 and 64, the length (L_f) and width (W_f) for each finger are fixed at 0.18 μm and 2.5 μm), with the *DNW* floating and grounded, respectively, were fabricated using the SMIC 0.18 μm 1P6M RF-CMOS process. *M*1 is used to connect all of the *S/D/G* terminals for different fingers together as port one, while the *B* terminal is port two for two-port RF measurement.

In this work, two-port *S*-parameters were measured and de-embedded (*Open* + *Short*) for parasitics introduced by the GSG PAD using an Agilent E8363B Network Analyzer and a CASCADE Summit probe station. Then, the de-embedded *S*-parameters were transformed to *Z*-parameters for directly extracting all the parameters of the *T*-networks shown in **Figure 3(c)** and **Figure 4(c)** using the parameter extraction methodology developed in this section.

As mentioned in [1], when the junctions become significant, the equivalent circuit in **Figure 2** and its corresponding parameter values are less reasonable. Thus, in this work, the extraction of the substrate network parameters is executed at V_B = –1 V and V_{SGD} = 0 V. A detailed extraction procedure for a 32-finger *DNW* nMOSFET (L_f = 0.18 μm and W_f = 2.5 μm for each finger) is given in **Figure 5** to **Figure 8**. Excellent linear regressions validated the feasibility and accuracy of the parameter extraction methodology developed in this section. Similar extraction procedures are finally used for substrate parameter value extraction for the nine fabricated devices with different number of fingers at V_B = –1 V and V_{SGD} = 0 V. The extracted results are plotted in **Figure 9**.

4. Scalable Model Verification and Validation

Once R_j, C_j, C_w, R_{w1}, R_{w2}, C_{sgdbt}, R_{dnw}, R_{sub}, C_{sub}, C_{dnwuo} and C_{dnw} are extracted, by using (3a)-(3h) and (2i), $R_{j,i}$, $C_{j,i}$, C_{wo}, $C_{w,i}$, R_{wo1}, $R_{w1,i}$, R_{wo2}, $R_{w2,i}$, C_{bo}, ($2C_{sdbi}$ + C_{gbi}), R_{dnwo}, R_{dnwi}, R_{subI}, $R_{subunit}$, C_{subI}, $C_{subunit}$, C_{dnwo}, C_{dnwui} and C_{dnwi} can be obtained with a simple optimization procedure from the relationships between the total extracted results and N_f. After determining C_{dnwui} and C_{dnwi}, (3h.2) gives $C_{dnwd,i}$. Thus, (2a)-(2k) and (3a)-(3h) become only $N_{s/d}$– and N_f– dependence equations. **Table 1** gives the extracted scalable model parameter values. **Figure 9** depicts the comparisons between the extracted substrate resistances and capacitances of the nine *DNW* nMOSFETs and the modeled results based on the extracted parameter values shown in **Table 1**. The excellent agreement between the extracted and modeled N_f- dependent substrate network components verifies that the proposed scalable model ((3a-3h)) can accurately describe the scalabilities of the substrate network components of *DNW* MOSFETs.

To verify the validity of the proposed substrate network, the accuracy of the derived scalable model and the developed methodology for parameter extraction, multi-finger *DNW* nMOSFETs, with the *G* terminal defining port one, the *D* terminal defining port two and the *S*, *B* and the p-substrate connected together with ground serving as the common terminal (*i.e.* common-source test configuration) with the *DNW* connected to ground, are also fabricated and tested. A macro-model (as shown in

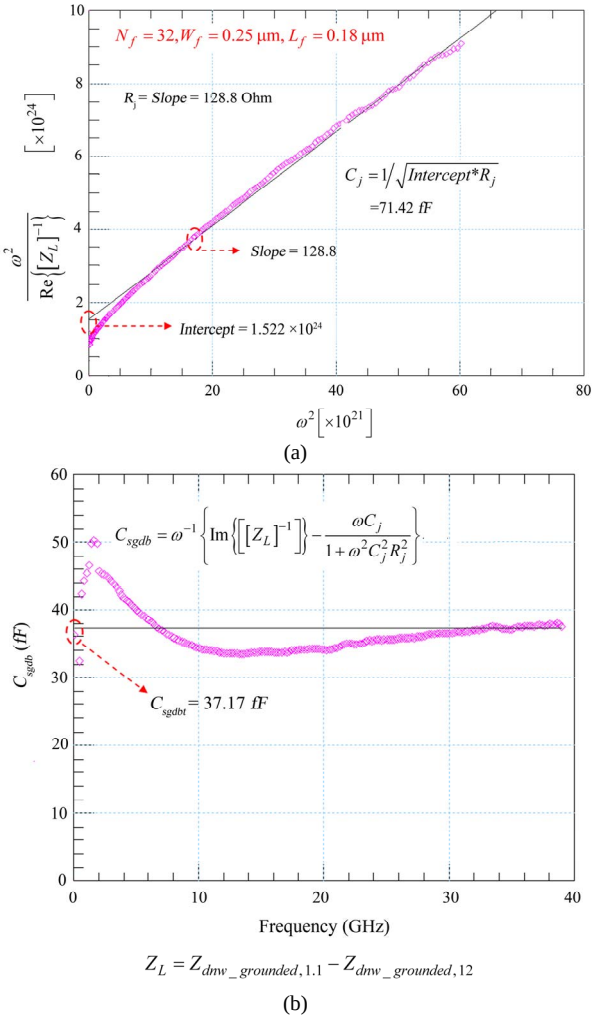
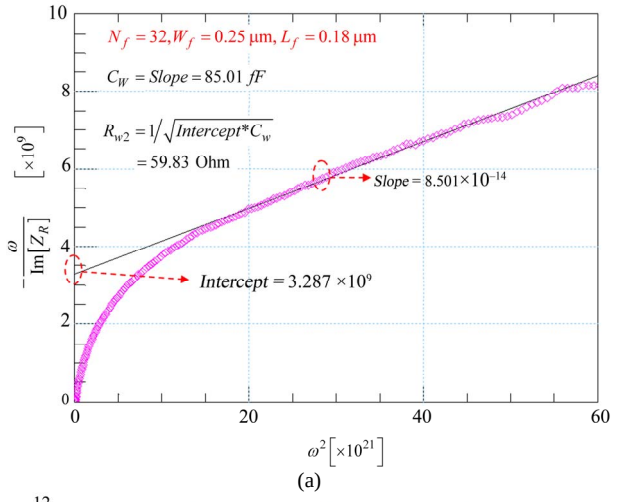
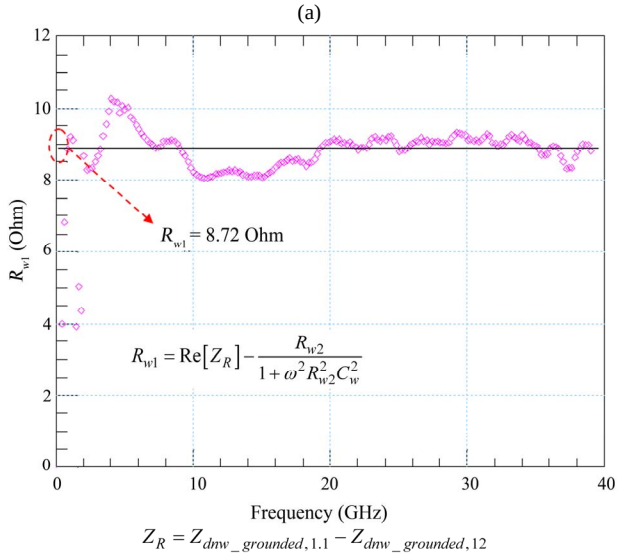


Figure 5. (a) Determine R_j from the slope of the linear regression curve of the experimental $\omega^2/\mathrm{Re}\{[Z_L]-1\}$ versus ω^2. C_j can be calculated from the intercept. (b) After subtracting R_j and C_j, (5b) gives C_{sgdbt}.

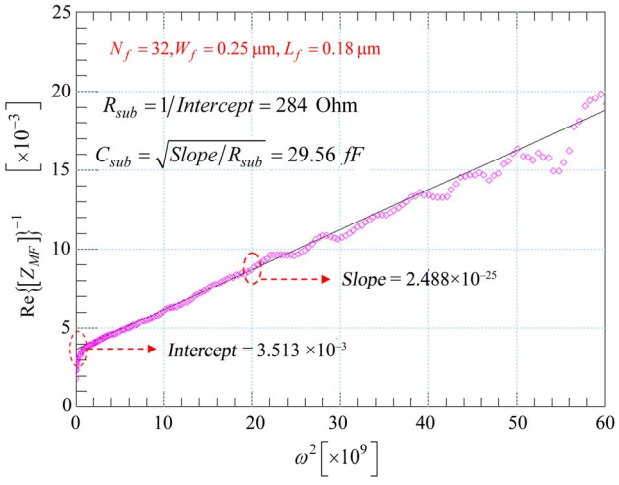


(a)

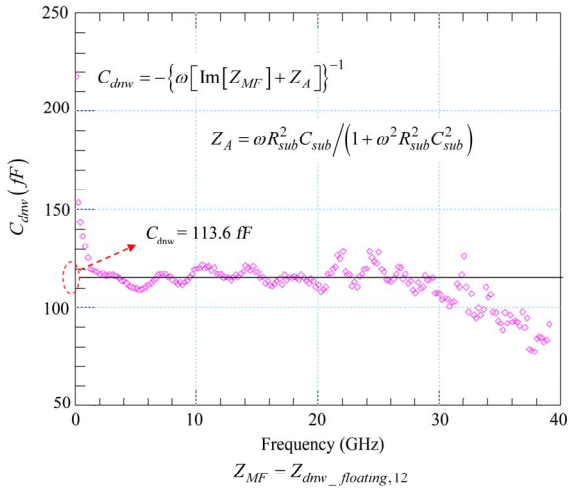


(b)

Figure 6. (a) Extract C_w from the slope of the linear regression curve of the experimental $-w/\mathrm{Im}[ZR]$ versus w^2. R_{w2} can be extracted from the intercept. (b) After subtracting R_{w2} and C_w, (5d) gives R_{w1}.

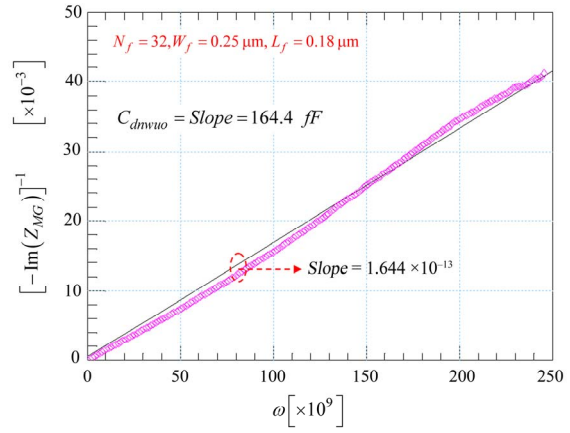


(a)

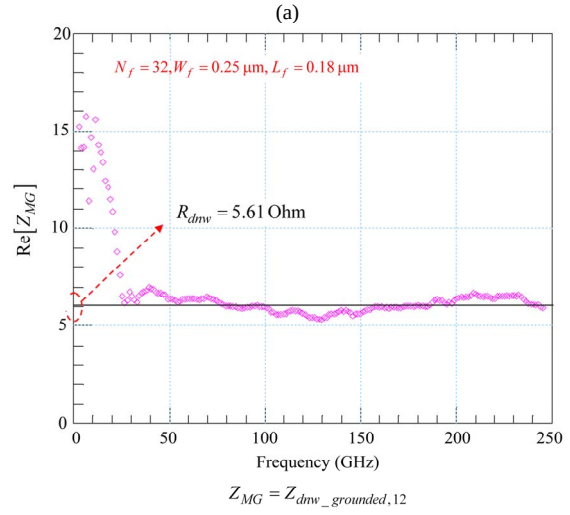


(b)

Figure 7. (a) Extract R_{sub} from the intercept of the experimental $\{\mathrm{Re}[Z_{MF}]\}-1$ versus w^2, and the slope gives C_{sub} after subtracting R_{sub}. (b) After subtracting R_{sub} and C_{sub}, (5f) gives C_{dnw}.



(a)



(b)

Figure 8. (a) Extract C_{dnwuo} from the slope of the linear regression curve of the experimental $\mathrm{Im}[Z_{MG}]$ versus w. (b) R_{dnw} can be determined from the real part of Z_{MG}.

Figure 10) for common-source connected *DNW* RF MOSFETs modeling was developed. The model consists of the BSIM3v3.2 model core with the proposed new substrate-network and is simulated in Agilent Advanced Design System (ADS) directly.

In **Figure 10**, R_g, R_d, and R_s are *G*, *D* and *S* terminal series resistances, C_{ds} is *D*-to-*S* capacitance. C_{gs}, and C_{gd} represent the *G*-to-*S* and *G*-to-*D* capacitances, respectively. C_{gb}, C_{db} and C_{sb} indicate the *G*-to-*B*, *D*-to-B, *S*-to-*B* capacitances, and the sum of the three components has been extracted in section 4. A conventional method developed in [13] is used to extract the initial values of three terminal series resistances from de-embedded *Y*-parameters. By using the extraction method proposed in [13], the following equations are employed for the remaining components extraction:

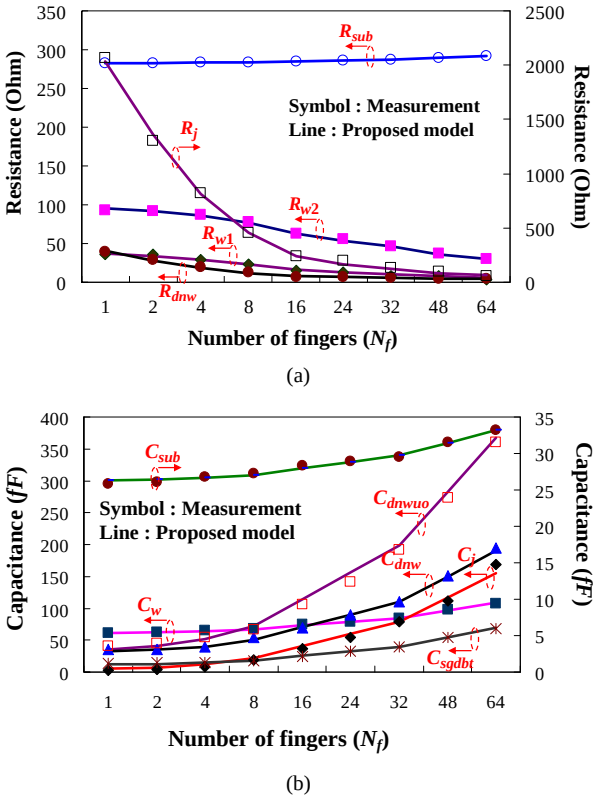


Figure 9. (a) Extracted and modeled substrate resistances and (b) capacitances of *DNW* nMOSFETs with different number of fingers, while the length (L_f) and width (W_f) for each finger are fixed at 0.18 μm and 2.5 μm.

Table 1. Extracted parameter values of the proposed model of the substrate network in *DNW* RF MOSFETs

$R_{j,i}$(Ω)	$C_{j,i}$(*fF*)	C_{wo}(*fF*)	$C_{w,i}$(*fF*)	R_{wo1} (Ω)
4162	2.395	30.64	0.737	87.78
R_{wo2}(Ω)	$R_{w2,i}$ (Ω)	C_{bo}(*fF*)	$2C_{sdbi}+C_{gbi}$(*fF*)	
203.7	2775	5.471	0.91	
R_{dnwi} (Ω)	R_{subI} (Ω)	$R_{subunit}$ (Ω)	C_{subI}(*fF*)	$C_{subunit}$(*fF*)
73.79	282.8	0.137	26.18	0.11
C_{dnwui}(*fF*)	C_{dnwdi}(*fF*)	$R_{w1,i}$ (Ω)	R_{dnwo} (Ω)	C_{dnwo}(*fF*)
5.045	4.771	447.7	3.46	15.2

Table 2. Values of the extracted external capacitors from common source connected devices with different N_f, at zero bias.(L_f = 0.18 μm; W_f = 2.5 μm)

N_f	$C_{gs/d}$ (*fF*)	C_{gb} (*fF*)	C_{ds} (*fF*)
1	0.66	3.4	0.68
2	3.5	4.2	1.02
4	3.9	7.2	3.1
8	8.6	8.5	10.7
16	18.4	10.3	24.1
24	28.3	13.2	41.2
32	36.1	15.5	54.6
48	55.4	16.2	83.4
64	72.2	17.5	110.2

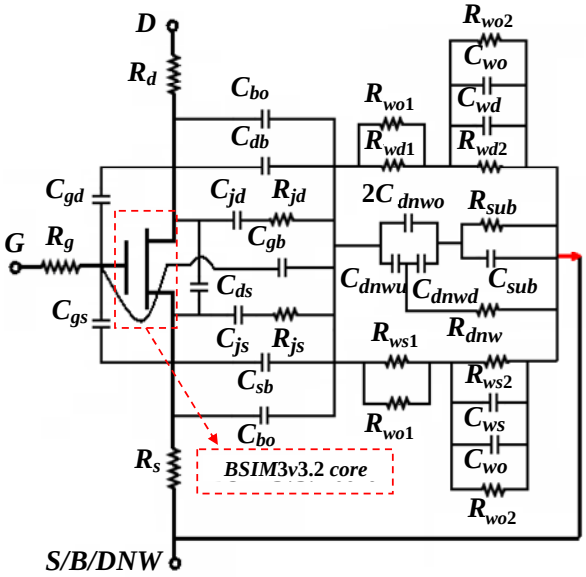


Figure 10. Macro-model for *DNW* RF-MOSFETs modeling when *S/D* junctions are not significant. The test configuration with the *G* terminal defining port one, the *D* terminal defining port two and the *S*, *B* and the p-substrate connected together with ground serving as the common terminal (*i.e.* common-source test configuration), with the *DNW* is tied to ground using M1 (metal level 1), are used in two-port measurement. All the parameters of the BSIM3v3.2, including the terminal resistances R_d, R_g and R_s, are extracted beforehand.

$$C_{gd} = \frac{\mathrm{Im}(Y_{12})}{\omega} \tag{6a}$$

$$C_{gs} = C_{gd} \tag{6b}$$

$$C_{gb} = \frac{\mathrm{Im}(Y_{11}+Y_{12})}{\omega} - C_{gd} \tag{6c}$$

According to (1c), the total C_{gb} of an RF MOSFET with the number of fingers is N_f can be calculated as follows:

$$C_{gb} = N_f C_{gb,i} \tag{6d}$$

Thus, $C_{gb,i}$ can be extracted for two or more devices with different number of fingers. Once $C_{gb,i}$ is obtained, (3f) gives $C_{sdb,i}$.

$$C_{sdb,i} = \frac{\left[C_{sgdbt} - 2C_{bo} - N_f C_{gb,i}\right]}{2N_f} \tag{6e}$$

In this work, the extracted values of $C_{gb,i}$ and $C_{sdb,i}$ for multi-finger devices with the length *(L)* and width *(W)* for each finger fixed at 0.18 μm and 2.5 μm, are 0.338 *f*F and 0.285 *f*F, respectively. C_{ds} in **Figure 10** is calculated from de-embedded *Y*-parameters of the common-source connected nMOSFET as follows:

$$C_{ds} = \frac{\mathrm{Im}\left(Y_{22} - Y_{12}\right)}{\omega} - \frac{C_d\left(C_s + C_t\right)}{C_d + C_s + C_t} \tag{6f}$$

where

$$C_d = C_{jd} + C_{bo} + C_{db}, \quad C_s = C_{js} + C_{bo} + C_{sb} \quad ,$$

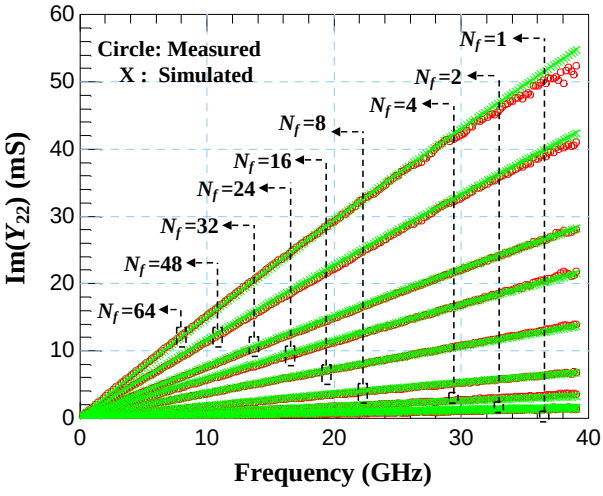
$$C_t = 2C_{wo} + C_{wd} + C_{ws} + \frac{C_n C_{sub}}{C_n + C_{sub}}$$

and $$C_n = 2C_{dnwo} + \frac{C_{dnwu} C_{dnwd}}{C_{dnwu} + C_{dnwd}}.$$

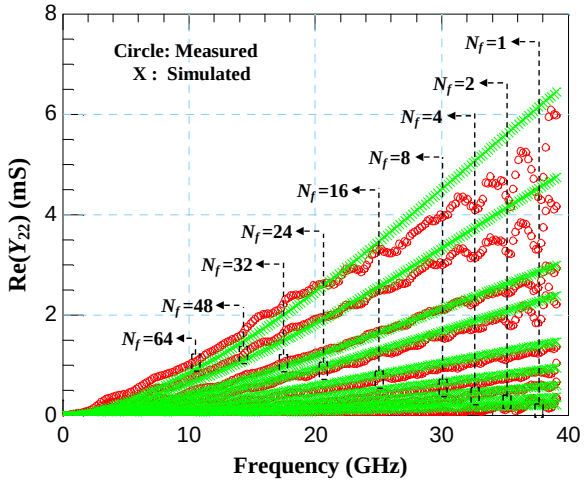
The external capacitances in **Figure 10** (*i.e.* C_{gd}, C_{gs} and C_{ds}) extracted from the nine devices with different N_f at zero-bias condition (V_G = 0 V; V_D = 0 V and $V_{S/B/DNW}$ = 0 V) are listed in **Table 2**. After all the parameters have been extracted, measured and simulated output admittances (Y_{22}) at zero-bias for the nine devices with different number of fingers are compared and plotted in **Figure 11**. Excellent agreement is achieved between the measured and simulated results. Due to the oscillation of the measurements at high frequencies, the resistive parasitics of the substrate are hard to be extracted accurately, which is further introducing errors between the measured and simulated results of the real parts of the output admittances of transistors.

5. Summary

A compact, physically based scalable model for the substrate network of *DNW* RF MOSFETs has been demonstrated. All of the substrate components are directly extracted from two-port measurements. The derived and extracted scalable model is directly used to capture the substrate characteristics of common-source connected devices. The model shows excellent agreement with measured output admittances of devices with different number of fingers at an operation frequency up to 40 GHz. The model and methodology developed in this paper also can be used to accurately extract the substrate network in RF MOSFETs without *DNW* implantation by removing the sub-network for the *DNW*.



(a)



(b)

Figure 11. Measured and simulated output admittances of *DNW* nMOSFETs with different number of fingers at zero bias (V_G = 0 V, V_D = 0 V and $V_{S/B/DNW}$ = 0 V). All the devices are connected in common source configuration, while the *DNW* is grounded.

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