

Efficient Time-Domain Signal and Noise FET Models for Millimetre-Wave Applications

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ABSTRACT

Based on the active coupled line concept, a novel approach for efficient signal and noise modeling of millimeter-wave field-effect transistors is proposed. The distributed model considers the effect of wave propagation along the device electrodes, which can significantly affect the device performance especially in the millimetre-wave range. By solving the multi-conductor transmission line equations using the Finite-Difference Time-Domain technique, the proposed procedure can accurately determine the signal and noise performance of the transistor. In order to demonstrate the proposed FET model accuracy, a distributed low-noise amplifier was designed and tested. A model selection is often a trade-off between procedure complexity and response accuracy. Using the proposed distributed model versus the circuit-based model will allow increasing the model frequency range.

Keywords: Distributed Model; FDTD; Noise Correlation Matrix; FET

1. Introduction

Efficient Computer-Aided Design (CAD) of high-frequency systems is critically based on the performance of their internal component models. As the core of modern communication systems, active devices should be then carefully modeled for reliable system design. In high frequencies, when the device physical dimensions become comparable to the wavelength, the input active transmission line has a different reactance from the output transmission line [1,2], exhibiting different phase velocities for the input and output signals. Therefore, the phase cancellation due to the phase velocity mismatching will affect the device performance [3]. Thus, a full-wave time-domain analysis involving distributed elements should be considered. However, this type of analysis is highly time consuming [4-6], even if different simulation time reduction techniques have been already proposed [7]. As a result, semi-distributed models such as the slice model could be seen as a suitable alternative to overcome this limitation [8]. However, by increasing the frequency up to the millimetre-wave range, the slice model cannot precisely model the wave propagation effect and phase cancellation phenomena. Therefore, to achieve more accurate design in millimetre-wave applications, one needs to develop a more advanced distributed model.

In this paper, a distributed model is proposed [9]. It includes the effect of wave propagation along the electrodes more accurately than the semi distributed model

although the CPU time of this model is a little higher than the slice model. Since a time domain analytical solution does not exist, a numerical approach was used. Among all the existing methods, the Finite-Difference Time-Domain method (FDTD) was retained as one of the most widely used in this area [10]. The proposed model was demonstrated through the design of a distributed amplifier.

2. Signal FET Modeling

The proposed millimetre-wave Field Effect Transistor (FET) model is shown in **Figure 1**. It consists of three active coupled transmission lines (*i.e.*, the three coupled electrodes of the device). As shown in this Figure, each elementary section Δx of the model can be represented by a 6-port equivalent circuit. This approach combines a conventional FET small-signal equivalent circuit model with a distributed circuit to account for the coupled transmission line effect of the electrode structure where all parameters are per unit length. With the condition $\Delta x \rightarrow 0$, we obtain the following system of equations [11,12]:

$$\frac{\partial I_d(x,t)}{\partial x} + C_{11} \frac{\partial V_d(x,t)}{\partial t} - C_{12} \frac{\partial V_g(x,t)}{\partial t} - C_{13} \frac{\partial V_s(x,t)}{\partial t} + G_m V'_g(x,t) + G_{ds} (V_d(x,t) - V_s(x,t)) = 0 \quad (1)$$

$$\frac{\partial I_g(x,t)}{\partial x} + C_{22} \frac{\partial V_g(x,t)}{\partial t} - C_{12} \frac{\partial V_d(x,t)}{\partial t} + C_{gs} \frac{\partial V'_g(x,t)}{\partial t} = 0 \quad (2)$$

$$\frac{\partial I_s(x,t)}{\partial x} + C_{33} \frac{\partial V_s(x,t)}{\partial t} - C_{13} \frac{\partial V_d(x,t)}{\partial t} - C_{gs} \frac{\partial V'_g(x,t)}{\partial t} - G_m V'_g(x,t) + G_{ds} (V_s(x,t) - V_d(x,t)) = 0 \quad (3)$$

$$\frac{\partial V_d(x,t)}{\partial x} + R_d I_d(x,t) + L_{dd} \frac{\partial I_d(x,t)}{\partial t} + M_{gd} \frac{\partial I_g(x,t)}{\partial t} + M_{ds} \frac{\partial I_s(x,t)}{\partial t} = 0 \quad (4)$$

$$\frac{\partial V_g(x,t)}{\partial z} + R_g I_g(x,t) + L_{gg} \frac{\partial I_g(x,t)}{\partial t} + M_{gd} \frac{\partial I_d(x,t)}{\partial t} + M_{gs} \frac{\partial I_s(x,t)}{\partial t} = 0 \quad (5)$$

$$\frac{\partial V_s(x,t)}{\partial z} + R_s I_s(x,t) + L_{ss} \frac{\partial I_s(x,t)}{\partial t} + M_{ds} \frac{\partial I_d(x,t)}{\partial t} + M_{gs} \frac{\partial I_g(x,t)}{\partial t} = 0 \quad (6)$$

with

$$\begin{aligned} C_{11} &= C_{dp} + C_{ds} + C_{dg}, \\ C_{22} &= C_{gp} + C_{dg}, \\ C_{33} &= C_{sp} + C_{ds}, C_{12} = C_{dg}, C_{13} = C_{ds}. \end{aligned}$$

and where V_d , V_g , and V_s are the drain, gate and source voltages, respectively, and V'_g the voltage across gate-source capacitor. I_d , I_g , and I_s are the drain, gate and source currents, respectively. These variables are time-dependant and function of the position x along the device width. Also, M_{ds} , M_{gd} , and M_{gs} represent the mutual inductances between drain-source, gate-drain and gate-source, respectively; In the above system, we have an extra unknown parameter, *i.e.*, the gate-source capacitance voltage V'_g . Therefore, the following equation should be included to complete the system of equations

$$V'_g(x,t) + V_s(x,t) + R_i C_{gs} \frac{\partial V'_g(x,t)}{\partial t} - V_g(x,t) = 0 \quad (7)$$

3. Noise FET Modeling

Similarly to the signal model proposed in the above section, a noise model can be developed based on the same concept, *i.e.*, a set of transmission lines excited by noise equivalent sources distributed on the conductors, as shown in **Figure 2**. We thus have

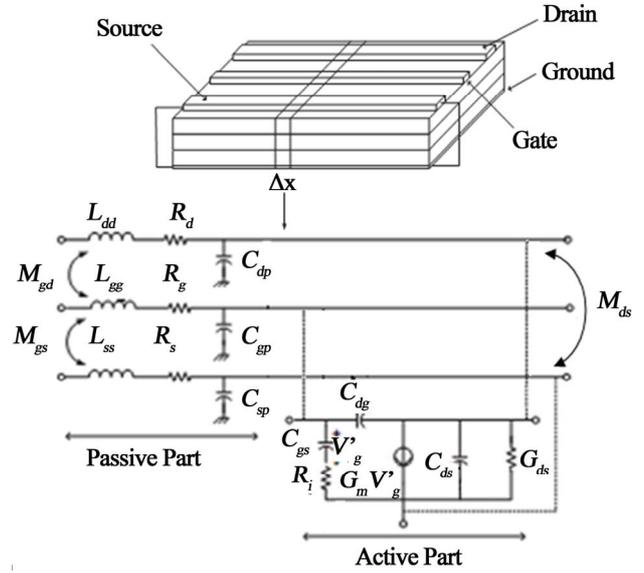


Figure 1. The different parts of a segment in the distributed model.

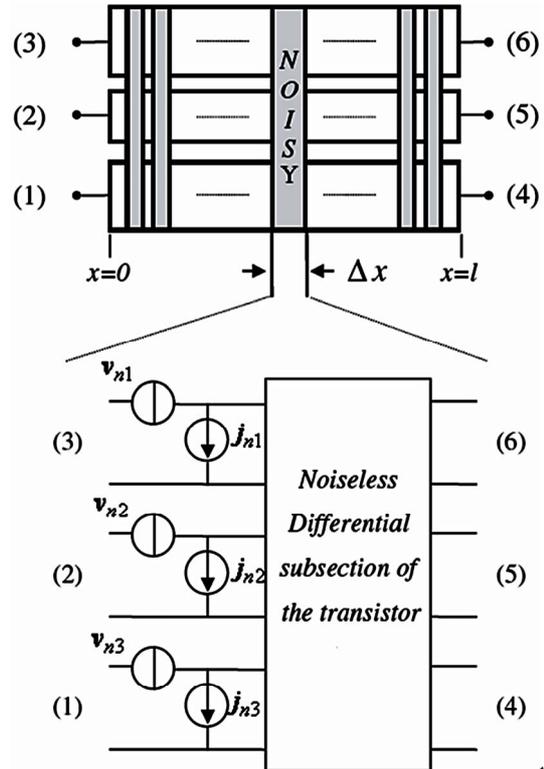


Figure 2. Noise-equivalent voltage and current sources.

$$\frac{\partial}{\partial x} [I'] + [C] \frac{\partial}{\partial t} [V'] + [G][V'] + [j_n] = 0 \quad (8a)$$

$$\frac{\partial}{\partial x} [V] + [L] \frac{\partial}{\partial t} [I] + [R][I] + [v_n] = 0 \quad (8b)$$

where

$$\begin{aligned}
\mathbf{I} &= [I_d(x,t), I_g(x,t), I_s(x,t)], \\
\mathbf{I}' &= [I_d(x,t), I_g(x,t), I_s(x,t), 0] \\
\mathbf{V}' &= [V_d(x,t), V_g(x,t), V_s(x,t), V'_g(x,t)], \\
\mathbf{V} &= [V_d(x,t), V_g(x,t), V_s(x,t)] \\
L &= \begin{bmatrix} L_{dd} & M_{gd} & M_{ds} \\ M_{gd} & L_{gg} & M_{gs} \\ M_{ds} & M_{gs} & L_{ss} \end{bmatrix}, \\
R &= \begin{bmatrix} R_d & 0 & 0 \\ 0 & R_g & 0 \\ 0 & 0 & R_s \end{bmatrix} \\
C &= \begin{bmatrix} C_{11} & -C_{12} & -C_{13} & 0 \\ -C_{12} & C_{22} & 0 & C_{gs} \\ -C_{13} & 0 & C_{33} & -C_{gs} \\ 0 & 0 & 0 & R_i C_{gs} \end{bmatrix}, \\
G &= \begin{bmatrix} G_{ds} & 0 & -G_{ds} & G_m \\ 0 & 0 & 0 & 0 \\ -G_{ds} & 0 & G_{ds} & -G_m \\ 0 & -1 & 1 & 1 \end{bmatrix}
\end{aligned}$$

Note that the vectors $[v_n]$ and $[j_n]$ in **Figure 2** are the linear density of exciting voltage and current noise sources, respectively.

To evaluate the noise sources, we considered a noisy FET subsection with gate width Δx . Thus, the unit-per-length noise correlation matrix for chain representation of the transistor (CA_{UPL}) can be deduced as [13]

$$[CA_{UPL}] = \left\langle \left(\begin{bmatrix} [v_n] \\ [j_n] \end{bmatrix} \right) \left(\begin{bmatrix} [v_n] \\ [j_n] \end{bmatrix} \right)^+ \right\rangle = \left\langle \begin{bmatrix} [C_{11}] & [C_{12}] \\ [C_{21}] & [C_{22}] \end{bmatrix} \right\rangle \quad (9)$$

where $\langle \rangle$ denotes the ensemble average and $+$ the transposed complex conjugate. According to the correlation matrix definition, we can calculate $[v_n]$ and $[j_n]$ knowing (CA_{UPL}) , to completely describe the proposed FET noise model. Indeed, by solving (9), the noise parameters of the transistor can be obtained.

Based on the transmission line circuit theory, the model impedance and admittance matrices can be expressed as

$$\begin{aligned}
[Z(\omega)] &= [R(\omega)] + j\omega[L(\omega)] \\
[Y(\omega)] &= [G(\omega)] + j\omega[C(\omega)] + [Y_{tr}]
\end{aligned} \quad (10)$$

where $[R]$, $[L]$, $[C]$, and $[G]$ refer to the matrix representation of the well-known distributed circuit parameters of a transmission line namely, the resistance R , the induc-

tance L , the capacitance C , and the conductance G , respectively. $[Y_{tr}]$ is accounted for the active parallel sub-section of the model. By solving the second-order differential equations of the model, its voltage and current vectors can be written as [14]

$$[V(x)] = [S_v] \exp(-[\Gamma x]) V^+ + [S_v] \exp(+[\Gamma x]) V^- \quad (11)$$

$$[I(x)] = [S_i] \exp(-[\Gamma x]) I^+ - [S_i] \exp(+[\Gamma x]) I^- \quad (12)$$

where

$$[V(x)] = [V^d(x) \quad V^g(x) \quad V^s(x)]^t$$

and

$$[I(x)] = [I^d(x) \quad I^g(x) \quad I^s(x)]^t$$

represent the voltage and current vectors at the transistor terminals, respectively (Here d , g , and s stand for drain, gate and source, respectively). The superscript “ t ” refers to the vector transpose. Let the elements of matrix $[\Gamma]$ be the eigenvalues of $[Z] \cdot [Y]$ (or $[Y] \cdot [Z]$) and the elements of matrices $[S_v]$ and $[S_i]$ be the eigenvectors of $[Z] \cdot [Y]$ and $[Y] \cdot [Z]$, respectively [16]. By considering the boundary conditions of the six-port model, the unknown coefficients V^+ and V^- can be determined. Then, applying (11) and (12) for $x = 0$ and $x = w$, w being the gate width, the voltages and currents of each port can be obtained, leading to the 6*6 impedance ($[Z]_{6*6}$) and admittance ($[Y]_{6*6}$) matrices of the model, which can be easily transformed to the scattering matrix form.

3.1. The FDTD Formulation

The FDTD technique was used to solve the above equations. Applications of the FDTD method to the full-wave solution of Maxwell's equations have shown that accuracy and stability of the solution can be achieved if the electric and magnetic field solution points are chosen to alternate in space and be separated by one-half the position discretization, e.g., $\Delta x/2$, and to also be interlaced in time and separated by $\Delta t/2$ [15-16]. To incorporate these constraints into the FDTD solution of the transmission-line equations, we divided each line into Nx sections of length x , as shown in **Figure 3**. Similarly, we divided the total solution time into segments of length Δt . In order to insure the stability of the discretization process and to insure second-order accuracy, we interlaced the $Nx + 1$ voltage points, $V_1, V_2, \dots, V_{Nx+1}$ and the Nx current points, I_1, I_2, \dots, I_{Nx} . Each voltage and adjacent current solution points were separated by $\Delta x/2$. In addition, the time points were also interlaced, and each voltage time point and adjacent current time point were separated by $\Delta t/2$ [17,18]. Then, (8) can lead to

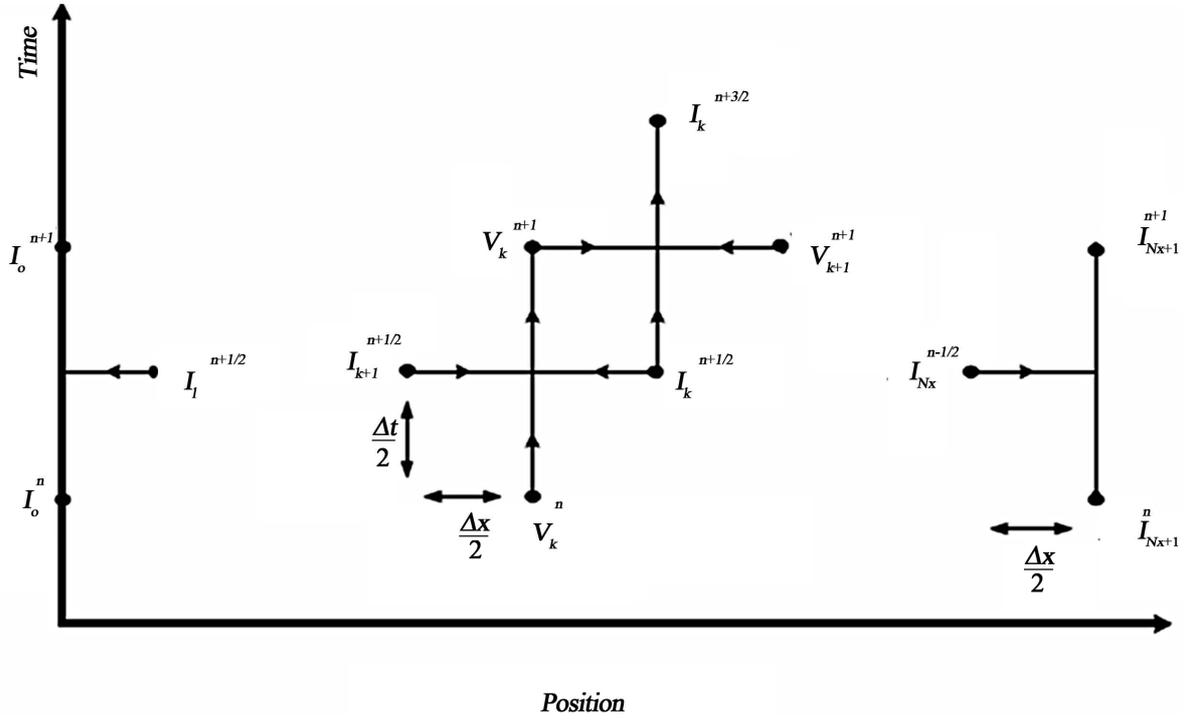


Figure 3. Relation between the spatial and temporal discretization to achieve second-order accuracy in the discretization of the derivatives.

$$\begin{aligned} & \frac{1}{\Delta x} \left([{}_d I_k^{n+1/2}] - [{}_d I_{k-1}^{n+1/2}] \right) + \frac{C_{11}}{\Delta t} \left([{}_d V_k^{n+1}] - [{}_d V_k^n] \right) \\ & - \frac{C_{12}}{\Delta t} \left([{}_g V_k^{n+1}] - [{}_g V_k^n] \right) - \frac{C_{13}}{\Delta t} \left([{}_s V_k^{n+1}] - [{}_s V_k^n] \right) \\ & + \frac{G_m}{2} \left([{}_g V_k^{n+1}] + [{}_g V_k^n] \right) \end{aligned} \quad (13)$$

$$\begin{aligned} & + \frac{G_{ds}}{2} \left([{}_d V_k^{n+1}] + [{}_d V_k^n] - [{}_s V_k^{n+1}] - [{}_s V_k^n] \right) \\ & + \sum_{m=1}^{N_{x+1}} \frac{1}{2} \left([{}_{n1} v_m^{n+3/2}] + [{}_{n1} v_m^{n+1/2}] \right) = 0 \\ & \frac{1}{\Delta x} \left([{}_g I_k^{n+1/2}] - [{}_g I_{k-1}^{n+1/2}] \right) + \frac{C_{22}}{\Delta t} \left([{}_g V_k^{n+1}] - [{}_g V_k^n] \right) \\ & - \frac{C_{12}}{\Delta t} \left([{}_d V_k^{n+1}] - [{}_d V_k^n] \right) + \frac{C_{gs}}{\Delta t} \left([{}_g V_k^{n+1}] - [{}_g V_k^n] \right) \end{aligned} \quad (14)$$

$$\begin{aligned} & + \sum_{m=1}^{N_{x+1}} \frac{1}{2} \left([{}_{n2} v_m^{n+3/2}] + [{}_{n2} v_m^{n+1/2}] \right) = 0 \\ & \frac{1}{\Delta x} \left([{}_s I_k^{n+1/2}] - [{}_s I_{k-1}^{n+1/2}] \right) + \frac{C_{33}}{\Delta t} \left([{}_s V_k^{n+1}] - [{}_s V_k^n] \right) \\ & - \frac{C_{13}}{\Delta t} \left([{}_d V_k^{n+1}] - [{}_d V_k^n] \right) - \frac{G_m}{2} \left([{}_g V_k^{n+1}] + [{}_g V_k^n] \right) \\ & - \frac{G_{ds}}{2} \left([{}_d V_k^{n+1}] + [{}_d V_k^n] - [{}_s V_k^{n+1}] - [{}_s V_k^n] \right) \\ & + \sum_{m=1}^{N_{x+1}} \frac{1}{2} \left([{}_{n3} v_m^{n+3/2}] + [{}_{n3} v_m^{n+1/2}] \right) = 0 \end{aligned} \quad (15)$$

$$\begin{aligned} & \frac{1}{\Delta x} \left([{}_d V_{k-1}^{n+1}] - [{}_d V_k^{n+1}] \right) + \frac{R_d}{2} \left([{}_d I_k^{n+3/2}] + [{}_d I_k^{n+1/2}] \right) \\ & + \frac{L_{dd}}{\Delta t} \left([{}_d I_k^{n+3/2}] - [{}_d I_k^{n+1/2}] \right) + \frac{M_{gd}}{\Delta t} \left([{}_g I_k^{n+3/2}] - [{}_g I_k^{n+1/2}] \right) \\ & + \frac{M_{gs}}{\Delta t} \left([{}_s I_k^{n+3/2}] - [{}_s I_k^{n+1/2}] \right) + \sum_{m=1}^{N_{x+1}} \frac{1}{2} \left([{}_{n1} j_m^{n+1}] + [{}_{n1} j_m^n] \right) = 0 \end{aligned} \quad (16)$$

$$\begin{aligned} & \frac{1}{\Delta x} \left([{}_g V_{k-1}^{n+1}] - [{}_g V_k^{n+1}] \right) + \frac{R_g}{2} \left([{}_g I_k^{n+3/2}] + [{}_g I_k^{n+1/2}] \right) \\ & + \frac{L_{gs}}{\Delta t} \left([{}_g I_k^{n+3/2}] - [{}_g I_k^{n+1/2}] \right) + \frac{M_{gd}}{\Delta t} \left([{}_d I_k^{n+3/2}] - [{}_d I_k^{n+1/2}] \right) \\ & + \frac{M_{gs}}{\Delta t} \left([{}_s I_k^{n+3/2}] - [{}_s I_k^{n+1/2}] \right) \\ & + \sum_{m=1}^{N_{x+1}} \frac{1}{2} \left([{}_{n2} j_m^{n+1}] + [{}_{n2} j_m^n] \right) = 0 \end{aligned} \quad (17)$$

$$\begin{aligned} & \frac{1}{\Delta x} \left([{}_s V_{k-1}^{n+1}] - [{}_s V_k^{n+1}] \right) + \frac{R_s}{2} \left([{}_s I_k^{n+3/2}] + [{}_s I_k^{n+1/2}] \right) \\ & + \frac{L_{ss}}{\Delta t} \left([{}_s I_k^{n+3/2}] - [{}_s I_k^{n+1/2}] \right) + \frac{M_{ds}}{\Delta t} \left([{}_d I_k^{n+3/2}] - [{}_d I_k^{n+1/2}] \right) \\ & + \frac{M_{gs}}{\Delta t} \left([{}_g I_k^{n+3/2}] - [{}_g I_k^{n+1/2}] \right) + \sum_{m=1}^{N_{x+1}} \frac{1}{2} \left([{}_{n3} j_m^{n+1}] + [{}_{n3} j_m^n] \right) \\ & = 0 \end{aligned} \quad (18)$$

Applying the finite difference approximation to (7) gives

$$\frac{R_i C_{gs}}{\Delta t} \left([{}_g V_k^{m+1}] - [{}_g V_k^m] \right) + \frac{1}{2} \left([{}_g V_k^{m+1}] - [{}_g V_k^m] \right) + \frac{1}{2} \left([{}_s V_k^{n+1}] + [{}_s V_k^n] \right) = \frac{1}{2} \left([{}_g V_k^{n+1}] + [{}_g V_k^n] \right) \quad (19)$$

with

$$[{}_d V_i^j] = [{}_d V((i-1)\Delta x, j\Delta t)]$$

and

$$[{}_d I_i^j] = [{}_d I((i-1/2)\Delta x, j\Delta t)] \quad (20a)$$

for the drain electrode

$$[{}_g V_i^j] = [{}_g V((i-1)\Delta x, j\Delta t)]$$

and

$$[{}_g I_i^j] = [{}_g I((i-1/2)\Delta x, j\Delta t)] \quad (20b)$$

for the gate electrode

$$[{}_s V_i^j] = [{}_s V((i-1)\Delta x, j\Delta t)]$$

and

$$[{}_s I_i^j] = [{}_s I((i-1/2)\Delta x, j\Delta t)] \quad (20c)$$

for the source electrode,

where k, m and n are integers. Solving these equations gives the required recursion relations

$$\begin{aligned} & [V_k^{n+1}] \\ & = \left(\frac{1}{\Delta t} [C] + \frac{1}{2} [G] \right)^{-1} \left\{ \left(\frac{1}{\Delta t} [C] - \frac{1}{2} [G] \right) [V_k^m] \right. \\ & \quad \left. - \frac{1}{\Delta x} \left([I_k^{m+1/2}] - [I_{k-1}^{m+1/2}] \right) + \frac{\Delta x}{2} \sum_{m=1}^{N_{x+1}} \left([j_m^{n+1}] + [j_m^n] \right) \right\} \end{aligned} \quad (21)$$

$$\begin{aligned} & [I_k^{n+3/2}] \\ & = \left(\frac{1}{\Delta t} [L] + \frac{1}{2} [R] \right)^{-1} \left\{ \left(\frac{1}{\Delta t} [L] - \frac{1}{2} [R] \right) [I_k^{n+1/2}] \right. \\ & \quad \left. - \frac{1}{\Delta x} \left([V_{k+1}^{n+1}] - [V_k^{n+1}] \right) + \frac{\Delta x}{2} \sum_{m=1}^{N_{x+1}} \left([v_m^{n+3/2}] + [v_m^{n+1/2}] \right) \right\} \end{aligned} \quad (22)$$

Superposing all the distributed noise sources is equivalent to a summation in (21) and (22) over the gate width for $m=1, \dots, N_{x+1}$. Because of its simplicity, the leapfrog method was used to solve the above equations [13,14]. First the voltages along the line were solved for a fixed time using (21) then the currents were determined using (22). The solution starts with an initially relaxed

line having zero voltage and current.

3.2. Transistor Noise Correlation Matrix

To find the noise correlation matrix for admittance representation of the transistor as a noisy six-port active network (as in **Figure 2**), the values of port currents should be determined when they are all assumed short-circuited simultaneously. Equation (21) for $k=0$ and $k=N_{x+1}$ becomes

$$V_1^{m+1} = \left(\frac{C}{\Delta t} + \frac{G}{2} \right)^{-1} \left\{ \left(\frac{C}{\Delta t} - \frac{G}{2} \right) V_1^m - \frac{I_1^{m+1/2} - I_0^{m+1/2}}{\Delta x/2} + \frac{\Delta x}{2} \sum_{m=1}^{N_{x+1}} (j_m^{n+1} + j_m^n) \right\} \quad (23)$$

$$V_{N_{x+1}}^{m+1} = \left(\frac{C}{\Delta t} + \frac{G}{2} \right)^{-1} \left\{ \left(\frac{C}{\Delta t} - \frac{G}{2} \right) V_{N_{x+1}}^m - \frac{I_{N_{x+1}}^{m+1/2} - I_{N_x}^{m+1/2}}{\Delta x/2} + \frac{\Delta x}{2} \sum_{m=1}^{N_{x+1}} (j_m^{n+1} + j_m^n) \right\} \quad (24)$$

By considering **Figure 3**, this equation requires that we replace Δx by $\Delta x/2$ only for $k=1$ and $k=N_{x+1}$.

In order to determine the transistor noise parameters, we set the input voltage source as zero ($V_s=0$). Referring to **Figure 4**, we denoted the currents at the source point ($x=0$) as I_0 and at the load point ($x=L$) as $I_{N_{x+1}}$. To determine the currents I_1 and I_{N_x} at short-circuited ports ($x=0$ and $x=L$), we set $V_1 = V_{N_{x+1}} = 0$. The finite difference approximation of (23) for $k=1$ and $k=N_x$ can be then written as (25) and (26), respectively.

$$\begin{aligned} & [I_1^{n+3/2}] \\ & = \left(\frac{1}{\Delta t} [L] + \frac{1}{2} [R] \right)^{-1} \left\{ \left(\frac{1}{\Delta t} [L] - \frac{1}{2} [R] \right) [I_1^{n+1/2}] \right. \\ & \quad \left. - \frac{1}{\Delta x} [V_2^{n+1}] + \frac{\Delta x}{2} \sum_{m=1}^{N_{x+1}} \left([v_m^{n+3/2}] + [v_m^{n+1/2}] \right) \right\} \end{aligned} \quad (25)$$

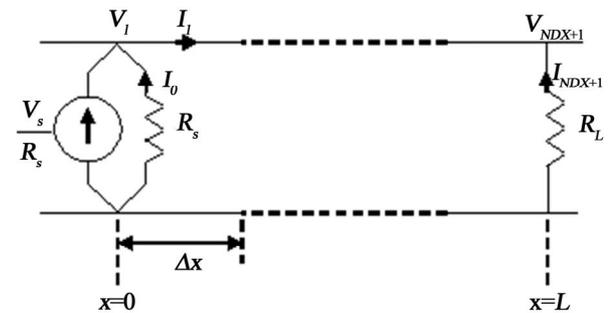


Figure 4. Voltage and current solution points. Spatial discretization of the line showing location of the interlaced points.

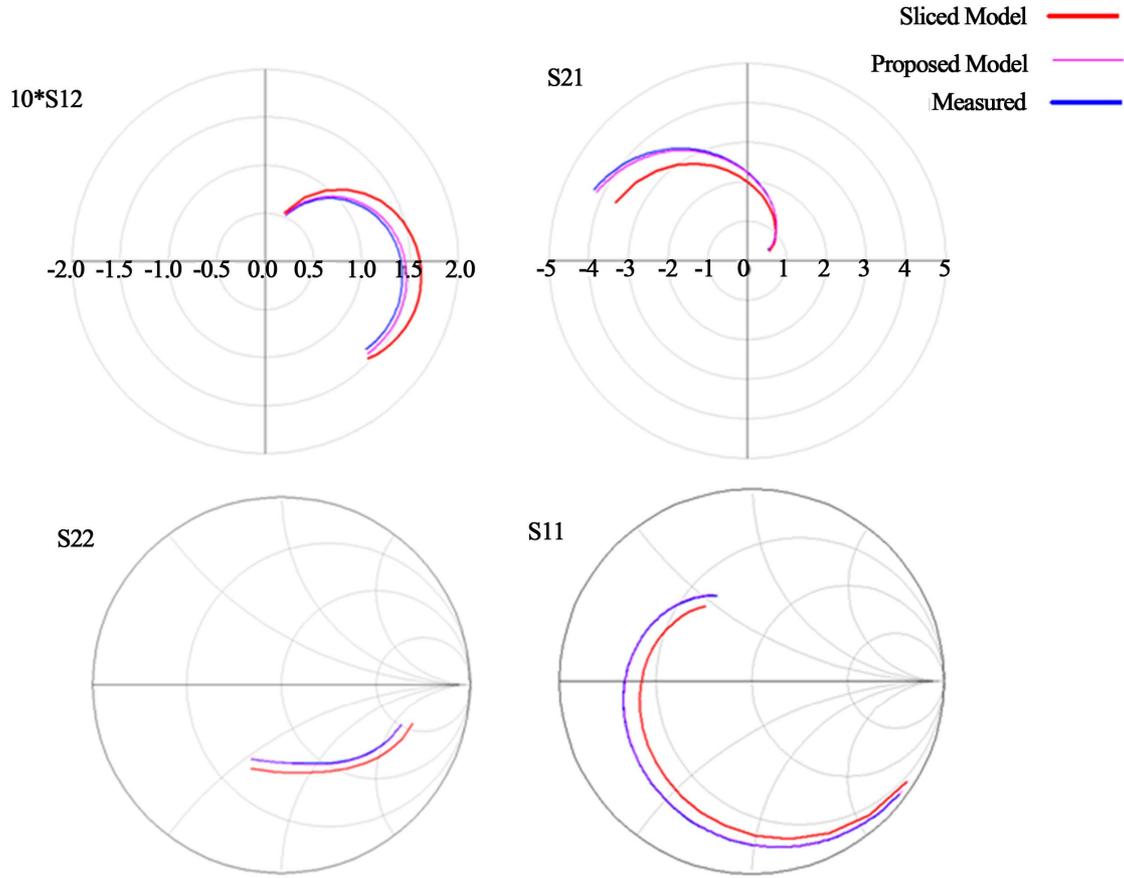


Figure 5. Comparison between S-parameters of NE710 for sliced, proposed distributed model and measurements.

$$\begin{aligned}
 & \left[I_{N_x}^{n+3/2} \right] \\
 &= \left(\frac{1}{\Delta t} [L] + \frac{1}{2} [R] \right)^{-1} \\
 & \times \left\{ \left(\frac{1}{\Delta t} [L] - \frac{1}{2} [R] \right) \left[I_{N_x}^{n+1/2} \right] \right\} \\
 & - \frac{1}{\Delta x} \left[V_{N_x}^{n+1} \right] + \frac{\Delta x}{2} \sum_{m=1}^{N_x+1} \left(\left[v_m^{n+3/2} \right] + \left[v_m^{n+1/2} \right] \right) \}
 \end{aligned} \quad (26)$$

Finally, the currents of the short-circuited ports can be determined as

$$\begin{aligned}
 \begin{bmatrix} I_1^{n+1/2} \\ I_{N_x}^{n+3/2} \end{bmatrix} &\cong \begin{bmatrix} A & B \\ A & B \end{bmatrix} \begin{bmatrix} \sum_{m=1}^{N_x+1} \left(\left[j_m^{n+1} \right] + \left[j_m^n \right] \right) \\ \sum_{m=1}^{N_x+1} \left(\left[v_m^{n+3/2} \right] + \left[v_m^{n+1/2} \right] \right) \end{bmatrix} \\
 &= [K] \begin{bmatrix} \sum_{m=1}^{N_x+1} \left(\left[j_m^{n+1} \right] + \left[j_m^n \right] \right) \\ \sum_{m=1}^{N_x+1} \left(\left[v_m^{n+3/2} \right] + \left[v_m^{n+1/2} \right] \right) \end{bmatrix}
 \end{aligned} \quad (27)$$

with

$$\begin{aligned}
 [A] &= \left(\frac{1}{\Delta t} [L] + \frac{1}{2} [R] \right)^{-1} \left\{ \left(\frac{1}{\Delta t} [L] - \frac{1}{2} [R] \right) \left(\frac{\Delta x}{2} \right)^2 \right\} \\
 [B] &= \left(\frac{1}{\Delta t} [L] + \frac{1}{2} [R] \right)^{-1} \left(\frac{\Delta x}{2} \right)
 \end{aligned}$$

The admittance noise correlation matrix of the six-port FET noise model is then equal to

$$\begin{aligned}
 & [C Y_{tr}] \\
 &= \left\langle \begin{bmatrix} I_1^{n+1/2} \\ I_1^{n+3/2} \end{bmatrix} \begin{bmatrix} I_1^{n+1/2} \\ I_1^{n+3/2} \end{bmatrix}^+ \right\rangle \\
 &= \left\langle \left([K] \begin{bmatrix} \sum [j_n] \\ \sum [v_n] \end{bmatrix} \right) \left([K] \begin{bmatrix} \sum [j_n] \\ \sum [v_n] \end{bmatrix} \right)^+ \right\rangle \\
 &= [K] \times [C A_{UPL}] \times [K]^+
 \end{aligned} \quad (28)$$

4. Numerical Results

The proposed approach was used to model a sub micrometer-gate FET transistor (NE710). The device has a $0.3 \times 560 \mu\text{m}$ gate. The input and output nodes were

connected to the beginning of the gate electrode and at the end of the drain electrode, respectively. The transistor was biased at $V_{ds} = 3$ V and $I_{ds} = 10$ mA. The obtained S-parameters of the transistor over a frequency range of 1-26GHz from the sliced model, the proposed fully distributed model and measurements are plotted in **Figure 5**.

As expected, our distributed model is more close to measurements than the slice model, especially at the upper part of the frequency spectrum, when the device physical dimensions are comparable to the wavelength. **Figure 6** shows the noise figure obtained for three different sets of data.

To further prove the accuracy of the proposed wave approach in noise analysis, our results were successfully compared to measurements as well as to those obtained by the sliced model, highlighting the advantage of our

model over this later (**Figure 7**). Thus, the proposed wave analysis can be applied for accurate noise analysis of FET circuits.

5. Amplifier Design and Analysis

To validate our proposed FET model, a three stage distributed FET amplifier was designed. In this work we considered a Pi-gate FET transistor suitable for low-noise applications. The topology of the gate and drain lines for transmission line modeling is shown in **Figure 8** while the amplifier layout is shown in **Figure 9**.

The obtained power gain and minimum noise figure of the amplifier are shown in **Figures 10** and **11**, respectively. As we observe there is good agreement between the proposed model and measurements as compared with the sliced model.

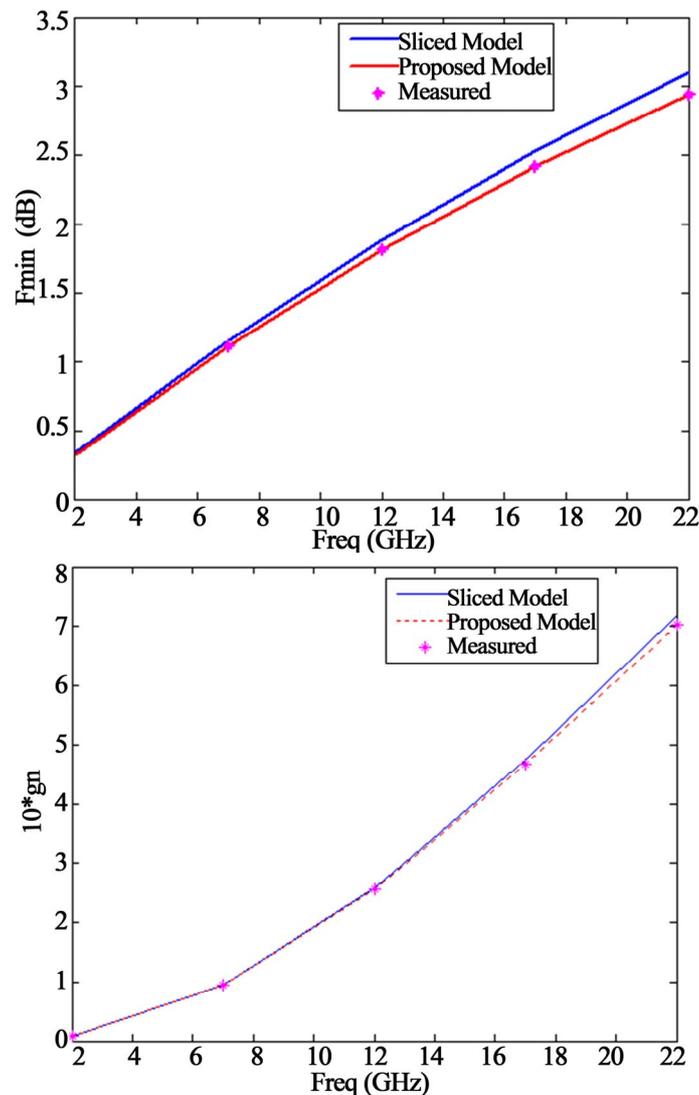


Figure 6. Comparison between normalized equivalent noise admittance and noise figure of FET for sliced, proposed distributed model and measurements.

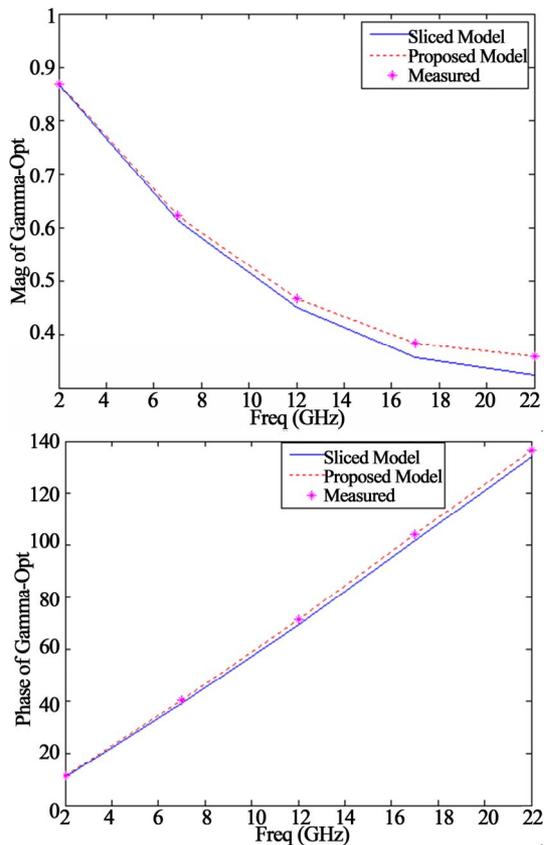


Figure 7. Comparison between the results of slice modeling, proposed model and measured values of amplitude and the phase of optimum reflection coefficient.

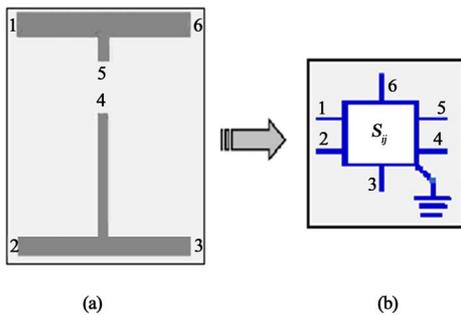


Figure 8. (a) Gate and drain lines topology; (b) Equivalent wave model.

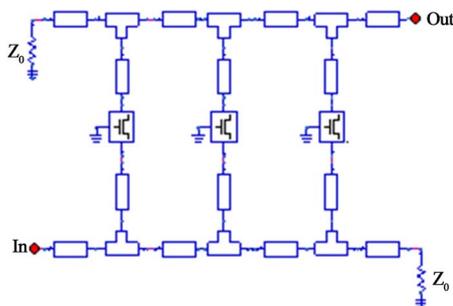


Figure 9. Designed three-stage distributed amplifier.

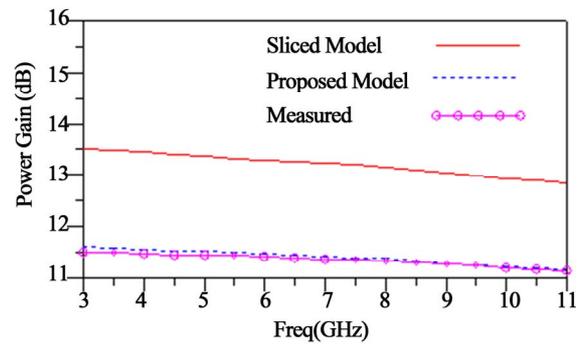


Figure 10. Power gain comparison for measured, proposed model and sliced model for distributed amplifier.

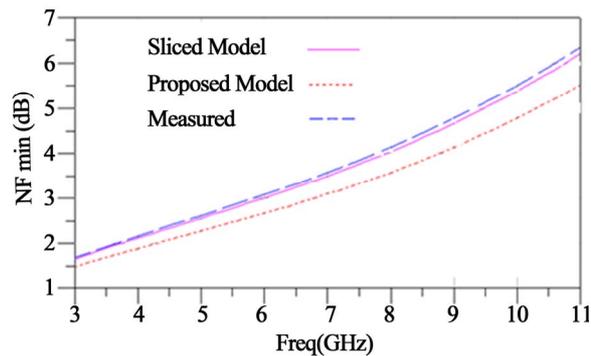


Figure 11. Minimum noise figure comparison for measured, proposed model and sliced model for distributed amplifier.

6. Conclusion

A new modeling approach for signal and noise analysis of high frequency transistors was presented. This method can accurately take into account the effect of wave propagation along the device electrodes. The promising model can be applied to solve issues related to simultaneous signal and noise analysis, as well as in modeling traveling wave FETs in which the gate width is much higher than that of a usual FET

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