Engineering, **2013, 5, 142-145**
doi:10.4236/eng.2013.51b026 Published Online January 2013 (http://www.SciRP.org/journal/eng)

Design of DC-DC Converter for Flash Memory IPs

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Received 2013

Abstract

A DC-DC converter for flash memory IPs performing erasing by the FN (Fowler-Nordheim) tunneling and programming by the CHEI (channel hot electron injection) is designed in this paper. For the DC-DC converter for flash memory IPs using a dual voltage of VDD (=1.5V±0.15V)/VRD (=3.1V±0.1V), a scheme of using VRD (Read Voltage) instead of VDD is proposed to reduce the pumping stages and pumping capacitances of its charge pump circuit. VRD (=3.1V±0.1V) is a regulated voltage by a voltage regulator with an external voltage of 5V, which is used as the WL activation voltage in the read mode and an input voltage of the charge pump. The designed DC-DC converter outputs positive voltages of VP6V (=6V), VP8V (=8V) and VP9V(=9V); and a negative voltage of VM8V (=-8V) in the write mode.

Keywords: Flash memory; CHCI, DC-DC converter, charge pump, low-voltage

1. Introduction

As a market for MCU (microcontroller unit) applied products such as mobile devices, household appliances, and so on grows continuously, the need of small-area non-volatile memories is also stressed [1]. As shown in Fig. 1, flash memories are applied to products requiring a memory capacity of more than 1 Mbits as a non-volatile memory [2].

An EEPROM cell of the SSTC (side-wall selective transistor cell) scheme was proposed as a small-area design technology [2]. The SSTC EEPROM cell has a structure that the CG (control gate) surrounds the sides of the FG (floating gate). The conventional EEPROM cell has a disadvantage that a cell size becomes bigger since an SL (source line) should be laid out to the cells on two adjacent rows. The cell size can be reduced by the common source method joining the SLs of the selected byte instead of joining SL contacts every two rows. A flash cell adapting the common source scheme modifying the SSTC structure in addition to erasing by the FN (Fowler-Nordheim) tunneling and programming by the CHEI (channel hot electron injection) can be implemented.

In this paper, a DC-DC converter for a flash memory cell erased and programmed by the CHEI method is designed. To reduce the pumping stages and pumping capacitances of charge pump circuit for the DC-DC converter using a low voltage of 1.5V±10% as a logic voltage

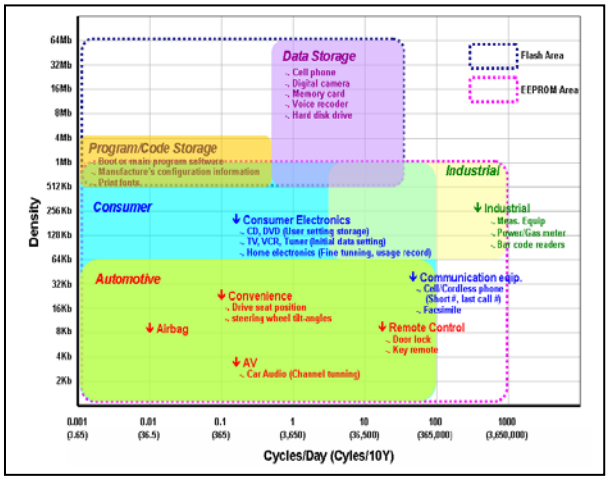


Figure 1. Required number of write cycles and memory capacity for each application product.

in case of flash memory IPs, a scheme to use VRD (read voltage) instead of VDD as an input voltage is proposed. VRD (=3.1V±0.1V) is a regulated voltage by a regulator with an external voltage of 5V and is used as the WL activation voltage in the read mode and an input voltage of the charge pump. The designed DC-DC converter outputs VP8V(=8V) and VM8V(=-8V) in the erase mode; and VP6V(=6V) and VP9V(=9V) in the program mode.

2. Circuit Design

As shown in Fig. 2(a), an EEPROM cell of SSTC structure has a structure that the CG (control gate) surrounds the sides of the FG (floating gate) [3]. An insulating material ONO (oxide-nitride-oxide) is used between the CG and the FG to raise the coupling ratio. The oxide of the SSTC EEPROM cell consists of a thin tunnel oxide of 92Å and a thick oxide of 300Å. A DNW (Deep N-well) surrounding the HPW is needed for isolation of the SSTC EEPROM cell since the HPW is applied with a high voltage of 14V in the erase mode. The thick gate oxide transistor is a HV select transistor. The operation that electrons are ejected from the FG is erasing and the operation that electrons are injected to it is the programming. Erasing and programming are done by the FN (Fowler-Nordheim) tunneling through the tunnel oxide under the FG of the EEPROM cell. As shown in Fig. 2(b), the conventional EEPROM cell has a disadvantage that a cell size becomes bigger since an SL (source line) should be laid out to the cells on two adjacent rows.

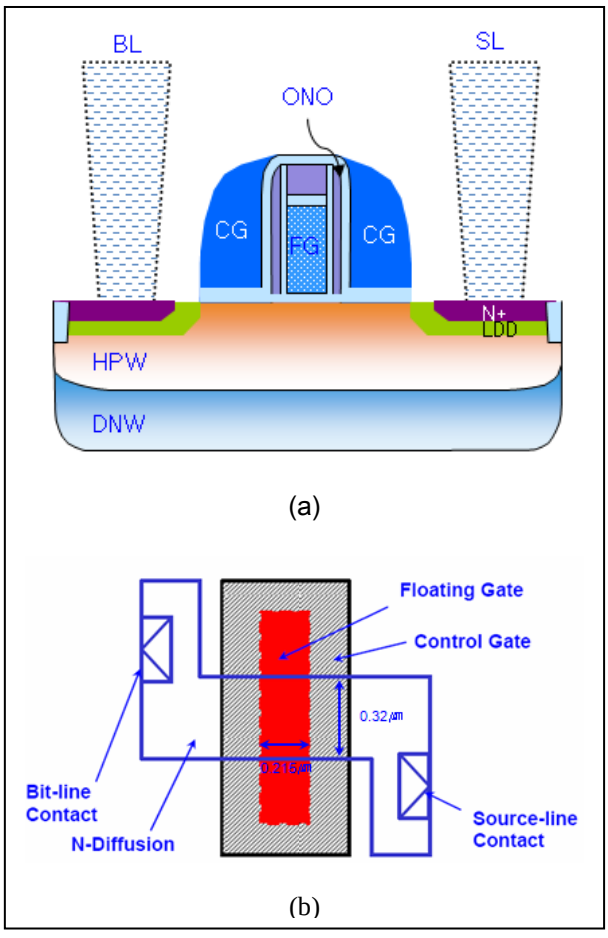


Figure 2. Conventional EEPROM cell: (a) cross-sectional view and (b) layout plot.

The cell size can be reduced by the common source method joining the SLs of the selected byte instead of joining SL contacts every two rows. Flash memory cell of common source scheme can be erased by the FN (Fowler-Nordheim) tunneling and be programmed by the CHEI (channel hot electron injection). Bias voltage conditions at each node of the flash memory cell is shown in Table 1. 8V and –8V are required in the erase mode; and pumping voltages of 6V and 9V are required in the program mode.

Table 1. Bias voltage conditions at each node of a flash memory cell of common source scheme.

		Program		Erase		Read	
		Sel.	Nonsel	Sel.	Nonsel	Sel.	Nonsel
CG	Sel.	9V	9V	-8V	-8V	VRD	VRD
	Nonsel	0V	0V	0V	0V	0V	0V
Bit line		6V	0V	Floating	Floating	VDD	Floating
Source Line		0V	0V	Floating	Floating	0V	0V
HVP-Well		0V	0V	8V	0V	0V	0V
Deep N-Well		VRD	VRD	8V	0V	VRD	VRD

Fig. 3 shows a two-phase three-stage Dickson charge pump generating VP8V (=8V). VRD is used as an input voltage and a MIM (metal-insulator-metal) capacitor as a pumping capacitor. The output voltage is VP8V. For the designed VPP charge pump, N-type Schottky diodes with lower cut-in voltage than their PN junction counterparts are used to reduce the pumping stages at a lower voltage leading to the smaller size of the charge pump [4]. The anodes of the used Schottky diodes are connected to metal material, Co salicide, and the cathodes to the deep HNW. Thus the Schottky diodes used in the charge pump function as N-type Schottky diodes. Fig. 4 shows a single-phase four-stage Dickson charge pump. The reason that the VP9V is single-phase while the V8V charge pump is two-phase is that the pumping current is enough at a target voltage of 9V.

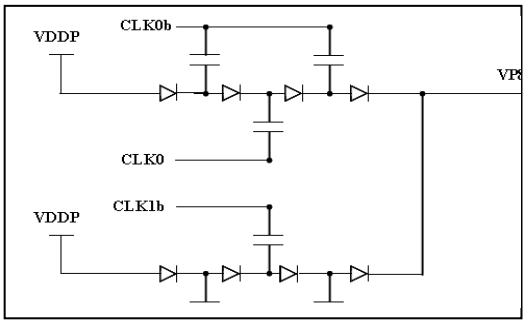


Figure 3. Circuit of two-phase three-stage VP8V charge pump using Schottky diodes.

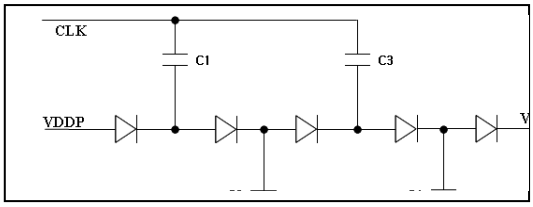


Figure 4. Circuit of single-phase four-stage VP8V charge pump using Schottky diodes.

Fig. 5 shows a VM8V charge pump generating a voltage of –8V which is designed with a four-stage Dickson charge pump using NMOS diodes [5]. VM8V sustains –8V by the negative feedback mechanism.

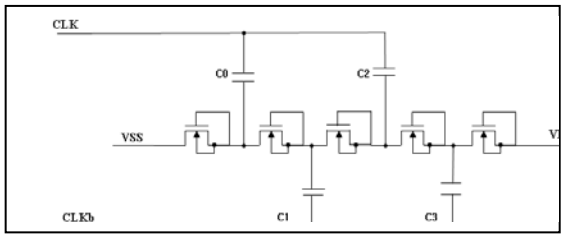


Figure 5. Circuit of four-stage VM8V charge pump using NMOS diodes.

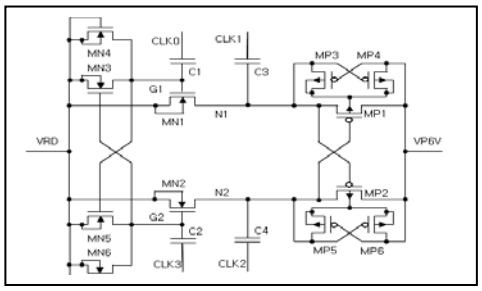
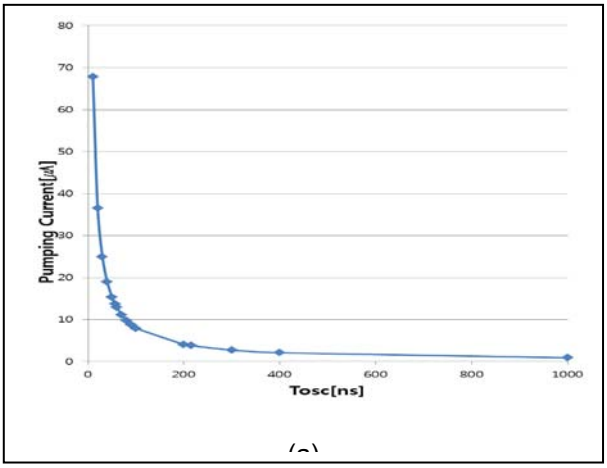


Figure 6. Circuit of two-phase one-stage VP6V cross-coupled charge pump.

3. Simulation Results

- A DC-DC converter for flash memory IPs is designed with a 0.13 ㎛ process. Fig. 6 shows that the pumping current increases as the oscillation period decreases. The ring oscillation periods of the VP8V and VM8V charge pumps are designed to be 100ns and 105ns under the following conditions: VRD=3V, Temp=-40℃, SS (slow NMOS and slow PMOS) model parameters. The pumping currents of VPP and VNN charge pumps at the designed ring oscillation period are 7.9 ㎂ and 5.4 ㎂, respectively. and their ripple voltages 166mV, 77mV, 146mV, and 79mV, respectively. Table 2 shows simulation results of the corresponding pumping currents for the output voltages of the DC-DC converters. We can see that the pumping currents are larger than their target currents.



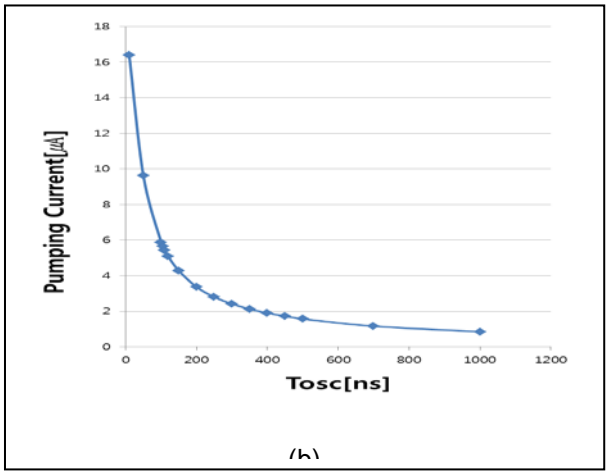


Figure 6. Pumping currents with respect to oscillation periods : (a) VP8V and (b) VM8V.

Table 2. Simulation results of the corresponding pumping currents for the output voltages of the DC-DC converters.

Output Voltage	Target Current	Pumping Current
VP6V	1mA	1.02mA
VP8V	5μA	7.9μA
VP9V	5μA	5.5μA
VM8V	5μA	5.4μA

A simulation result of ripple voltages for VPP and VNN charge pumps is shown in Fig. 7. The ripple voltages are designed to be 77mV for VPP and 79mV for VNN under the conditions: VRD=3.2V, Temp=85℃, and FF (fast NMOS & fast PMOS) model parameters. Table 3 shows simulation results of ripple voltages for the output voltages of the DC-DC converter.

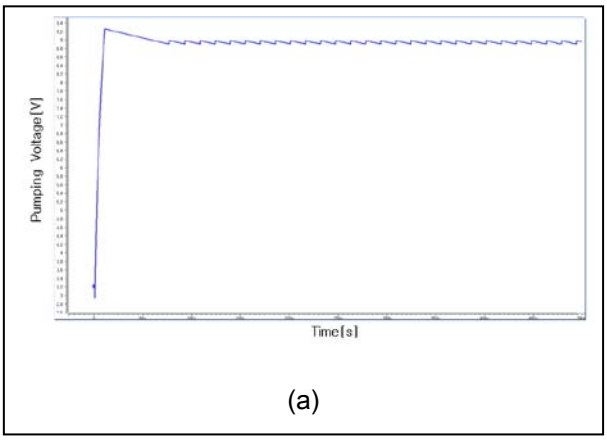


Figure 7. Ripple voltages of charge pumps : (a) VPP and (b) VNN.

Table 3. Simulation results of the corresponding ripple voltages for the output voltages of the DC-DC converters.

Output Voltage	Ripple Voltage
VP6V	166mV
VP8V	77mV
VP9V	146mV

Output Voltage	Ripple Voltage
VP6V	166mV
VM8V	79mV

4. Conclusion

Non-volatile memory IPs are widely used in such applications as smart cards, mobile devices, MCU applied automation products, and so on. Flash memories are applied to products requiring a memory capacity of more than 1 Mbits as a non-volatile memory

In this paper, a DC-DC converter for flash memory IPs in programming flash memory cells with the CHEI method was designed. For the DC-DC converter for flash memory IPs using a low voltage of 1.5V±0.15V as the logic voltage, a scheme of using VRD (read voltage) instead of VDD was proposed to reduce the pumping stages and pumping capacitances of its charge pump circuit. The designed DC-DC converter outputted VP6V (=6V) and VP9V(=9V); and VP8V (=8V) and VM8V (=-8V) in the erase mode. The pumping currents of VP6V, VP8V, VP9V and VM8V charge pumps designed with a 0.13 ㎛ process were 1.02mA, 7.9 ㎂, 5.5 ㎂, and 5.4 ㎂, respectively; and their ripple voltages 166mV, 77mV, 146mV, and 79mV, respectively.

5. Acknowledgements

This work was financially supported by Ministry of Education, Science, and Technology (MEST, Korea) through the fostering project of industrial complex campus.

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