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Advanced Burst Mode Control to Reduce the Standby Power of Flyback Converter

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Abstract

This paper we proposed advanced burst mode control technique to reduce the standby power consumption of the switch mode power supply (SMPS). To reduce the standby power consumption, most of the converter use burst mode or skip mode control technique. However Conventional standby mode control techniques have some problems such as audible noise and poor regulation. In proposed techniques, basically, the burst mode control technique is employed to reduce the fundamental switching frequency while limiting the peak drain current. But, in proposed technique, to improve the regulation characteristic, burst period of the proposed technique is shorter than that of the conventional burst mode technique. And also, to reduce the switching loss increase due to the short burst period, burst switching signal of the proposed technique is partially skipped. By using proposed advanced burst mode control technique, calculated standby power is 0.695W while standby power of the conventional burst mode control is 1.014W.

Keywords: Standby power**,** Flyback converter, PWM IC, SMPS

1. Introduction

Many electrical and electronics devices operate in low power or standby power mode, in readiness for an externally activated signal. This external signal can be activated by remote control, network connection, etc. Recently, the standby mode is widely adopted for many kinds of applications as users require devices that are always available and can be remotely turned on and off. Electronic devices operate in standby mode are always on and consumes some electric energy required to supply the micro-controller and other standby circuitry [1].

According to the report from Lawrence Berkley National Laboratory (LBNL), the standby power in many countries accounts for more than 10% ~ 15% of national residential electricity use [2-3].

Due to the necessity of standby power reduction in electronic devices, many kinds of standby power control techniques such as burst mode control, skip mode control, etc., were invented. However, these kinds of techniques have some disadvantages as shown in table 1 [4].

In this paper, advanced burst mode control technique to reduce the standby power consumption is proposed. In proposed techniques, basically, the burst mode control technique is employed to reduce the fundamental switching frequency while limiting the peak drain current. But, in proposed technique, to improve the regulation characteristic, burst period is shorter than that of the conventional burst mode technique. And also, to reduce the switching loss increase due to the short burst period of the proposed technique, burst switching signal is partially skipped. By using proposed advanced burst mode control technique, calculated standby power is 0.695W while standby power of the conventional burst mode control is 1.014W.

Table 1. Conventional standby mode control method

doMe	egatnavdA	egatnavdasiD
edom pikS	noitaluger dooG	elbidua hgiH esion
edom tsruB	elbidua woL esion	noitaluger rooP

2. Power loss of the converter

Figure 1 shows conventional circuit of the AC-DC flyback converter. When converter operates in standby

mode, most of the power loss comes from passive component such as resistor, inductor etc., and switching device such as power MOSFET. Generally, because of the fundamental characteristics and poor controllability of the passive component, power loss of the passive component is hard to reduce. Therefore, most of the standby power reduction techniques focused on reducing power loss of the switching device. In this section, we analyze the source of the power loss of the converter and proposed novel standby power control technique to reduce the standby power loss without characteristic degradation of the converter.

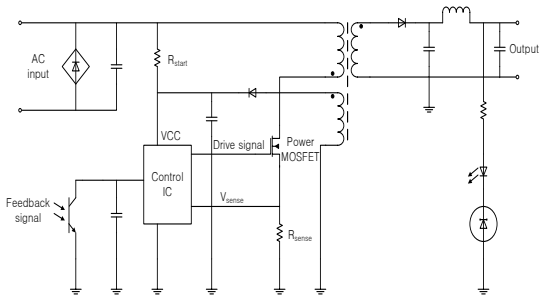

Fig. 1 Conventional AC-DC flyback converter

2.1. Source of power loss

Power loss in start-up resistor

Before PWM IC begins operating, the VCC capacitor is charged through the start-up resistor (R_{start}). And this resistor consumes power when PWM IC starting. Equation (1) shows the power loss in start-up resistor.

$$P_{loss} = \frac{(\sqrt{2}Vin - VCC)^2}{R_{start}} \tag{1}$$

Switching loss from switching device

When converter operates in standby mode, due to the switching loss from switching device such as power MOSFET, converter consumes standby power. Switching loss is comprised of driving loss from the gate drive circuit of the PWM IC and capacitive turn-on loss from power MOSFET.

Driving loss depends on total gate charge, gate to source voltage and operating frequency.

$$P_{loss} = Q_{gate} \times V_{gs} \times f_{sw} \tag{2}$$

And capacitive turn-on loss depends on MOSFET output capacitance, drain to source voltage and operating frequency.

$$P_{loss} = \frac{1}{2} C_o \times V_{ds}^{\ 2} \times f_{sw} \tag{3}$$

Power loss in PWM IC

PWM IC also consumes standby power and it depends on operating voltage and current.

$$P_{loss} = VCC \times I_{op} \tag{4}$$

Table 2 shows specification of the commercial switching device and control IC for flyback converter. By using this specification and equation (1) ~ (4), we can calculate standby power loss of the conventional flyback converter.

Table 2. Simple specification of switching device and control IC

gnihctiwS ecived	Output capacitance : 200pF Input Charge : 63nC Rds(ON) : 0.85 ohm
CI lortnoC	Driving signal voltage : 15V Operating frequency : 50kHz Duty ratio : 87% Operating current : 3mA
Start-up resistor	200kohm

Calculated standby power loss of the conventional flyback converter is about 1.014W.

2.2. Conventional standby power control technique

Start-up circuit

As mentioned in the previous section, start-up resistor consumed power when PWM IC starting. To reduce power loss from the start-up resistor, it is needed to replace it to internal current source which consist of high voltage device such as JFET. Before PWM IC starting, the internal current source supplies the internal bias and VCC capacitor. After VCC capacitor is charged, internal current source is disabled and PWM IC begins switching.

Reducing the switching frequency of driving signal

Figure 2 shows reducing the switching frequency of the driving signal techniques which is widely used to reduce the switching losses in the power MOSFET and hysteresis losses in the transformer.

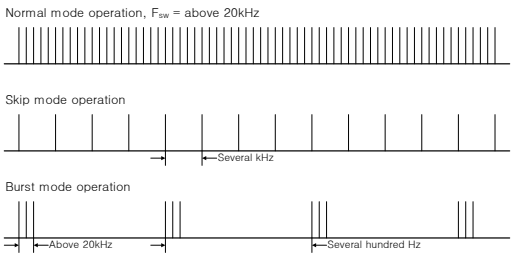

Fig. 2 Frequency reduction technique

However, reducing the switching frequency lowers switching loss in power MOSFET, it also cause a problem such as audible noise or poor regulation of the converter output. To reduce the audible noise, it is needed to limit the peak drain current. However, it also lowering the converter efficiency. Therefore, the optimum value of peak drain current is determined by trade-off between converter efficiency and audible noise. And also, to reduce the poor regulation problem, it is required to increase the period of switching signal from several hundred Hz to several tens Hz or several kHz. But it may cause an audible noise problem or increase the switching losses.

Auxiliary power supply

If the power of the application is higher than 200W, due to the large output capacitance of the power MOSFET which used in high power application, reducing the switching frequency has limitation in lowering switching losses. Therefore, auxiliary power supply is used to reduce the standby power.

Output voltage drop or disconnection

Output voltage drop or disconnection techniques are also used to reduce the standby power of the converter. However, these kind of techniques have some problems such as high cost, lowering the converter efficiency, etc.

2.3. Proposed standby power control technique

As mentioned in the previous section, skip and burst mode control techniques have some disadvantages such as audible noise, poor regulation. Therefore, we proposed advanced burst mode control technique to overcome the problems of the conventional standby mode control techniques without increase of standby power consumption.

In the proposed technique, basically the burst mode control technique is employed to reduce the fundamental switching frequency while limiting peak drain current. However, to improve the regulation characteristic, burst period of the proposed technique is shorter than conventional burst mode control technique. But short burst period means switching losses of the proposed technique is higher than that of the conventional one. So, as shown in the figure 3, switching signal of the proposed burst mode operation is partially skip to reduce the switching losses. Averagely, minimum 60% of the conventional burst mode switching signal is skipped.

Figure 4 shows switching signal of the conventional (lower side) and proposed (upper side) burst mode operation as a function of feedback voltage variation. When converter operates in standby mode, conventional burst mode technique generates switching signal when feedback voltage decreasing phase (inside of the dashed line). However, proposed burst mode technique generates switching signal when both side of feedback voltage increasing and decreasing phase (inside of the straight line). So, regulation characteristic of the proposed technique is improved. And also, as mentioned above, switching signal of the proposed burst mode operation is partially skip, standby power consumption is not increase.

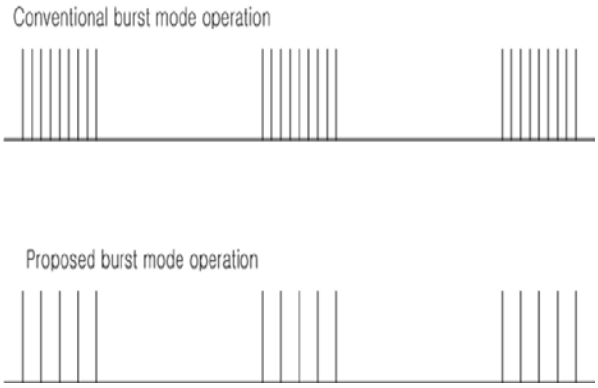

Fig. 3 Switching signal of the conventional and proposed burst mode operation

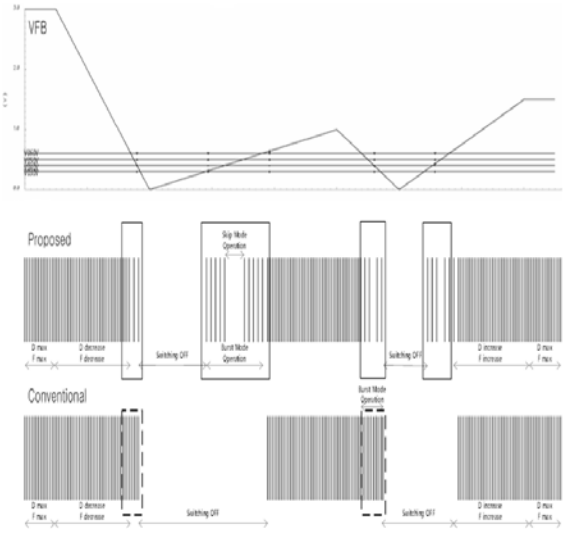

Fig. 4 Switching signal of the proposed and conventional burst mode as a function of feedback voltage

3. Schematic and simulation result of the proposed burst mode control

Schematic of the proposed burst mode control

Control part of the proposed burst mode control technique is composed of four comparators (COMP1 ~ COMP4) and two gates as shown in figure 5. Each of the comparators has different reference voltage. Table 3 shows reference voltages of the comparators.

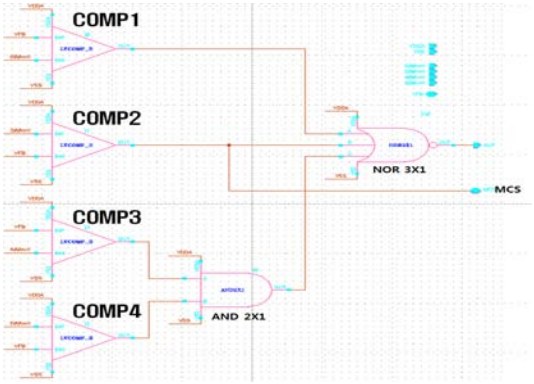

Fig. 5. Schematic of the proposed burst mode control

Table 3. Reference voltages of the comparators

rebmun rotarapmoC	egatlov ecnerefeR
1PMOC	600mV
2PMOC	300mV
3PMOC	400mV
3PMOC	500mV

PWM IC enters advanced burst mode operation when feedback voltage drops below 600mV. Switching continues until feedback voltage drops below 500mV. And switching is partially skipped until feedback voltage drops below 400mV. After feedback voltage drops below 400mV, switching resumes until feedback voltage drops below 300mV. When feedback voltage drops below 300mV, switching stops and the output voltage of the converter starts to drop. This causes the feedback voltage to rise. When feedback voltage rises above 300mV, switching resumes. If switching skip period is long, feedback voltage possibly rise due to the possibility of the converter output voltage drop. However, switching skip period is too short and switching resumes again before converter output voltage starts to drop. So, feedback voltage drops until it passes 300mV. After the feedback voltage drops below 300mV, as mentioned above, feedback voltage rise. Burst mode witching starts when rising feedback voltage passes 300mV and continues until feedback voltage reaches 600mV. When feedback voltage rise above 600mV and converter still operates in standby mode (means light or no load), feedback voltage then falls and the advanced burst mode process repeats.

Simulation result

Figure 6 shows simulation result of the proposed burst mode control circuit.

As shown in the figure, when feedback voltage drops below 600mV, burst mode operation starts. And it continues until feedback voltage drops below 300mV. As mentioned previous section, to reduce the switching losses, burst mode switching signal is partially skipped.

By using parameters from table 1 and proposed advanced burst mode control technique, calculated standby power is about 0.695W. However, about 60% of the calculated standby power comes from the start-up resistor. So, if we replace the start-up resistor to high voltage current source then calculated standby power may be lower than 0. 3W.

Fig. 6 Simulation result of the proposed burst mode control circuit

4. Conclusion

In this paper, we proposed advanced burst mode control technique to reduce the standby power of the converter. In proposed advanced burst mode control technique, burst period is shorter than conventional burst mode control to improve the regulation characteristic and burst switching signal is partially skipped to reduce the switching losses. Calculated standby power consumptions are 0.695W and 1.014W for the proposed advanced burst mode control and conventional burst mode control, respectively, yielding about 30% improvement in the standby power consumption. The standby power consumption can be enhanced to 0.3W for the proposed technique when start-up resistor of the converter is replaced to high voltage current source.

5. Acknowledgements

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