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Fully On-Chip Integrated Photodetector Front-End Dedicated to Real-Time Portable Optical Brain Imaging

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ABSTRACT

Optical brain imaging using functional near infra-red spectroscopy (fNIRS) offers a portable and noninvasive tool for monitoring of blood oxygenation. In this paper we have introduced a new miniaturized photodetector front-end on a chip to be applied in a portable fNIRS system. It includes silicon avalanche photodiodes (SiAPD), Transimpedance amplifier (TIA) front-end and Quench-Reset circuitry to operate in both linear and Geiger modes. So it can be applied for both continuous-wave fNIRS (CW-fNIRS) and also single-photon counting. Proposed SiAPD exhibits high-avalanche gain (>100), low-breakdown voltage (<12 V) and high photon detection efficiency accompanying with low dark count rates. The proposed TIA front-end offer a low power consumption (<1 mW), high-transimpedance gain (up to 250 MV/A), tunable bandwidth (1 kHz - 1 GHz) and very low input and output noise (~few fA/√Hz and few μV/√Hz). The Geiger-mode photon counting front-end also exhibits a controllable hold-off and rest time with an ultra fast quench-reset time (few ns). This integrated system has been implemented using submicron (0.35 μm) standard CMOS technology.

Keywords: Biochip; Analog CMOS Integrated Circuit; Trans-Impedance Amplifier; fNIRS; Brain Imaging; Medical Imaging; Optical Sensors

1. Introduction

Optical sensors and systems are widely applied in biological and biomedical imaging. Optical coherent tomography (OCT), pulse-oximetry, Brillouin scattering (BLS) imaging, Optical dermatology, and spectroscopy are some examples. Common brain monitoring systems are bulky, non-portable and invasive and require sophisticated and expensive hardware and software tools [1], so they are not a proper platform to be developed as a portable brain imaging system. The commonly used non-invasive brain imaging techniques are electro-encephalography (EEG), magneto-encephalography (MEG), positron emission tomography (PET), functional magnetic resonance imaging (fMRI), and functional near-infrared spectroscopy (fNIRS) [2]. Only EEG and fNIRS can be realized using equipment that is small and light enough to be worn continuously while allowing body movements. However some portable EEG systems has been developed currently for brain imaging [3], EEG is not ideal for human-computer interface (HCI) [4], it is susceptible to artifacts from eye and facial movement, as well as near by electronic devices, it requires gel in the participant's hair, it takes time to setup properly and is not spatially determined [5]. We are applying fNIRS to develop a portable tool for real-time brain imaging. fNIRS is a non-invasive, minimally intrusive, safe, and high-temporal resolution imaging technique for real-time and long-term monitoring of the brain function and biological tissues. It is considered as one of the most efficient diagnosis and investigation techniques of different neurological diseases, such as, stroke and epilepsy seizures that require continuous monitoring of the patient at the hospital, which is a costly endeavor. In contrast to the other bulky and high-voltage brain imaging systems suffering from electromagnetic interfaces and slight movement artifacts, fNIRS is portable, low-voltage and immune to electromagnetic interferences with the advantages of ease of use and short setup time [5]. In fNIRS, the brain tissue is penetrated by near-infrared (NIR) radiation and the reflected signal is observed to investigate the brain function. In NIR range (650 nm - 950 nm), water has relatively low absorption while oxy- and deoxy-hemoglobin have high absorption.

Due to these properties, NIR light can penetrate biological tissues in the range of 0.5 - 3 cm allowing investigation of relatively deep brain tissues, and ability to differentiate between healthy and diseased tissues based on their optical properties. The typical CW-fNIRS system consists of NIR light source, photodetector, data

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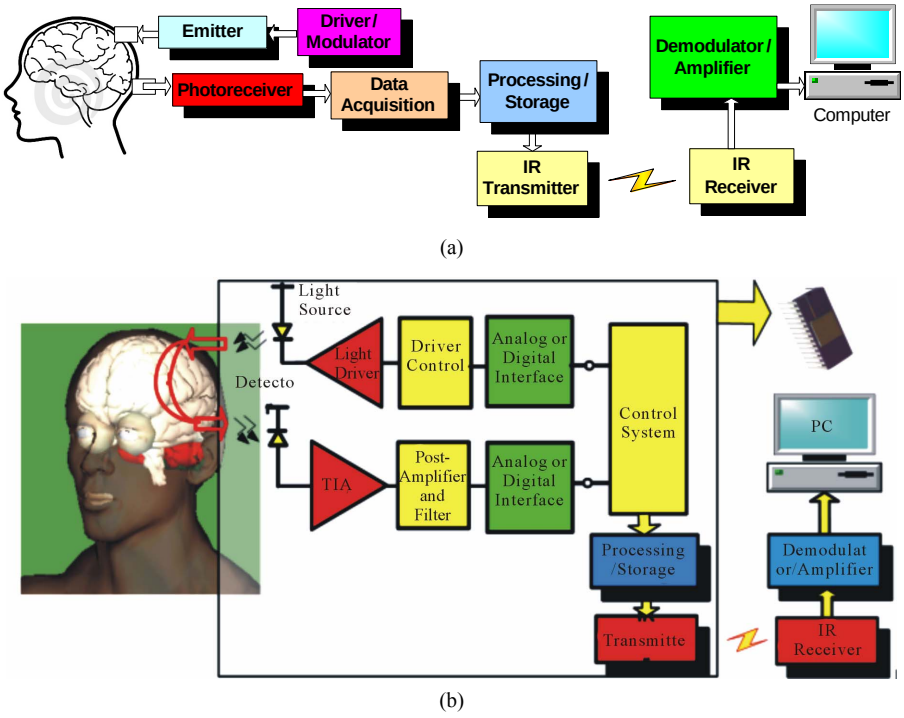

Figure 1. Block diagram of a typical portable wireless fNIRS (a) and the phototransceiver front-end building blocks (b).

acquisition module and control unit, and a processing block (**Figure 1(a)**). The light source is placed on the surface of the head (scalp) and it generates light in the NIR range. Generally, the light sources used for NIRS system are either LEDs or laser diodes that emit NIR light with optical power within a range of 5 mW to 17 mW at discrete wavelengths (for example 735, 840, and 940 nm). The fNIRS photodetector front-end includes a photodetector that monitors the intensity of the reflected NIR signal, Quench-Reset Circuit, Trans-impedance Amplifier (TIA), Limiting Amplifier, post amplifiers and filters (**Figure 1(b)**). Although fNIRS is compact when compared to other brain imaging systems, but current commercially available NIRS devices are still too bulky to be wearable or portable for monitoring brain function. They are not miniaturized enough in order to be integrated with other wireless and portable medical imaging systems intended for bedside real-time brain monitoring. It also suffers from low spatial resolution, high-level noise, susceptible to the internal and ambient light/temperature and bias voltage variations.

In this paper we propose a miniaturized, reconfigurable, low-power, low-noise and high-gain fNIRS photoreceiver for real-time brain imaging. Integrating the photodiode and corresponding circuitries on the same chip and on-chip multi-mode operation using smart CMOS image sensor concept has not been considered yet in literature for fNIRS application. Using smart CMOS image sensor concept for fabrication of photodiode and photodetection circuitry and integrating them on the same chip with ability to work on different modes of operations, leads to a more compact and miniaturized design. Using p+/n-well topology with guard-ring and negative feedback avalanche concept in fabrication of photodiode, we have designed a photodiode with high detection efficiency and low-noise using standard CMOS process. An integrated low-noise, high-gain and low-power photodetector TIA front-end and an ultra-fast quench-reset front-end also have been introduced in this paper.

The remaining parts of this paper are organized as follows. First the implementation of the CMOS photodetector is described at Section 2. The integrated electronics front-ends for linear and Geiger modes of operation are introduced in Sections 3 and 4 respectively. Section 5 depicts the general characteristics of the integrated system.

2. Design of CMOS SiAPDs as Image Sensor

Conventional photodetectors use photon multiplier tubes (PMTs) which are bulky, subtle, sensitive to magnetic fields and require high-supply voltage [6]. The photodiode used in the photodetector requires being highly sensitive, enabling the reliable conversion of the ultra-low amplitude light signal into a detectable electric signal. Silicon avalanche photodiode (SiAPD) is a potential candidate for low-level light detection in the visible and near-infrared regions due to its bias dependent internal

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gain and its ability to amplify the photogenerated signal by avalanche multiplication [7].

The SiAPDs fabricated in dedicated process have two major disadvantages: the production cost is very high due to the specialized fabrication process, and the impossibility to integrate electronic circuits on the same chip. Optimizing the performance of both the CMOS devices and the SiAPD is a challenging task. To overcome these problems, researchers have investigated the design and fabrication of SiAPDs in a standard CMOS process [8,9]. The advantages of standard CMOS fabrication process are: the availability of a fully supported, mature and reliable technology at reasonably low cost, and the possibility of developing a complete system on chip with a high degree of complexity [10-12].

The mandatory requirement for SiAPD fabrication in standard CMOS process is that a suitable subset of CMOS fabrication process flow should be able to build a planar p-n junction without device breakdown at the photodiode periphery. SiAPDs fabricated using standard CMOS process involves high doped p or n layer resulting in shallow or medium depth depletion region. As a consequence, CMOS SiAPDs are inefficient to detect red and NIR photons, and are not suitable for NIR signal detection in neuroimaging. However, to increase the use of SiAPD-based front-end receivers for biomedical applications, integration of the SiAPD and peripheral circuitry on the same chip using standard CMOS technology is highly desired. The fabrication of SiAPDs in standard CMOS technology permits fabrication of both the photodetector and the necessary peripheral circuits on the same chip for an integrated system. This leads to feasibility of implementation of a portable brain imaging system which is highly desired. However, it is challenging to make SiAPDs in CMOS technology due to lack of special fabrication steps [9], the punch-through, high tunneling and premature edge breakdown (PEB) effects [10,13] and also the trade-offs between several design parameters such as scale, shape, doping, noise, efficiency, gain, speed, etc.. High-level noise and low-efficiency of the currently available detectors [7,8], encourages us to design a new SiAPD with low-noise and high detection efficiency at NIR region [13-15].

Here we have designed the p+/n-well SiAPDs with different guard rings (n-well and p-well) in different shapes and scales. These provide a tradeoff between fill factor and angularity and a feasible way to validate the efficiency of the applied guard-rings. The p-well APD is a p+/n-well APD developed in square and octagonal shape with p-well guard ring to preventing PEBs. The guard ring is achieved by low doped p-well around p+ active area with 100 µm diameter (**Figure 2(a)**). Another new photodiode (APD2) which is an n+/p-sub SiAPD with n-well PEB prevention (PEBP) technique (**Figure 2(b)**). It uses the connection between the highly doped n region and the substrate as the active region. Optimization of the performance of SiAPD is done by device level simulation using Sentaurus TCAD software. The active junction of the photodiode exists between p + (N_a = 5 × 10^{19}/cm^3) and deep n-well (N_d = 1.28 × 10^{17}/cm^3). The main characteristics of these APDs are shown in **Table 1**. The photon detection probability (PDP) and the sensitivity of the APDs also are plated and compared in **Figure 3**. The results show a higher PDP and sensitivity of the p-well APD comparing to APD2.

3. Geiger-Mode Front-End Implementation

A diode working in the region near the breakdown voltage can be applied in two different modes of operations: Proportional (linear or amplification) mode and Geiger (digital or trigger) mode. In Geiger mode, SiAPDs work as trigger devices rather than amplifying devices. For operating the SiAPD in Geiger mode (single photon counting mode) quenching and reset circuits are necessary. Generally three types of quenching circuits have been used for Geiger mode operation: passive, active and mixed quenching circuits.

Passive quenching (PQ) is suitable for APDs having small area and small RC time contacts since it can be operated at higher speed. The schematic of two possible configurations of passive quench circuits [16-20] are shown in **Figure 4**. In **Figures 4(b)** and **(c)** the APD cathode voltage and current in response to single photon arrival are plotted. They can also be used with large area devices where high counting rates are not a requirement. Since we require large area APDs for our application that is expected to count photons at high-speed (≥1 MHz), PQ is not a feasible option.

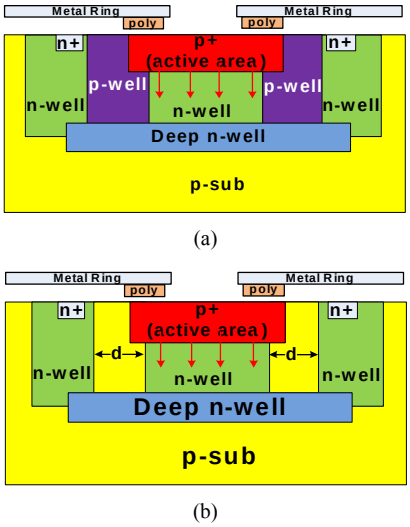

Figure 2. Cross-section of the proposed APDs: (a) The p-well (APD1) and (b) The p-sub (APD2).

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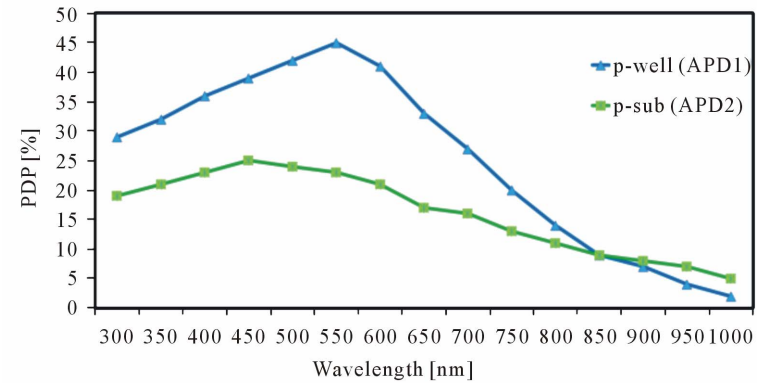
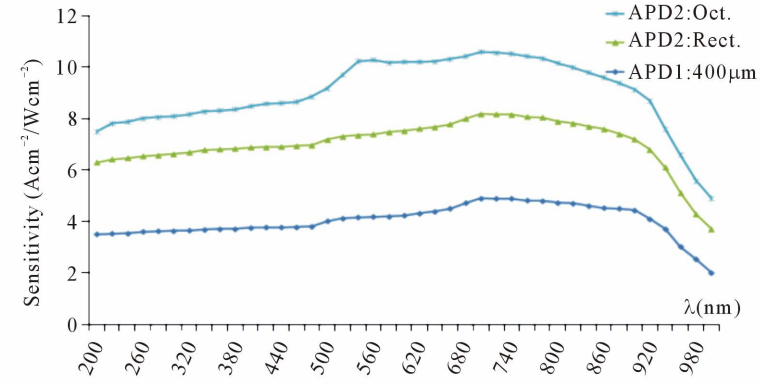
Table 1. The characteristics of the proposed SiAPDs.

Parameter \ Reference	SiAPD			
	p-well (APD1)		p-sub (APD2)	
	Rectangular	Rectangular	Rectangular	Octagonal
Linear Gain	200	220	140	100
Area(~μm^2)	100 × 100	400 × 400	100 × 100	100 ×100
PDE @550 nm	45%	75%	22%	52%
F@M = 20	89@800nm	60@800nm	59@800nm	138@800nm
Impedance (Ω)	600	600	0.5	0.5
Capacitance	1pF	30 pF	1pF	1pF



(a)



(b)

Figure 3. Comparison of different implemented APDs: (a) PDP and (b) Sensitivity.

In order to achieve faster quenching, active quenching circuit (AQC) is used [11]. This method forces back on the APD to drop the bias voltage much quicker enabling significant speed improvements over the PQ method. It causes high accuracy in photon timing. Small delay in quenching the avalanche resulting in fewer carriers crossing the junction and hence low false re-triggering of avalanche (lower after pulse). This also results in lower power loss and hence less heating of the APD. Dead time of the circuit does not depend on the component values and can be accurately controlled, hence determination of precise dead time is possible for satisfactory circuit operation [12]. However, it is difficult to design an effective AQC and it needs extra and complicated ultra-precise circuitry to reduce propagation delays as well as stray capacitances.

Using proposed mixed quench circuit (MQC), depicted in **Figure 5** [12], reduces the required size of load resistor

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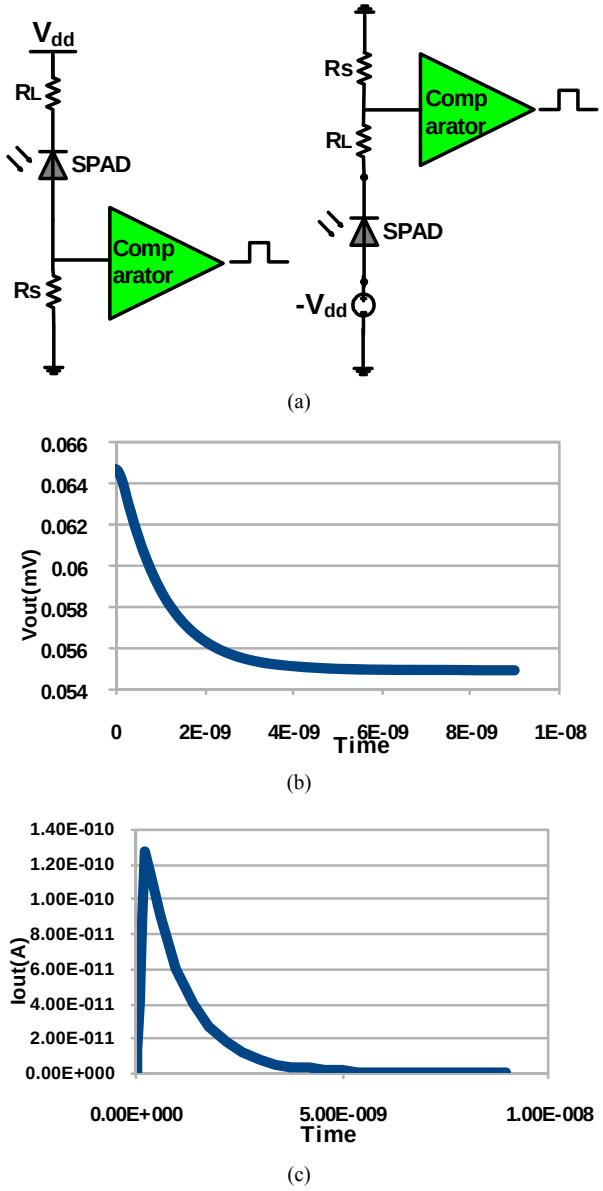

Figure 4. Schematic of the passive quench circuit in two possible voltage and current mode configurations (a) and the APD cathode voltage (b) and current (c) in response to single photon arrival.

(RL) and so the power consumption, charge trapping, after-pulsing and the optical crosstalk and also improve the performance by quicker detection of the photon in a wider dynamic range optical input.

In order to operate the single photon avalanche photodiode (SAPD) in Geiger mode for single photon counting, a quenching circuit and a reset circuit are designed in this stage to be used along with the photodiode. A new, fast, low-noise and high efficient quenching and a reset circuit are designed in this stage by combination of previously applied active and passive techniques. This circuit used along with the photodiode in Geiger mode for higher performance single-photon counting.

In order to make the avalanche quenching as fast as possible, we apply the MQC, as a hybrid approach. **Figure 5** shows the block diagram of the mixed passive-active quenching circuit proposed in [12]. Here, passive quenching is used as the first stage to limit the avalanche current to a low value, followed by the application of a quench pulse during the quench delay time and a reset pulse to recharge the SPAD back to the reverse bias voltage higher than breakdown voltage (V_{BR}).

This method adopts a simpler design while still allowing some control over the dead time and the use of a voltage pulse to speed up quenching. The value of the load resistor that provides the initial passive quenching action can be lower as compared to pure PQ since the actual quenching is done by AQC block [12]. However, the switching delays related to the relatively large parasitic capacitances and high value PQ resistance of the circuit limit the performance and quenching speed of the MQC and it needs more extra complicated circuitry and extra size, but still simpler and with a better performance comparing to the AQC.

Here we develop a new controllable MQC with lower power and lower complexity accompanying with more flexibility and dynamic range of operation by developing an adaptive and faster hold-off time control on the previously proposed MQC. The circuit diagram of the AQC mixed with PQC is shown in **Figure 6**. In quiescence condition, the cathode of SPAD is biased to V_{dd} (usually 5% - 10% above the breakdown voltage for achieving higher sensitivity) through R1 and is ready to detect a photon. The onset of the avalanche current starts a passive quenching action and the voltage drop across R1 reduces the voltage at the SPAD cathode. As such, S_{sense} goes in deeper conduction and the voltage drop caused by R3, turns the quench transistors ($S_{quench1}$ and $S_{quench2}$) ON via $S_{feedback}$. This starts the active quenching action by quickly pulling the SPADs cathode down to ground. This brings the reverse bias of the SPAD below breakdown

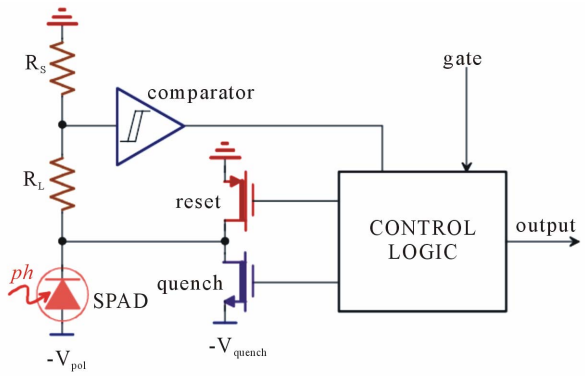

Figure 5. Mixed passive-active quenching circuit proposed by [12].

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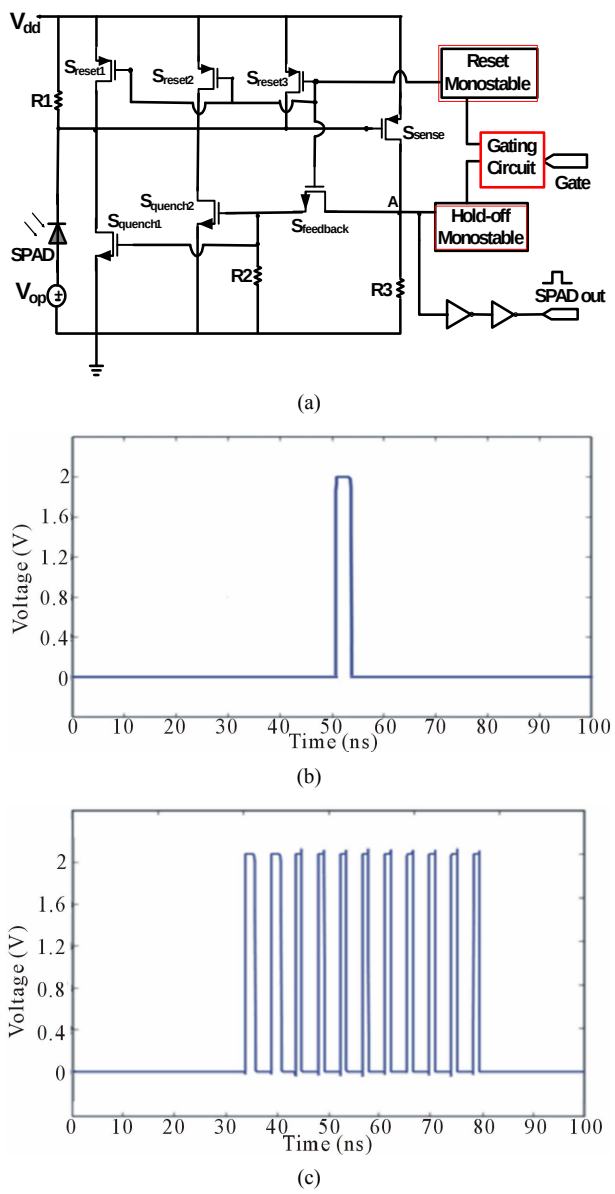

Figure 6. Schematic diagram of the controlled mixed quenching circuit (a) and the APD cathode voltage in response to single photon arrival (b) and multiple-photon arrivals between 35 ns - 80 ns (c).

and the avalanche current quickly dissipates. The quench transistors ($S_{quench1}$ and $S_{quench2}$) are then turned OFF and the three parallel reset transistors (S_{reset1}, S_{reset2}, and S_{reset3}) are turned ON.

The reset transistors are activated by an output pulse from the reset monostable which triggers with the end of the hold-off period. These reset transistors are equivalent of the three low resistance transistors, which resets the quiescent bias of the SPAD and brings the SPAD cathode voltage back to detect the next photon. Short duration of the reset-time decreases the dead-time between photon counts [21-23].

Note that in this circuit the excess voltage V_E, is given by:

$$V_E = V_{dd} + |V_{op}| - V_{BR} \quad (1)$$

where the bias voltage is provided by circuit supply voltage (V_{dd}) and a DC voltage (V_{op}) connected to the APD anode. The SPAD performance is directly proportional to the amount of the excess electric bias voltage above the breakdown voltage. So in additional to the mentioned preferences, MQC can improve the performance comparing to the PQC, due to the significant influence of the V_E on detector performance.

Using this circuit, faster quenching results in lower power loss and hence less heating of the SPAD can be achieved. High power dissipation can drift the breakdown voltage, and change the SPAD response regarding to the detection efficiency and noise. Delayed release of trapped charges due to the large charge trapping in SPAD can retrigger the detector and cause false ignitions (after-pulsing). After-pulsing cause a non-linear distortion in photon counting [18]. Decreasing the avalanche time duration reduces the power dissipation, charge trapping and the optical crosstalk due to the minimization of the hot-carrier photon-emission [16,17].

Because of the complementary action of the AQC in MQC in order to suppress more the initially quenched avalanche by the PQC, there is more flexibility in choosing the PQ load (RL). Therefore by reducing the load resistor RL one can achieve a quicker detection of the photon [17]. By increasing the light intensity received by the APD, the current flow through the diode and the series connected resistor (RL) will also increase. The resulting increased voltage across RL, decreases the bias voltage across the APD, so that the gain of the APD is reduced. Therefore the dynamic range of optical input of the APD will be increased for a fixed dynamic range of output voltage [18].

Here also in order to improve the integrity and compactness, and in order to reduce the power consumption due to the large size of the load resistor in passive quench circuit, the passive quenching is embeded in a CMOS APD structure by adding resistor at the top side of the cathode of photodiode CMOS layout cross-section.

4. Linear Mode Front-End for CW-fNIRS

Based on the mode of operation, we need several amplifiers and processing blocks to operate the photodetector [13]. For linear mode operation, SiAPD requires a transimpedance amplifier (TIA) to convert the input photocurrent into a voltage signal [24,25]. The bias of an APD just near but below a breakdown voltage is referred to as a linear mode operation. At this bias voltage, the gain is high, and the output signal is proportional to the amount

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of scintillation light interacting in the APD. Here we need a transimpedance amplifier in order to amplify the APD current.

Due to the ultra low level and usually high source impedance of fNIRS signals, this amplifier should be established to meet certain basic requirements and must cope with various challenges in order to extract the biopotential signals. The challenges of designing such a TIA for portable biopotential acquisition systems are: High Common Mode Rejection Ratio (CMRR) to reject interference [15], High-Pass Filter (HPF) characteristics for filtering differential DC electrode offset [17], low-noise for high signal quality [18], ultra-low power dissipation (<50 mW) for long-term power autonomy, configurable gain and filter characteristics that suit the needs of different biopotential signals and different applications, high transimpedance gain (>1 k) [26], narrow Bandwidth (around 100 k), high output swing, wide dynamic range, ambient light rejection, and low-voltage operation [13].

There are mainly three TIA structures reported in literature: common-gate TIA, resistive feedback TIA, and capacitive feedback TIA.

Figure 7 shows the schematic of three configurations while the detail description of them can be found in [12]. Common-gate TIA(CG-TIA), usually used in open-loop topology and exhibits low input impedance and high transimpedance gain, however its input noise current and input bias current are high and its BW is also low.

Besides so much works [31-35] on developing a proper photoreceiver amplifier, designing such a proper dedicated front-end for fNIRS has not been considered in the literature yet and none of the reported NIRS detectors provide these features taken together, which is a crucial factor in real-time brain imaging.

Available proposed amplifiers for this case are suffering from a lot of limitations so that trade-off between necessary parameters occurs with the cost of losing reliability and performance. For example reported variable-gain transimpedance amplifiers are difficult to stabilize. The key problem with these designs is that they are based on the traditional two-stage topology consisting of a common-source gain stage followed by an output buffer. Phang *et al*. [5] proposed a TIA combining a sub 1-V current mirror [5,14] and a common-gate TIA based on a current-gain amplifier for optical communication. Achigui *et al*. [4] modified this TIA by adding an Operational Transconductance Amplifier (OTA) with dynamic threshold transistor (DTMOS) for NIRS front-end photoreceiver. All of these designs are based on fixed-gain and only one mode of operation. Reaching high data-rate and high-BW in these designs is also with the cost of small gain, high noise and power-consumption. So the needs for a new design with the ability to overcome these limitations and cover the requirements for a fNIRS photodetector front-end, is a critical issue which we address in this paper. In resistive-feedback TIA (RF-TIA), the transimpedance gain is high and offers the smallest noise specially at high frequencies comparing to other structures, but its BW is limited. Capacitive-feedback TIA (CF-TIA), offers smaller noise at low frequencies but it is noisy at higher frequencies [36,37]. A common-gate configuration is typically chosen as it can tolerate a wide range of SiAPD capacitance. However, resistive feedback architecture has better noise performance and is more attractive when SiAPD models are readily available.

Here we have proposed three new TIAs. The first structure (**Figure 8**) is a combination of common-gate TIA (CG-TIA) and RF-TIA. This new structure offers a low-noise, high-gain and high-BW TIA. The design consists of a current amplifier implemented in a transimpedance configuration. In this circuit (**Figure 8**), we have used the combination of M6-M9 transistors to act as a feedback resistor to minimize the output ripple and omit the extra drawn current. The DC transimpedance gain and the GBW are given by:

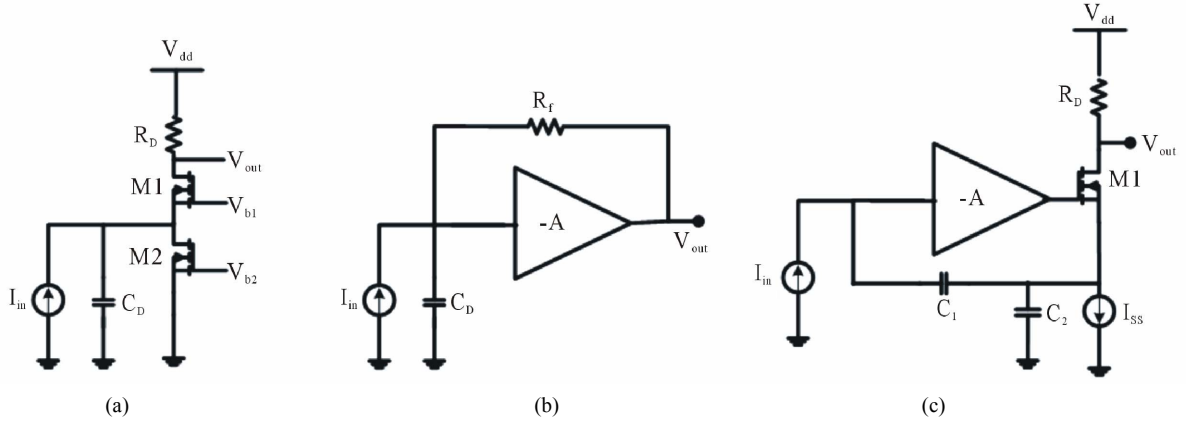

Figure 7. Different TIA structures: (a) Common-gate; (b) Resistive feedback; and (c) Capacitive feedback.

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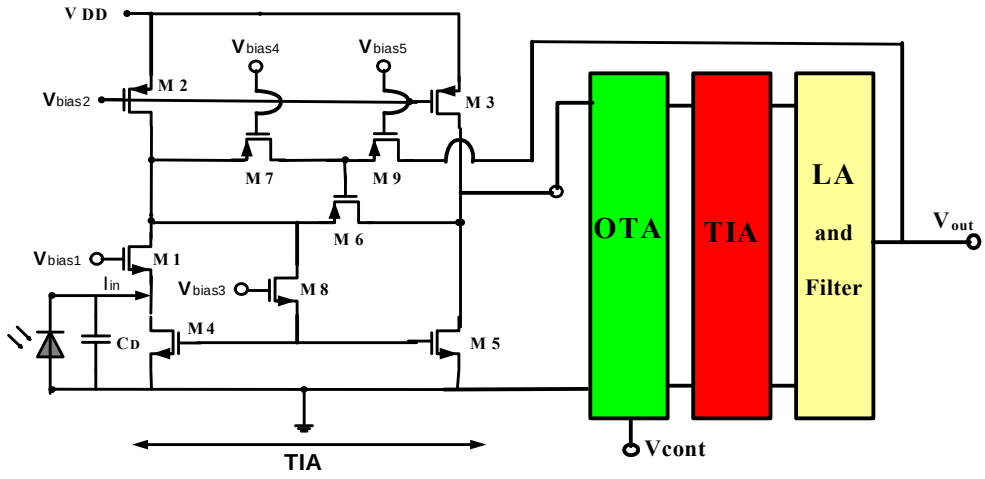

Figure 8. Schematic of the proposed TIA front-end (TIA1).

$$\frac{V_{out}}{I_{in}} = -\frac{g_{M5}R_f - 1}{g_{M4} + g_{M5}} \quad ;$$

$$GBW = \frac{\left(g_{m1} + g_{s1}\right)\left(1 - g_{m5}R_f\right)}{C_{in} + \left(g_{m1} + g_{s1}\right)\left(C_L + C_f\right)R_f / K_{cm}} \quad ; \qquad (2)$$

$$\left(K_{cm} = \frac{g_{m5}}{g_{m4}}\right)$$

where g_{mi} is the transconductance and R_f is the feedback resistance implemented by M6, M7 and M9 biased in the linear region. Bandwidth of TIA increases by decreasing the C_D (~1 pF). In order to boost the voltage swing and match the output impedance to drive the photoreceiver output, a Limiting Amplifier (LA) [12] and a current-mirror OTA [13] are used at the output of the TIA. Using the constant applied voltage of $V_{cont}\left(0\text{ V} < V_{\text{cont}} < 2\text{ V}\right)$, the Gain, BW, power-consumption and dynamic range of the output stage could be changed in a wide desirable output range.

The OTA used in the proposed front-end amplifier design is a current-mirror OTA, which is modified from OTA reported in [3]. Performance of this OTA which is shown in **Figure 9** is highly dependent on the bias current (, and the sizing of the transistors. We have considered these two parameters fairly in order to reach best performance. In order to boost the voltage swing and match the output impedance to drive the photoreceiver output (usually a counter or an analog-to-digital-converter), a LA [6] for post amplification is added to the output of the OTA.

To increase the maximum output swing, and improve the stability of the circuit, we have used a filtering block followed by TIA and LA (**Figure 8**). As mentioned before, one of the main requirements of biosignal amplifiers is to have a wide dynamic range. In order to achieve wide dynamic range, we have considered the proposed photoreceiver circuit as shown in **Figure 8** by adding the ability of parameters tuning. Using the constant applied voltage V_{cont}, the Gain, BW, power-consumption and dynamic range of the output stage could be changed in a wide desirable output range.

Figures 10(a)-(c) show the transimpedance gain, the input and output noise of the proposed circuit in function of frequency variation. Measurements show that the input noise is very low compared to the existing TIAs. Measured output noise is 1.8 μv/√Hz. The power consumption of the front-end circuit is also very low. The TIA has high transimpedance gain and high bandwidth.

The simulation and measurement results of the proposed circuit verify its efficiency and reliability for fNIRS system. By varying the V_{cont} in proposed variable-gain front-end (**Figure 11**), between 0 - 1.5 V, we reached the very-high and fixed value of 45 × E9 for gain-bandwidth product (GBW). This value is tuneable between 10 M and 45 G for various applications. We can reach the transimpedance gain in the range of 2 - 400 MV/A and BW in the range of 1.7 - 5 MHz using this configuration. The power consumption of this circuit is in the range of 0 - 3 mW, which is very convenient for biomedical portable applications. Referring to **Table 2**, the input noise of the proposed design is one of the lowest reported input noises comparing to all similar photoreceiver amplifiers. Measured output noise is also 1.8 μv/√Hz. The output pulse with the maximum swing of 3.3 V is also one of the best indexes to show the appropriateness of the proposed design. In order to verify the effect of the supply voltage, we have also tested the tuneable-gain configuration by increasing the supply voltage to 1 V.

The second TIA structure is a four-stage TIA depicted in **Figure 12**. For cascade TIA in order to reduce the relative noise contribution of the subsequent amplifier stages, the SNR of the first stage should be tuned to be as

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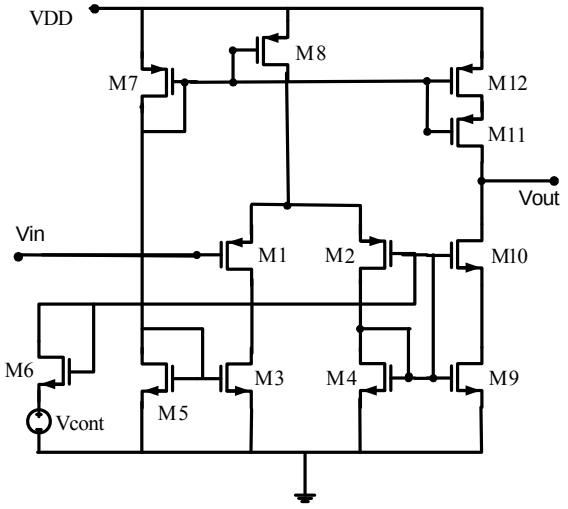

Figure 9. Schematic of the OTA (M1, M2, M9, M10: W/L = 2/0.35 M11, M12: W/L = 10/0.35 and for all other transistors W/L = 1/0.35).

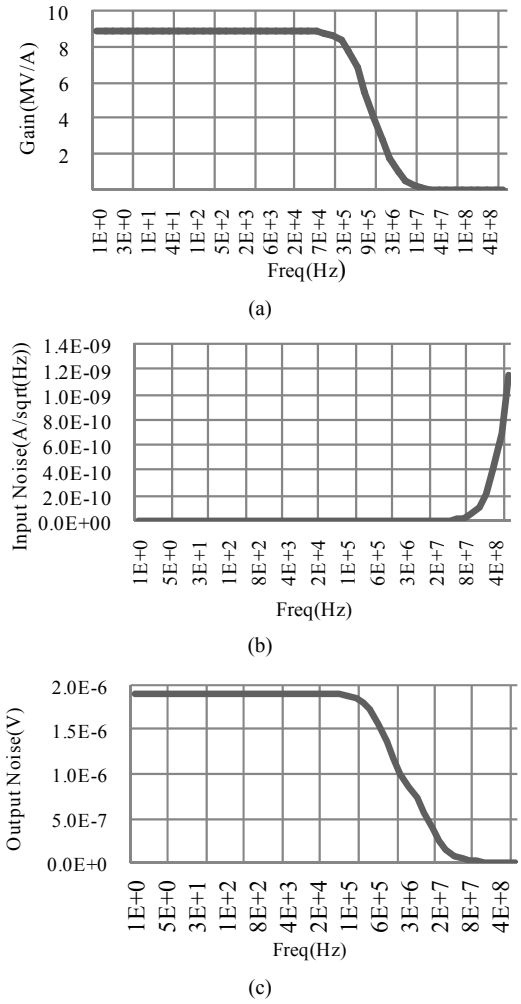

Figure 10. The gain (a), the input noise (b) and the output noise (c) of the proposed circuit shown in Figure 8 at different frequencies.

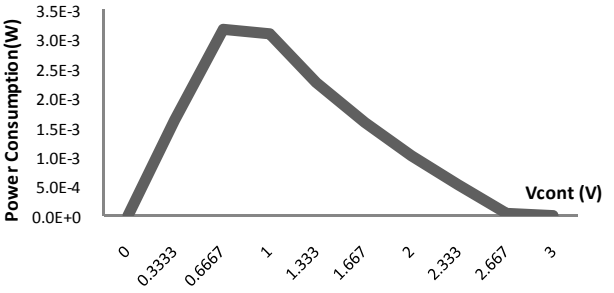

Figure 11. Power-consumption variation with different control voltages.

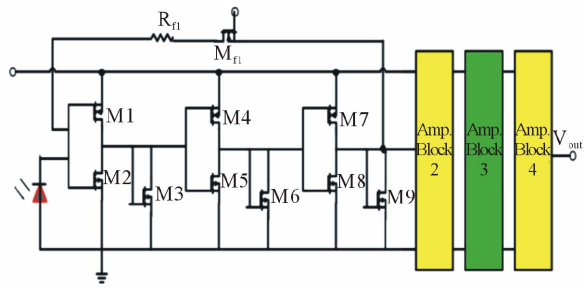

Figure 12. Schematic of the second proposed TIA (TIA2).

large as possible so the feedback transistor (Mf) is placed in series with Rf to reduce the input noise of the TIA by applying different control voltage via V_{cont}. Using the constant applied voltage of V_{cont} at each stage, the Gain, BW, power-consumption and dynamic range of the output could be changed in a vast desirable output range. The DC gain and the BW of a single stage are equal to:

$$A_i = \frac{g_{m1} + g_{m2}}{g_{m3} + g_{ds1} + g_{ds2} + g_{ds3}} \approx \frac{g_{m1} + g_{m2}}{g_{m3}} \; ; \mathrm{BW} = \frac{1 + A_i}{2\pi R C_{in}} \quad (3)$$

where A is the gain and C_{in} is the input capacitance of each stage.

In order to achieve best performance in our design, we have analyzed the sensitivity of each component presented in our design and the best values for optimal sizing are selected. **Figure 13** shows the TIA gain. The output voltage regarding to the sinusoid input with amplitude of 10 μA and its frequency response is depicted at **Figures 14(a)** and **(b)** respectively. The input and output noises are shown in **Figure 15**.

A novel logarithmic TIA (TIA3) also has been designed as depicted in **Figure 16** [38,39]. The later TIA is useful in systems that need scale-invariant and wide dynamic range operation. Its sensitivity to the contrast (AC/DC) of the input and its scale-invariant fractional amplification is beneficial in several applications where percentage changes rather than absolute changes carry information. The previously reported applications of logarithmic TIA in the photodetectors are very limited. But no application of such TIA for fNIRS system has been reported yet in the literature. Here we have proposed a new

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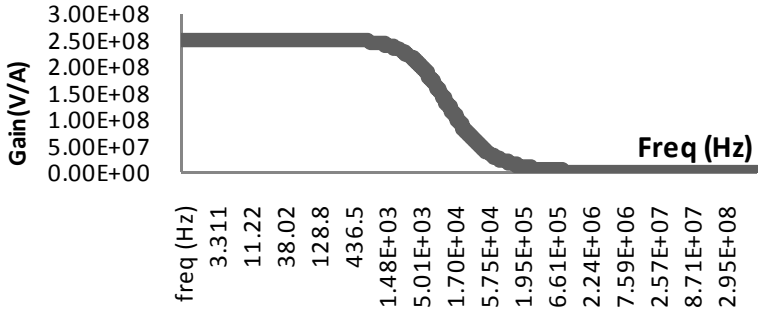

Figure 13. The TIA gain.

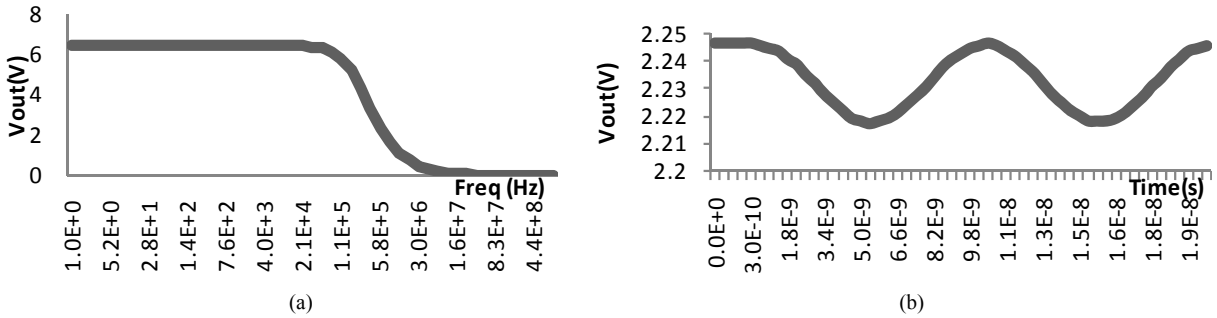

Figure 14. The output voltage (a) and the frequency response of the output stage (b).

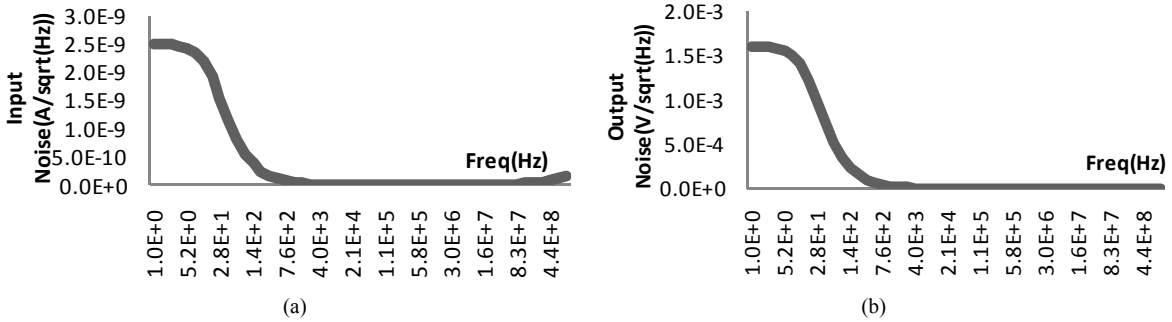

Figure 15. The input noise (a) and the output noise (b) of the proposed circuit.

topology to be applied in fNIRS photodetector front end.

In this circuit, M1 act as the logarithmic amplifier transistor, M6-M7 provides the feedback resistor. M9 acts as a feedback transistor placed directly across the input and output terminals of the current mirror. Using this direct feedback topology, decrease the input impedance seen by the photodiode and improve the speed of the circuit by the cost of the lower output swing. Using logarithmic amplifier makes also the response to a fixed image contrast invariant to absolute light intensity and improves the dynamic range of the photodetector. The performance of the proposed TIA comparing with other works is shown in **Table 2**. Here we have defined the figure of merit (FOM) as GBW/Power dissipation [GHzΩ/mW] to evaluate the efficiency of the proposed TIAs comparing to other works.

5. Integrated Photoreceiver Front-End

The developed photodiode was integrated with photo-detection circuitry and control unit using standard CMOS 0.35 μm technology in order to implement a one-channel photoreceiver including circuits for both linear and Geiger mode. The layout and microphotograph of the designed integrated circuit are depicted in **Figure 17**. This IC only includes the TIA1, TIA2 and the APDs. This IC has been fabricated by TSMC via CMC Microsystems. In order to verify the effect of on-chip integration of APD and TIA, the characteristics of the integrated circuits and devices are measured and compared with discrete components (off-chip separated). **Figure 18** shows the main characteristics of the SiAPDs, normalized for better comparison. The results also show that the main effects of integration are increasing the SNR and sensitivity, while

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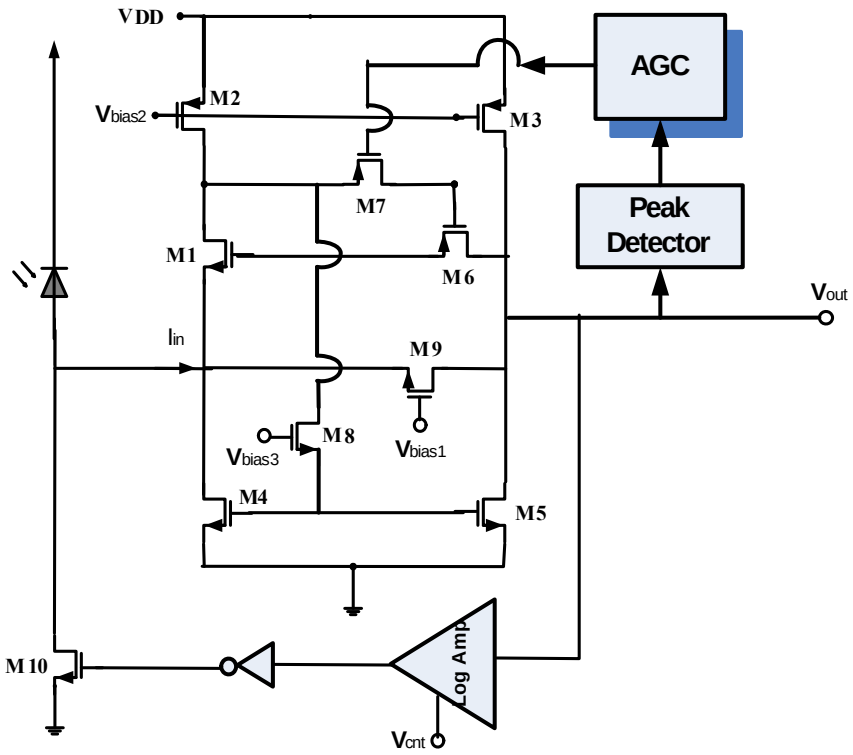

Figure 16. Proposed logarithmic third TIA (TIA3) with ambient light rejection and AGC loops.

Table 2. Comparison of the proposed TIAs with different works.

Ref	Tech	Supply voltage (V)	Power diss. (mW)	Max gain	BW (MHz)	Input noise at 1 kHz (A/√Hz)	GBW/power dis. (GHz Ω/mW)
[3]	0.35	1	1	210 k	50	11 p	10,500
[4]	0.6	3	30	8.7 k	500	4.5 p	145
[8]	0.35	2.5	0.14	1.5 k	110 Hz	-	0.001
[9]	0.18	2	7.2	6.3 k	2500	<10 p	2190
TIA1	**0.35**	**3**	**0.8**	**250 M**	**1000**	**100 f**	**312.5 M**
TIA2	**0.35**	**3**	**4**	**200 M**	**100 K-1**	**280 f**	**62,500**
TIA3 (simulation)	**0.35**	**3**	**0.2**	**300 M**	**2000**	**50 f**	**-**

it doesn't have any significant effect on gain.

6. Conclusion

This paper proposed a miniaturized, reconfigurable and low-noise light detector. It includes low voltage, high efficiency, high-gain avalanche photodiodes in different topologies with maximum sensitivity and minimum noise using standard CMOS 0.35 µm technology. Three new high GBW and low-noise TIA are introduced based on distributed gain concept to be applied in linear operation mode. A high-speed photon counting system includes an ultra-fast quench-reset circuit, pulse generator, monostable and counter with small quenching time and controllable reset time is also proposed. All the components have been designed and evaluated based on the simulation and layout implementation in CADENCE and TCAD. The main characteristics of the APDs are also validated and the impact of each parameter is studied based on the simulation results. The quench-reset circuitries and new implemented APDs with boosted quality and improved efficiency are also currently fabricated and we are now working on test and measurement of these components to

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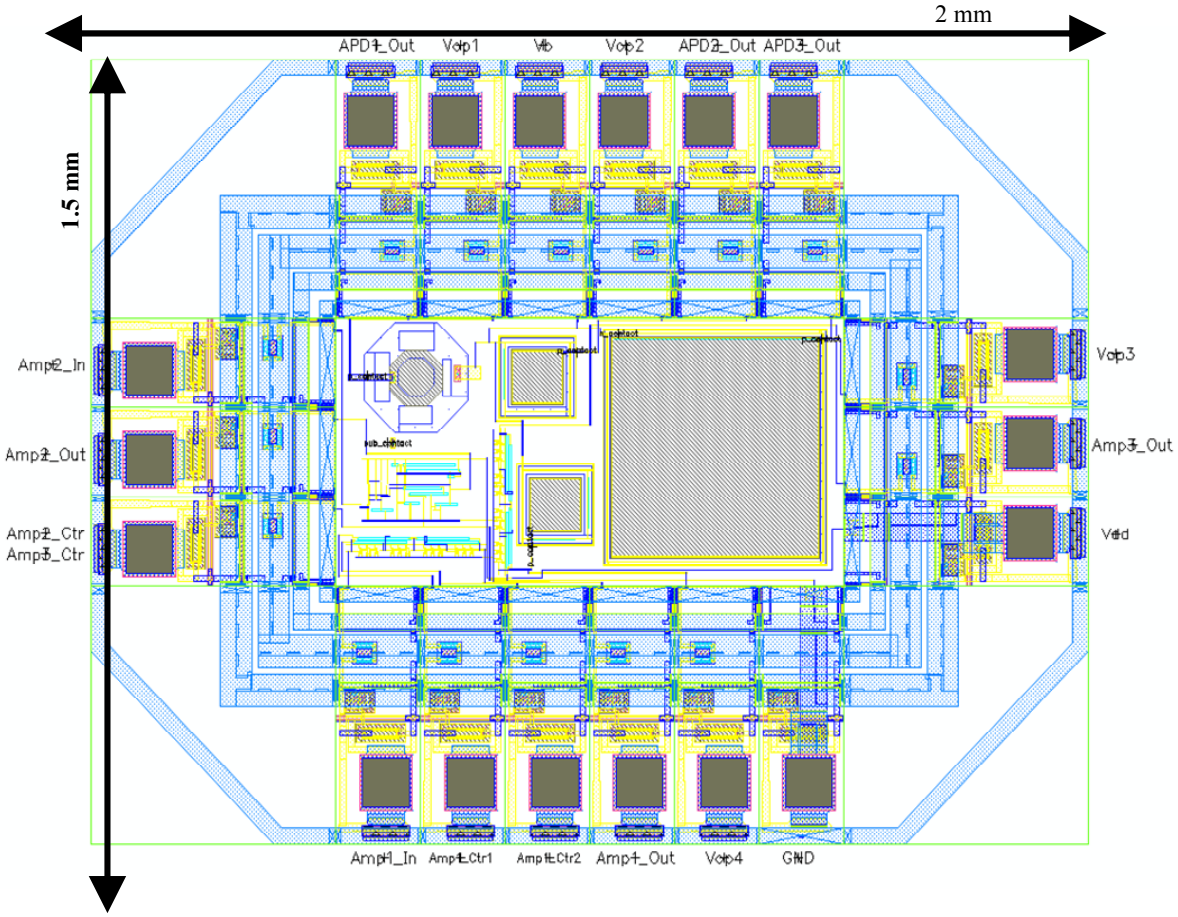
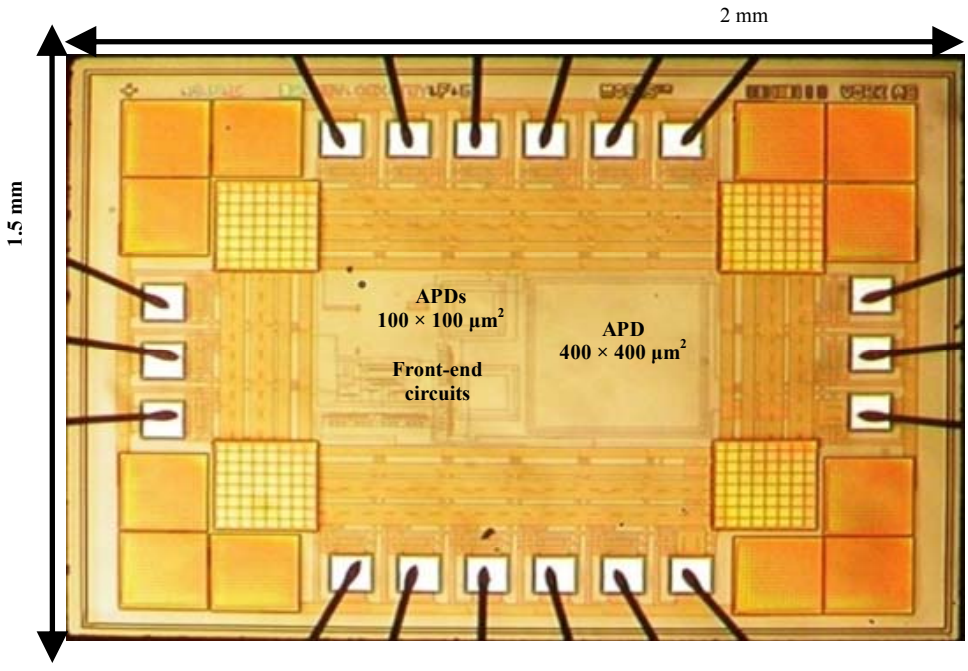


(a)



(b)

Figure 17. The layout (a) and microphotograph (b) of the fabricated IC.

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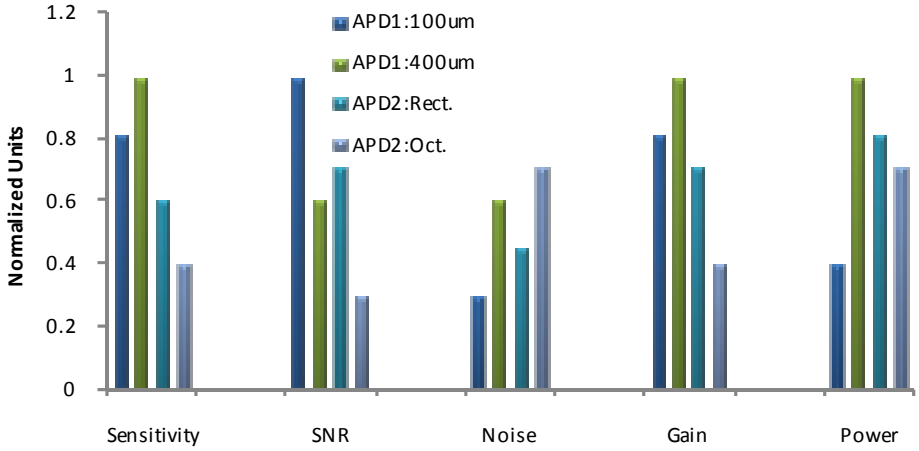

Figure 18. Validation the integration effect on APDs efficiency.

be integrated with the proposed TIAs.

7. Acknowledgements

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