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Design of Low Power CMOS LNA with Current-Reused and Notch Filter Topology for DS-UWB Application

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ABSTRACT

This paper presents the design of a low power LNA with second stage that uses a notch filter for DS-UWB application. The LNA employs a current reuse structure to reduce the power consumption and an active second order notch filter to produce band rejection in the 5 - 6 GHz frequency band. The input reflection coefficient S11 and output reflection S22 are both less than –10 dB. The maximum power gain S21 is 15 dB while the maximum rejection ratio is over –10 dB at 4.8 GHz. The minimum noise figure is 5 dB. The input referred third-order intercept point (IIP3) is –7 dBm at 6 GHz. The power consumption is 6.4 mW from a 1-V power supply.

Keywords: Low Noise Amplifier (LNA); Low Power; Low Voltage; Ultra-Wideband (UWB); Active Notch Filter

1. Introduction

Recently, the Federal Communications Commission (FCC) in the US approved the use of ultra-wideband (UWB) technology for commercial applications from 3.1 GHz to 10.6 GHz. The UWB transmission system has two major proposed applications, direct-sequence ultra-wideband (DS-UWB) and multi-band orthogonal frequency division multiplexing (MB-OFDM). The band definition of DS-CDMA is illustrated in **Figure 1(a)** which extends from 3.1 to 4.9 GHz and 6 to 9.7 GHz, and MB-OFDM is defined as the range from 3168 MHz to 10296 MHz which is shown in **Figure 1(b)**. The band range of 5 - 6 GHz is not considered in the current UWB system which is caused by the 802.11a wireless local area network (WLAN). UWB performs excellently for short-range high-speed uses, such as automotive collision-detection systems, through-wall imaging systems, and high-speed indoor networking, and plays a more and more important role in communication system applications. Low power consumption is one of the most important design concerns in the applications of this technology [1].

There are several existing topologies that have been proposed for wide-band amplifiers. The most important characteristics are that distributed amplifiers (DAs) provide good impedance matching, flat gain over a very wide range of bandwidth, and higher third-order inter modulation products (IIP3). However, the distributed amplifiers usually consume a lot of power, provide only medium gain, and occupy a large chip area [2].

Resistive shunt feedback amplifiers can provide good wideband impedance matching and improve good flatness at the expense of gain. However, a very wide bandwidth range with low noise and high gain is hard to achieve. Recently, LC-ladder matching, and band-pass Chebyshev or Butterworth filter networks have been proposed for a low-power UWB low noise amplifiers (LNA) in a 0.18 μm CMOS process [3]. It provides wideband input matching and a minimum noise figure of 4 dB under 9 mW power consumption. However, the noise figure (NF) rises rapidly at high frequencies, ranging from 5 - 8 dB in the band of 7 - 10 GHz. In addition, this topology needs a large number of high-Q inductors at the input node, so it is difficult to realize them in a small area. Therefore, it must have flat gain over the entire bandwidth, good linearity, minimum possible noise figures and low power consumption.

This paper focuses on the design and implementation of a common gate low noise amplifier (CGLNA) in a 0.18 μm CMOS process technology for DS-UWB applications. In order to minimize the undesired frequency, the active notch filter is adopted to provide a deep rejection ratio at 5.5 GHz. Recently, the research into circuits with multi-function operation capability is a hot topic. Our proposed circuit is multi-function circuit which it simultaneously performs a UWB signal amplifying and

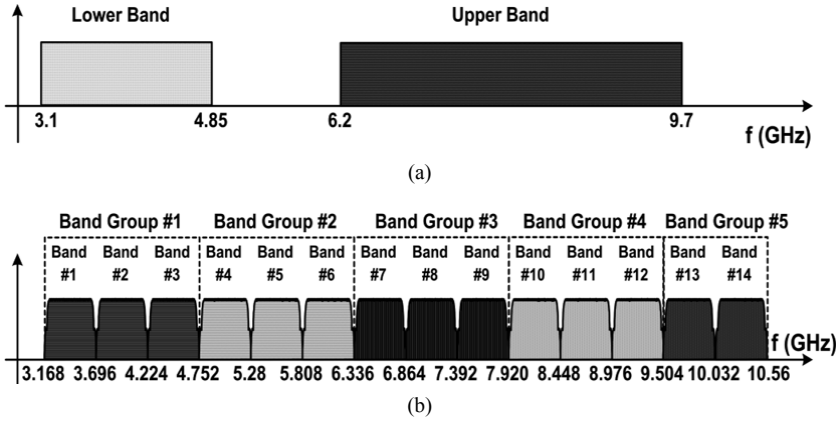

Figure 1. Spectrum allocated for UWB communication. (a) DS-CDMA; (b) MB-OFDM.

notch filtering function. In the first step, we design the UWB amplifying circuit. In the second step, the notch filter is added properly. The input impedance, noise, gain and notch filter of UWB LNAs are discussed in Section 2. Section 3 presents the final schematic of the proposed LNA. Finally, the measurements and simulation results of the UWB LNA are discussed in Section 4, which is followed by conclusions in Section 5.

2. LNA Design Technique

2.1. Input Impedance Matching of Common Gate Amplifier

In the design of LNAs for broadband wireless receivers, there are several issues that need to be investigated. These include low and stable 50 Ω input matching, flat gain with sufficient linearity, NF of the amplifier, and low power consumption, which is needed in portable systems. In this section, input impedance matching, noise analysis, and gain analysis for broadband LNA development is discussed.

Figure 2 shows the circuit with input stage of a common-gate amplifier. The inductor L_S is placed between the source of the MOS transistor and the ground terminal forming an LC resonator with the gate-to-source capacitance C_{gs} in a common-gate configuration [4]. The finite output resistance of the transistor also changes the input reflection of the LNA. In **Figure 2**, the load impedance of the common-gate stage and input impedance of the next stage will affect the matching and noise contribution due to the short-channel MOS transistor's relatively low output resistance which is about 500 Ω for a 0.18 μm CMOS process [6]. The small-signal equivalent circuit for the impedance calculation is shown in **Figure 3**. From **Figure 3**, the input impedance can be derived as

$$Z_{in}(s)=\frac{1}{sC_1}+\left[sL_S//\frac{1}{sC_{gs1}}//\frac{Z_{D1}}{1+g_{m1}r_{o1}}\right] \quad (1)$$

Note that g_{m1} is the small signal transconductance of the transistor M_1, and that Z_{D1} and Z_{D2} are given by Equations (2) and (3), respectively.

$$Z_{D1}(s)=\left[r_{o1}//\frac{1}{sC_{ds1}}\right]+\left[\frac{1}{sC_{gd1}}//Z_{D2}\right] \quad (2)$$

$$Z_{D2}(s)=\frac{1}{sC_g}+sL_g+\frac{1}{sC_{gs2}} \quad (3)$$

In the process of the derivation, Z_{D2} is indicated as the input impedance of the transistor M_2 amplifier with resistor R_1 feedback loop. And Z_{D1} is the total impedance

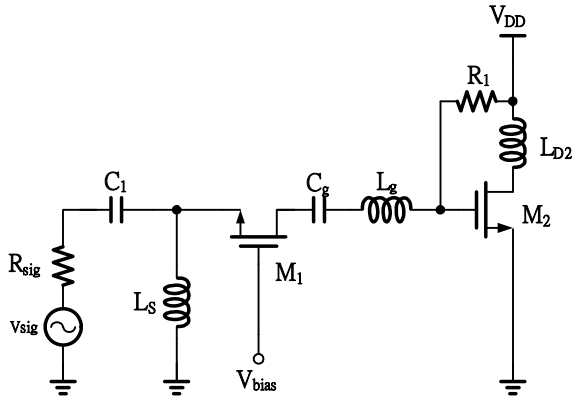

Figure 2. Configuration of a common-gate input stage.

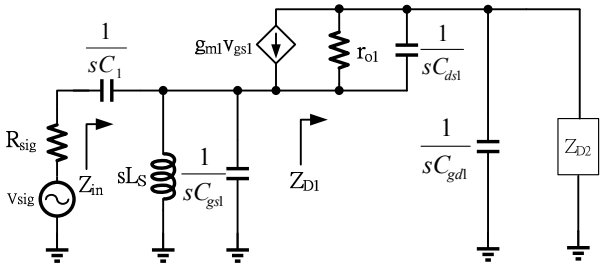

Figure 3. Small-signal equivalent circuit of a common-gate CMOS amplifier.

looking into the drain terminal of transistor M_1.

If we set $S = jw$, then Re(Z_{in}) is the real part resistance for 50Ω source signal matching, and Im(Z_{in}) is the imaginary part for resonance frequency tuning.

2.2. Noise Analysis

To analyze the noise characteristics of the CGLNA, the noise sources are added to the small-signal equivalent circuit as shown in **Figure 4**. $\overline{i_{nd}^2}$ represents the mean-square drain noise current which is given by [5-8]

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f \tag{4}$$

where k is the Boltzmann constant, T is the absolute temperature in Kelvin, g_{d0} is the zero-bias drain conductance, and Δf is the noise bandwidth in hertz over which the measurement is made. The parameter γ is a bias-dependent factor. For long-channel devices, γ has the value of unity at zero V_{DS} and 2/3 at saturation. For short-channel devices, the value of γ can be more than 2, depending on the bias conditions. The induced gate noise current $\overline{i_{ng}^2}$ is given by [5-8]

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f \tag{5}$$

where δ is the gate noise coefficient of which the typical value is 4/3 for long-channel devices. Note that g_g is given by

$$g_g = \frac{\omega^2 C_{gs1}^2}{5g_{d0}} \tag{6}$$

Due to the low gain of the common-gate stage, the noise contribution of the second stage cannot be neglected. The total noise factor of a two-stage amplifier can be expressed as follows [4]

$$\begin{aligned} F &= \frac{\text{Total}}{\text{Source}} \\ &= 1 + \frac{S_{n,g,u,1} + S_{n,g,d,c,1} + S_{n,g,u,2} + S_{n,g,d,c,2}}{S_{n,R_S}} \\ &= F_1 + \frac{S_{n,g,u,2}}{S_{n,R_S}} + \frac{S_{n,g,d,c,2}}{S_{n,R_S}} \end{aligned} \tag{17}$$

where F_1 is the noise factor of the single common-gate stage, excluding the effect of the noise contributed by the common source-stage which is given by the later two terms. F_1 is given by

$$\begin{aligned} F_1 = 1 &+ \frac{\gamma}{\alpha R_S g_{m1}}\left(1 + \frac{R_S^2}{\left|Z_S(\omega)\right|}\right) \\ &+ \frac{\alpha\delta\left(1 - |c|^2\right)\cdot\omega^2 C_{gs1}{}^2 R_s}{5g_{m1}} \\ &+ \frac{\alpha\delta|c|^2\,\omega^2 C_{gs1}{}^2 R_s}{5g_{m1}} + \frac{2|c|\sqrt{\frac{\alpha\delta}{5}}\omega C_{gs1} R_s}{jg_{m1}Z_S} \end{aligned} \tag{8}$$

where $\alpha = g_m / g_{d0}$ and |c| is a correlation coefficient with predicted value of 0.395 [9-11].

According to Equation (8), the drain noise is based on our circuit when considering Equation (4). The correlation between input and output noise is about 0.68 - 0.85, which is dependent on bias voltage. The total noise contribution is dominated by g_{m1} in the denominators; we can increase it to reduce the overall noise. However, the input matching degrades as g_{m1} increases. By properly choosing the device parameter to satisfy simultaneous gain and noise matching, we can sacrifice a little S_{11} to reduce the noise contribution.

2.3. Gain Analysis (Compensation)

In order to reduce supply voltage and power consumption while providing sufficient gain at multigigahertz frequencies, a complementary amplifier with a current-reused circuit topology is employed [11-14]. Because of the corresponding gain, performance is usually not high enough for UWB application due to the tradeoff between gain and bandwidth [15,16]. The presented LNA adopts two-stage cascade architecture to achieve enough power gain and bandwidth. The first stage is designed to resonate at the lower band, and the second stage is to resonate at the higher band. In order to achieve a flatness power gain, the inter-stage matching network is designed for gain compensation. The behavior of gain compensation is illustrated in **Figure 5**.

2.4. Notch Filter

Recently, some researchers have reported on LNA with notch filters [17-22]. **Figure 6(a)** shows an active second-order notch filter and a small signal equivalent circuit is shown in **Figure 6(b)**. From **Figure 6(b)**, the input impedance of the filter is given by [18]

$$\begin{aligned} Z_{\text{in,notch}} &= j\omega L_f + \frac{1}{j\omega}\left(\frac{1}{C_{gs1}} + \frac{1}{C_f}\right) \\ &- \frac{g_{m1}}{\omega^2 C_{gs1} C_f} + R_{Lf} + r_{g1} \end{aligned} \tag{9}$$

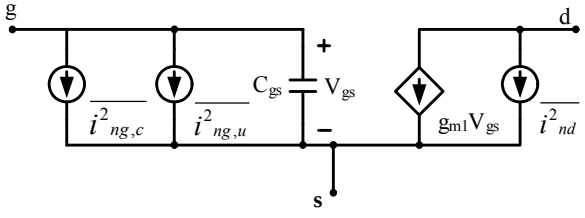

Figure 4. Noise model for the amplifying transistor.

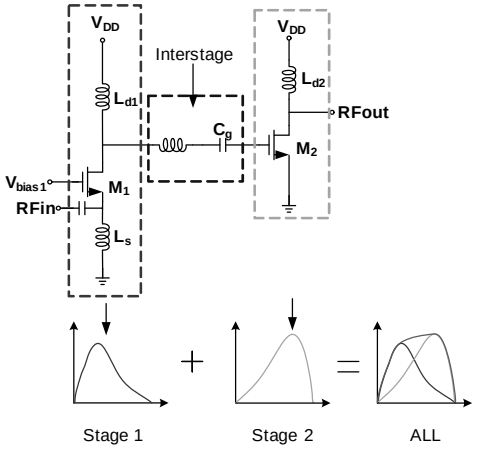

Figure 5. Two-stage amplifiers with the behavior of gain compensation.

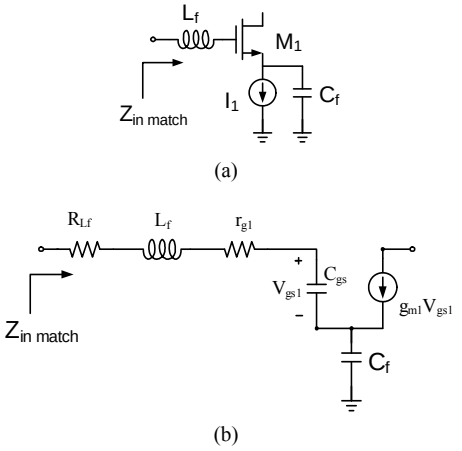

Figure 6. (a) Schematic of the second-order active notch filter; (b) The small signal equivalent circuit.

where r_{g1} is the series gate resistance of M_1, and R_{LF} is the series resistance of on-chip inductor L_f.

Note that the negative term on the Equation (9) represents the negative resistance seen at the gate of transistor M_1 which is proportional to g_{m1}. R_{L1} and r_{g1} can be cancelled by a suitable negative value hence leaving the imaginary impedance. Though the negative resistance comes from the notch filter, its purpose is to function as the deep rejection ratio. Therefore, the stability of the UWB amplifying circuit does not matter.

Therefore, the quality factor of the on-chip integrated inductor plays a minor role in the quality factor of the filter, which can be obtained as

$$Q = \frac{\left(\frac{L_f}{C_{gs1}} + C_f\right)^{\frac{1}{2}}}{R_{Lf} + r_{g1} - \frac{g_{m1}}{\omega^2 C_{gs1} C_f}} \tag{10}$$

where g_{m1} is large enough to cancel the denominator, and where the Q-factor of the notch filter becomes infinity. Thus, a very deep rejection ratio is obtained. The rejection frequency can be derived as

$$f_{\text{notch}} = \frac{1}{2\pi\sqrt{L_f\left(\frac{C_{gs1}C_f}{C_{gs1}+C_f}\right)}} \tag{11}$$

From the 802.11a WLAN system, the major interference sources are the in-band signal which occupies at the 5 - 6 GHz band, so the frequency of notch filter f_{notch} which is set to be 5.5 GHz. As can be seen from **Figure 7**, the image signal at 5.5 GHz is very low, while the impedance at the wanted signal has a peak value.

3. Final Proposed LNA Circuit

The fully integrated UWB LNA with current-reused and notch filter topology is implemented in the TSMC 0.18 μm CMOS process. The schematic of this circuit including the output buffer is shown in **Figure 8**. In this circuit, both M_1 and M_2 operate as common-source stages, but they share the same bias current. The signal amplified by M_1 is coupled to the gate of M_2 by C_1 while the source of M_2 is bypassed by C_2. The circuit thus saves power through the reuse of the bias current [14]. To elevate the bandwidth of the CMOS LNA close to 3.1 - 10.6 GHz, a two-stage configuration with band extension inductor Ls is adopted. The input common-gate stage not only provides wideband input matching, but also a narrow-band frequency at lower frequency. The spiral inductor Ls is chosen with a relatively high Q factor, and resonates with C_{gs} of M_1 around the center of the 3.1 to 10.6 GHz band. The second stage of the common source amplifier with inductive load L_{d2} provides high-frequency gain and determines higher frequency of the LNA. To achieve the goal of low power operation, the second stage is stacked on top of the first stage. The inter-stage matching network consists of L_g and C_g, which is to maintain gain

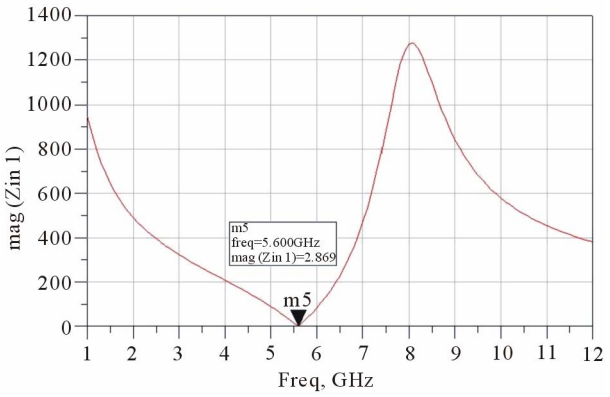

Figure 7. Filter characteristic of the proposed notch filter.

flatness. The M_6 transistor with bias in **Figure 8** is tuned as a current source I_1 in **Figure 6**.

The series inductor L_b further resonates with the input capacitance of M_3, resulting in a large bandwidth and some residual peaking on the frequency response. **Figure 9** shows the bandwidth improvement for practical L_b value.

The bypass capacitor C_2 provides an ac ground path for the second stage and avoids the coupling to the first stage. A source follower stage has been added as an output buffer for measurement purposes. The branch current in the proposed circuit with I_{D1}, I_{D2} and I_{D3} is 2.76 mA, 2.27 mA and 0.88 mA, respectively. I_{D1} indicates the current of the first stage with current-reused topology, I_{D2} indicates the current of the output stage, and I_{D3} indicates the current of the notch filter circuit. Devices sizes are summarized in **Table 1**.

4. Measurement Results

The chip microphotograph of the fully integrated UWB

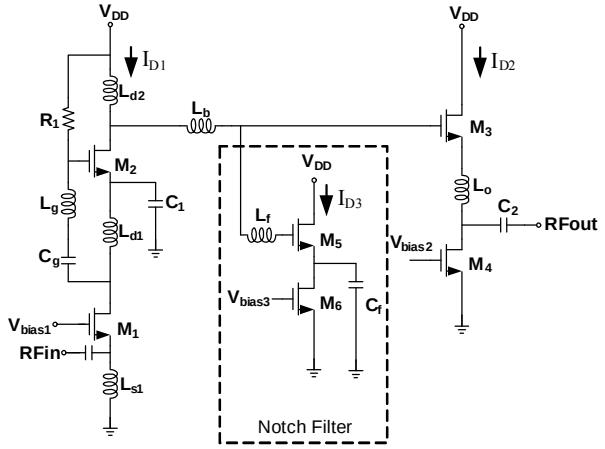

Figure 8. Proposed circuit for UWB system.

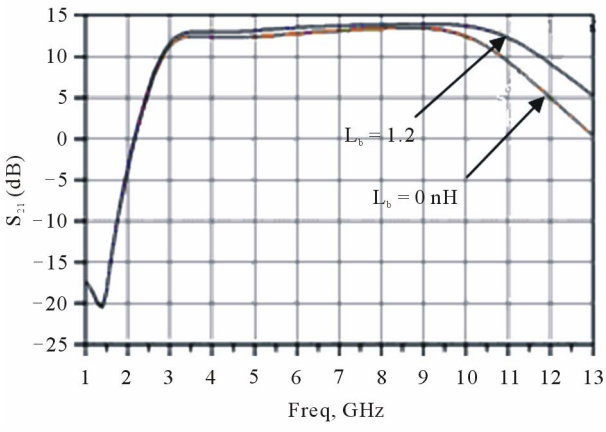

Figure 9. The bandwidth improvement of the gain performance.

Table 1. Device dimension.

Parameters	Device dimension
	Devices Size
M_1	0.18 × 85 (L × W) (μm)
M_2	0.18 × 80 (L × W) (μm)
M_3	0.18 × 60 (L × W) (μm)
M_4	0.18 × 55 (L × W) (μm)
M_5	0.18 × 72 (L × W) (μm)
M_6	0.18 × 55 (L × W) (μm)
L_{d1}	8.68 (nH)
L_{d2}	1.87 (nH)
L_g	2.02 (nH)
L_{s1}	2.31 (nH)
L_b	1.21 (nH)
L_f	6.84 (nH)
L_o	0.32 (nH)
C_g	900 (fF)
C_1	198 (fF)

LNA is shown in **Figure 10**. The area of the circuit including testing pads occupies approximately 1.26 mm^2. The total power consumption of the proposed LNA including the output buffer is only 6.4 mW under 1-V supply voltage. **Figures 11** and **12** show the measured and simulated input and output reflection coefficients.

The S_{11} and S_{22} are both below –10 dB over the entire 3 - 10 GHz band. The difference with the 1 GHz frequency shift between simulation and measurement is caused by the variation of parameters and pad coupling capacitance of the measuring process.

The measured and simulated power gain of the LNA is shown in **Figure 13**. In the 3 - 5 GHz band, the measured peak gain is 15 dB at 3.1 GHz while in the 6 - 12 GHz band the peak gain is 11 dB at 11.6 GHz. The high band has gained variation with about 3 - 4 dB between the simulation and measurement. The original frequency of the notch filter is designed at 5.5 GHz. The results come from the parasitic quality of the notch filter, especially caused by the input capacitive property of transistors M_5 and M_6. Owing to the variation of capacitance, the location of the frequency also shifted forward. Therefore, the center frequency of the notch band is tuned to 4.8 GHz with a minimum rejection gain of –9.7 dB. **Figure 14** shows the measured and simulated noise figures of the LNA.

The measured minimum noise figure is about 5 dB around 4 GHz. The difference of average noise figures between the measurement and simulation is about 2 dB below 8 GHz. This extra noise arose from the process

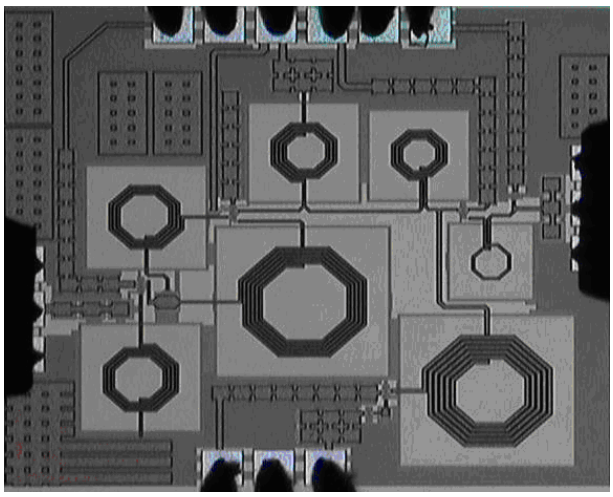

Figure 10. Microphotograph of the CMOS LNA chip.

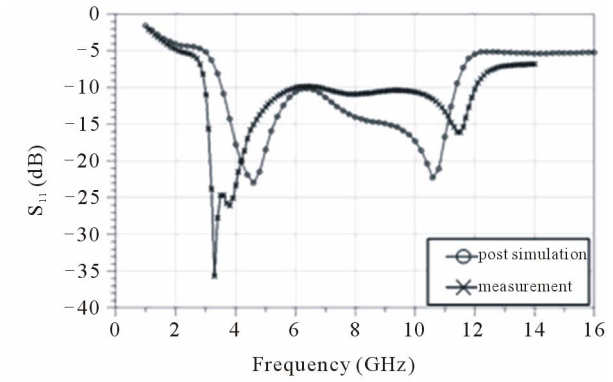

Figure 11. Measured and simulated input returns loss.

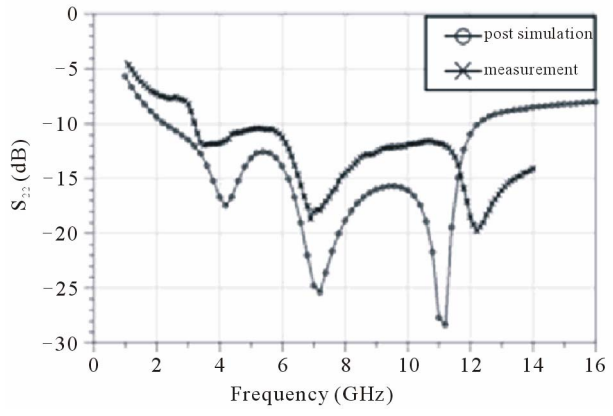

Figure 12. Measured and simulated output returns losses.

variation of the device and the structure of the common-gate LNA circuit. The high NF in the 5.5 GHz zone will slightly affect the signal transmission of system performance. A two-tone test with 10 MHz tone separation was performed to measure the third-order intermodulation distortion (IMD3). **Figure 15** shows that the measured input third-order intercept point (IIP3) at 6 GHz is

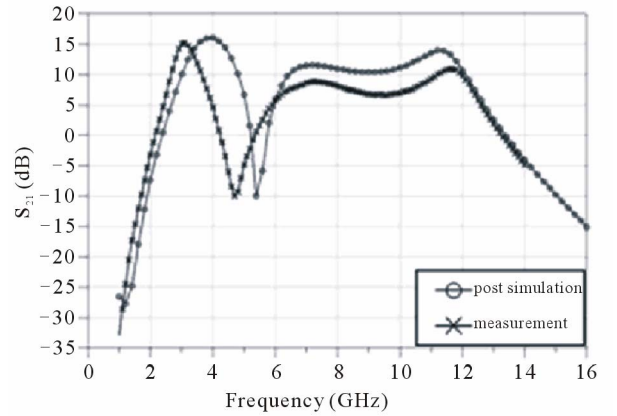

Figure 13. Measured and siumlated gain of the CMOS LNA.

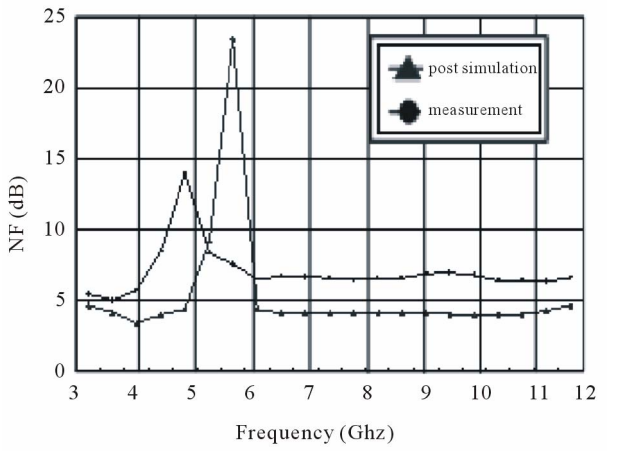

Figure 14. Measured and simulated noise figures.

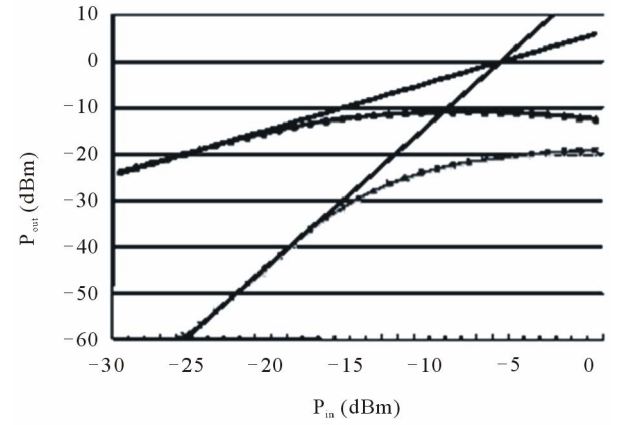

Figure 15. Measured input IIP3 at 6GHz.

–7 dBm.

A figure-of-merit (FOM) is proposed to characterize the overall performance of the UWB LNA and evaluate the effectiveness of the design methodology as follows [21]:

$$\text{FOM} = \frac{\text{Gain}_{\max} \cdot BW_{\text{GHz}} \cdot RR_{\text{dB}}}{NF_{\min} \cdot PD_{\text{mW}}} \quad (12)$$

where Gain is maximum power gain, BW is bandwidth, NF is the minimum noise figure and RR indicates the rejection ratio. Generally, gain variation is not considered in notch filter; yet in this design, $\text{Gain}_{\max}$, bandwidth, $\text{noise}_{\min}$, power consumption and rejection ratios are considered in the FOM.

A summary of the rest of the measurements is also included in **Table 2**. The performance comparison with other reported papers is shown in **Table 3**. The rejection gained more than 20 dB in **Table 3** which is nearly the lowest because of the larger variation of the ripple with gain flatness. Compared with these amplifiers, this work achieves the highest FOM and the lowest power consumption of 6.4 mW.

5. Conclusion

A low power LNA with notch filter intended for 4.8 GHz interference rejection in UWB systems has been presented in this paper. The proposed common-gate is employed to achieve wideband input matching with low noise and very low power consumption using a stagger tuning technique and current reused architecture. The power consumption is 6.4 mW with 1 V supply voltage. From 3.1 to 10.6 GHz, the power gain is higher than 15 dB and the minimum noise figure is 5 dB. The deepest rejection ratio that can be attained is –10 dB.

Table 2. Summary of the measurement result.

Summary of the measurement result		
performance	*Low band*	*High band*
S_{11} (dB)	<–10	<–10
S_{22} (dB)	<–10	<–10
S_{21}max (dB)	15	11
$NF_{\min}$ (dB)	5	6.3
IIP3 (dBm) [@6GHz]	–7	
Power (mW)/Supply (V)	6.4/1	

Table 3. Comparison with other reported LNA.

	Comparison with other reported LNA				
	[20]	[21]	[22]	[23]	This work
Technology <μm>	0.18	0.18	0.18	0.18	0.18
Frequency <GHz>	3.1 - 10.6	3.1 - 10.6	3.1 - 10.6	3.1 - 10.6	3.1 - 10.6
P_D <mW>	23.4	36	22.6	22.6	6.4
$NF_{\min}$ <dB>	6.4	4.1	5	2.5	5
S_{11} <dB>	<–10	<–10	<–10	<–8.6	<–10
$S_{21\max}$ <dB>	>5.6	12.1	11.5	15.5	15
S_{22} <dB>	N/A	N/A	<–10	<–10	<–10
Rejection gain (dB)	29	>40	49	15	>20
FOM	16	24.1	38.4	29.7	52

6. Acknowledgements

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