# PCB Via Analysis in Microwave Simulation Model

**Liu Erli, Zhao Lianqing**

*School of Electrical and Electronic Engineering ,North China Electric Power University,Beijing, China,102206*

*Liuerli22@126.com,zhaolianqing@163.com*

**Abstract:** PCB via effect on high-frequency signals can not be ignored in modern circuit design. Based on microwave theory, a dual-port network model of via is established in this paper and the mathematical model about the relationship between the frequency and $S_{21}$ is brought out. The validity of the theoretical approach is verified by comparing the simulation results of different vias using Ansoft HFSS. In the end some design guidelines are advanced in high-speed PCB design.

**Keywords:** via; high-speed PCB; signal transmission; dual-port network

## 1. Introduction

In the design of digital systems, the wiring density and clock frequency are continuously improving. Signal integrity, electromagnetic compatibility and other issues become more serious, so board-level hardware design becomes more difficult. In the multi-layer PCB, via is usually used for electrical connections between different layers. In the high-frequency circuits (above 1 GHz) design , the impact of via parasitic parameters on the signal integrity can't be ignored and its effect has become one of the key constraints that its improper handling may lead to failure of the whole design[1].

## 2. Via Structure

As an important component in multilayer design, via can be used for fixing device and electrical connections between different layers .A typical via consists of three parts: hole, pad area surrounding the hole and clearance hole in power plane[2].Fig.1 shows a typical via structure. As Fig.2 shows, via in general is divided into three categories: blind via, through-hole via and buried via. Blind via which is located at the top and bottom PCB surfaces has a certain depth, is often used for connecting the surface and the inner line and its hole depth and diameter don't normally exceed a certain ratio. Buried via which is used to connect PCB inner planes will not extend to the surface of the board. Through-hole via which crosses through the entire circuit board is used to achieve interconnection or internal components installed as a hole location. As through-hole via is much more easy to implement and cost less, it is widely used in PCB design.

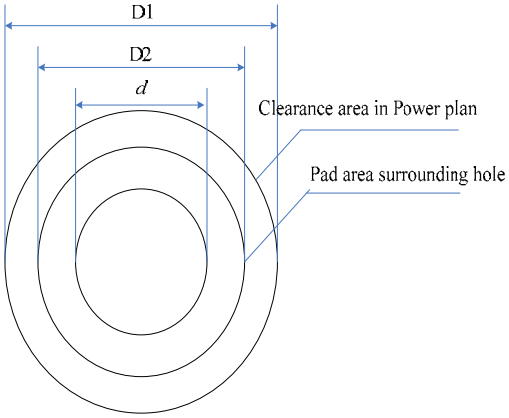


**Fig.1 A typical via structure**

## 3. $S_{21}$ Model of Via

For further analysis of via, the equivalent model is established. Each via contains parasitic capacitance and parasitic inductance which does more harm to high-frequency signal than the former.Fig.3 shows the equivalent model of via.

In the microwave point of view, a via can be equivalent to a dual-port network.Fig.4 shows a typical dual-port network[4], a port inputs signals and the other outputs signals. If Port1 is defined input port and Port2 defined output port, $S_{21}$ is on behalf of the Transmission

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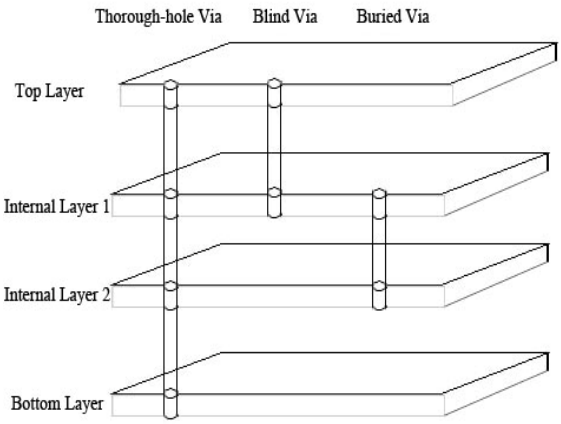


**Figure 2 Via Categories**

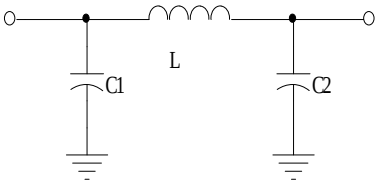


**Figure 3 Via equivalent model**

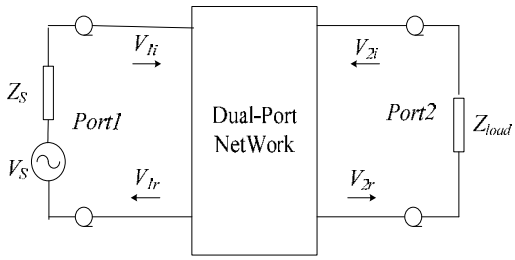


**Figure 4 A typical dual-port network**

The equation of $S_{21}$ is shown in Equ.1 and means the ratio of reflection voltage $V_{2r}$ in Port2 and incident voltage in $V_{1i}$ in Port1.For Port2 is passive, to meet the condition that $V_{2i}$ = 0,Port2 and $Z_{load}$ should be conjugate match.

$$S_{21} = \frac{V_{2r}}{V_{1i}}\bigg|_{V_{2i}=0} \tag{1}$$

As is shown in Fig.5, the dual-port network model of via can be derived from via model in Fig.1 and dual-port network in Fig.4.In the model, $S_{21}$ can be solved from port voltage($V_1$,$V_2$) and port current ($I_1$,$I_2$)[5].

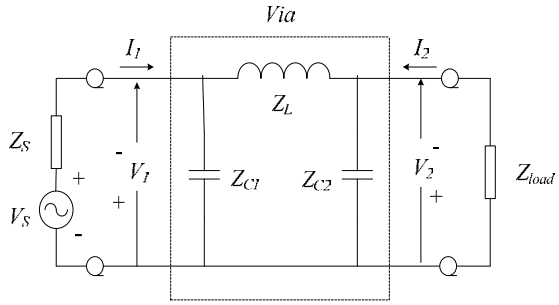


**Figure 5 Via dual-port network model**

In Fig.5: $Z_L = j\omega L, Z_{c1} = Z_{c2} = Z_C = \frac{1}{j\omega C}$, Output impedance of Port2 is $Z_{out2} = (Z_{C1} // Z_S + Z_L) // Z_{C2}$, Conjugate matched load of Port2 is $Z_{load} = Z^*_{out2}$ .

By Kirchhoff's voltage law, we can get the two ports' voltage and current:

$$I_1 = -\frac{V_s(H + N \cdot Z_{load})}{K \cdot Z_{load} + M} \tag{2}$$

$$V_1 = V_S + \frac{V_s Z_s (H + N \cdot Z_{load})}{K \cdot Z_{load} + M} \tag{3}$$

$$I_2 = -\frac{V_s}{K \cdot Z_{load} + M} \tag{4}$$

$$V_2 = -\frac{V_s \cdot Z_{load}}{K \cdot Z_{load} + M} \tag{5}$$

In the equations above:

$$N = \frac{2}{Z_C} + \frac{Z_L}{Z_C^2}$$

$$H = 1 + \frac{Z_L}{Z_C}$$

$$K = 1 + 2 \cdot \frac{Z_S}{Z_C} + \frac{Z_L Z_S}{Z_C^2} + \frac{Z_L}{Z_C}$$

$$M = Z_s + Z_L + \frac{Z_L Z_S}{Z_c}$$

$S_{21}$ can be represented by port voltage and current as is shown in Fig.5.The equation is shown in the following:

$$S_{21} = \frac{V_2 - I_2 Z_{out2}}{V_1 + I_1 Z_S} \sqrt{\frac{|\mathrm{Re}\, Z_S|}{|\mathrm{Re}\, Z_{load}|}} \tag{6}$$

From Equ.2 to Equ.6,the relation equation of $S_{21}$ and frequency $w$ is that:

$$S_{21}(\omega) = \frac{k_1\omega^{5/2} + k_2\omega^{3/2} + k_3 + j(k_4\omega^{7/2} + k_5\omega^{3/2})}{k_6\omega^{7/2} + k_7\omega^{5/2} + k_8\omega^{3/2} + k_9\omega^{1/2} + k_{10}} \tag{7}$$

In the above equation, $k_i$ is a expression that has nothing to do with $w$ and $k_6 > k_4$.

From Equation 6 and 7,we can know $|S_{21}|<1$.In the microwave point of view, via is a loss component. In the case of fixed parasitic parameters, the frequency of signals directly determine the value of $S_{21}$ that the higher the signal frequency is, the greater the via loss is, the smaller $S_{21}$ is. In this paper ,Ansoft is used for via simulation to validate the relation between the signal frequency and $S_{21}$.

## 4. Simulation of Via effect

Before the simulation, it's necessary to explain that via simulation in this paper is used for comparison between different models and the results can't represent the real via. In the models, the main physical (package) parameters are that substrate is FR-4 ($\varepsilon_r = 4.4$),both the thickness of copper plating and via plating are 1oz.In the following paper, we will establish three different models for through-hole via, buried via and blind via to verify the relation between the signal frequency and $S_{21}$ as is shown in Equation 6 and7.

As is shown in Figure 2, the via is divided into three categories: blind via, through-hole via and buried via. Different models have different effect on high frequency signals, that's to say the trends of $S_{21}$ are different. In this paper, the model of through-hole via has two layers(bottom layer, top layer),the simulation result of $S_{21}$ is shown in Figure 6;the model of blind via has four layers(top layer, bottom layer, internal layer1,internal layer2),the simulation result of $S_{21}$ is shown in Figure 7;the model of buried via has six layers(top layer, bottom layer, internal layer1,internal layer2,power layer, ground layer), the simulation result of $S_{21}$ is shown in Figure 8.

As is shown in Figure 6,in through-hole via model the value curve of $S_{21}$ (dB) decline gradually with the increase in the frequency that the loss of the signals that transmit from Port1 to Port2 is increasing gradually. The result is in line with the Equ.6 and7.As is shown in Fig.7,in blind via model ,the value curve of $S_{21}$ (dB) decreases steeply when the frequency is between 1～2GHz, has some fluctuations when the frequency is between 2～16GHz.But on the whole the result is in line with the Equations.6 and7.As is shown in Figure 8, the value curve of $S_{21}$ (dB) increases gradually when the frequency is between 1～2.7GHz and has some fluctuations when the frequency is between3～8GHz.On the whole the result is not in line with the Equ.6 and7.The result shows that the electromagnetic environment around the buried via which is located between the layers and is near the power layer and ground layer is so complex that a more effective model should be build to represent it.

## 5. Conclusion

In high-frequency, high-density PCBs, the loss of through-hole via and blind via would increase with the increasing frequency. As the complexity of he electromagnetic environment, the buried via which needs a more effective model has no regular change trend. In short, in order to avoid the parasitic parameters of via effect on high frequency signals, the designers should pay more attention to the following advices: ①Minimize unnecessary via; ② Minimize the length of via and Back-Drilling technology can be used to reduce parasitic parameters; ③ Choose a reasonable via diameter. The size on power and ground layers can be more large to reduce the impedance. In the consideration of cost the signal lines can reduce the via diameter.

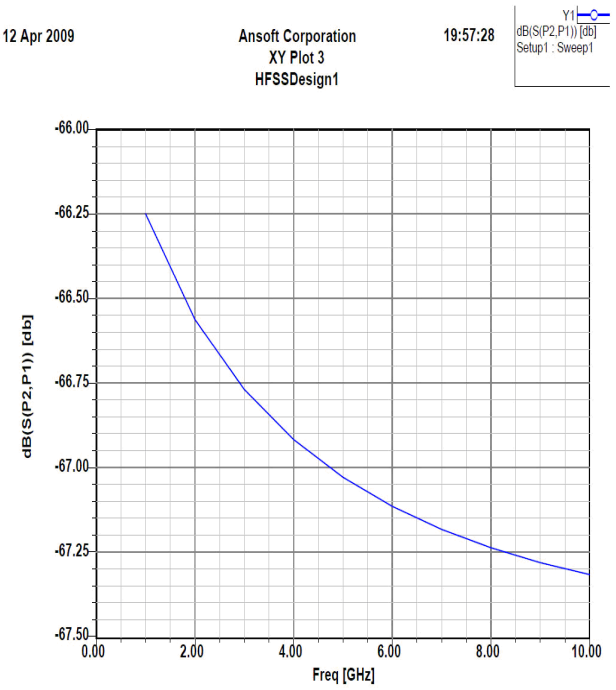


**Figure 6 $S_{21}$ simulation result of through-hole via**


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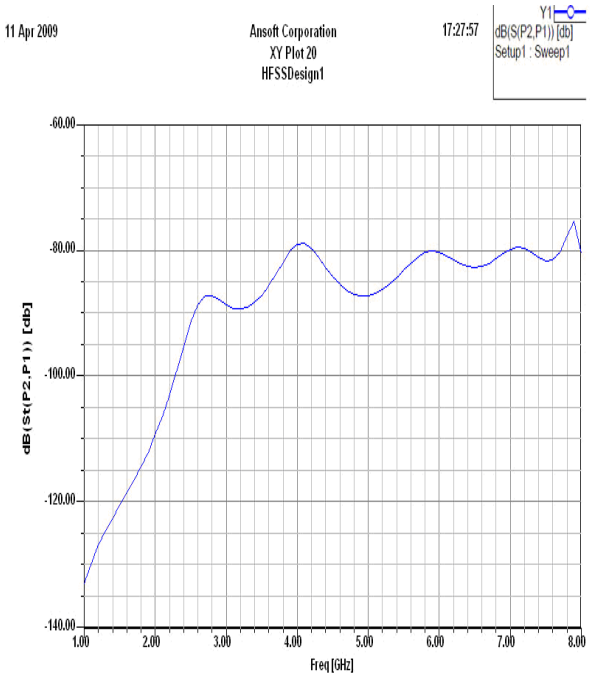


**Figure 7 $S_{21}$ simulation result of blind via**

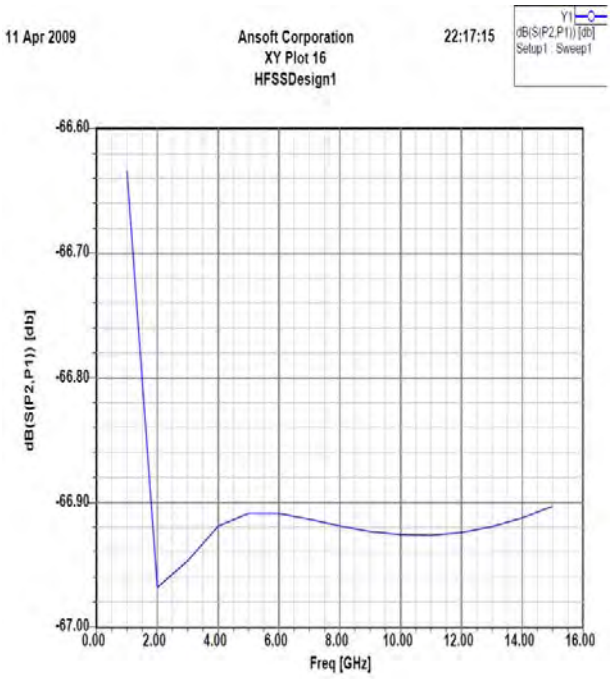


**Figure 8 $S_{21}$ simulation result of buried via**

## References

[1] Martin Graham. High-speed Digital Design, AHandbook of Black Magic[M]. University of California at Berkeley.1993.

[2] E. Laermans, J. De Geest, D. De Zutter, et al. “Modelingdifferentialvia holes”, IEEE ransactionson AdvancedPackaging, vol.24, no.3, 2001,P357-363.

[3] User's guide-high frequency structure simulator [Z].Ansoft Corporation,2005,P143-163.

[4] Constantine A. Balanis, Advanced Engineering Electromagnetics,John Wiley & Sons, New York, 1989,P791-793

[5] Robert J.Weber.Introduction to MicroWave Circuits Radio Frequency and Design Applications[M].Beijing: Publishing House of Electronics Industry,2005,P13-18