Int. J. Communications, Network and System Sciences, **2011, 4, 662-666**
doi:10.4236/ijcns.2011.410081 Published Online October 2011 (http://www.SciRP.org/journal/ijcns)

Using LDMOS Transistor in Class-F Power Amplifier for WCDMA Applications*

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Received August 8, 2011; *revised August* 27, 2011; *accepted September* 6, 2011

Abstract

The fundamental operating principle of a Class F power amplifier and the factors aiding or affecting Class F performance were explicated previously. A Class F power amplifier design which satisfies WCDMA specifications is explained in this paper. The Class F amplifier was designed by employing Motorola's LDMOS (Laterally Diffused Metal Oxide Semiconductor) transistor models and we simulated its performance by means of ADS. A variety of procedures were applied in the process of designing Class F amplifier, namely, DC simulation, bias point selection, source-pull and load-pull characterization, input and output matching circuit design and the design of suitable harmonic traps, which are explained here.

Keywords: ADS, Class F Power Amplifier, LD MOS, WCDMA

1. Introduction

The significance of wireless communications in the telecommunications industry of present stage is unquestionable. Almost every aspect of our daily life is somehow tied to wireless technologies. The technology of Universal Mobile Telecommunications System (UMTS) has already put 3G communication standard into practice for mobile communications.

Within wireless communication systems, power amplifiers are the most power-consuming units. The power amplifiers employed in UMTS devices should be extremely efficient. Enhanced efficiency, in addition to extending the battery life, reduces the DC power consumption, transmitter size and weight. Even though the power amplifiers applied in existing second generation GSM (Global System for Mobile Communications) transmitters are greatly efficient, they cannot be used in UMTS/WCDMA for GSM uses the constant envelope feature of GMSK (Gaussian Minimum Shift Keying) modulation which only establishes phase variations. A WCDMA system with QPSK modulation is employed in UMTS, where both phase and amplitude variations are established by the modulation. The power amplifiers which are designed for WCDMA should suit the contradicting operation requirement between linearity and efficiency [1,2].

*This work was supported in part by N.S.T.R.I, Tehran, Iran.

A very efficient class F power amplifier which has been designed for WCDMA band with a center frequency of 2.14 GHz and bandwidth of 5 MHz, applying LDMOS transistor, is introduced in this paper. The amplifier is simulated by means of a high frequency circuit simulator, titled as the Agilent Advanced Design System (ADS).

2. Design Architecture

Figure 1 illustrates the basic design architecture for Class F power amplifier. V_{DD} and V_{GG} present the mandatory drain and gate bias, which were determined before from a 26 V supply. DC bias and DC blocks are overlooked in this design. Input and output corresponding networks transform the impedance so the transistor, at their respective sides, should meet 50 ohms. Based on the fundamental frequency, filter combination L_0C_0 is tuned. It supplies very high impedance (preferably an open circuit) for the fundamental frequency, and very low impedance (preferably a short circuit) for harmonic frequencies. Together, L_3 and C_3 make the third harmonic trap. This trap makes high impedance available for the third harmonics and permits all other signals to pass through. Therefore, the third harmonic voltages are added out of phase to the fundamental voltage at the drain, resulting in the flattening of the drain voltage waveform. The series filter combination L_2C_2, together with bypass capacitor bypasses the second harmonics to

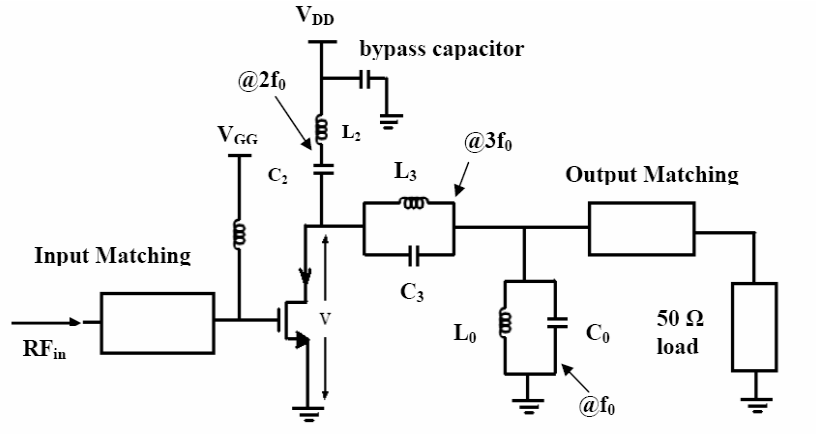

Figure 1. Class F power amplifier design architecture.

ground and, at other frequencies, provides high impedance. The consequence is a short circuit second harmonic current which, consecutively, makes the drain current waveform be similar to a peaked half sinusoid [3].

3. Class F Implementation

We have clarified various design blocks of the Class F amplifier. The final design was recognized in ADS. Motorola's High Voltage Version 10p04 LDMOS transistor model is employed in the PA. We have applied non-ideal inductors with a Q of 20 in order for the results gained to be close to the performance gained applying commercial inductors. Identical transistors, bias points and input and output corresponding networks are used for Class F amplifiers. **Figure 2** illustrates the ultimate realization of the Class F designs respectively. These designs are then simulated with the results to be analyzed.

3.1. DC Characteristics Analysis

The first step in designing any power amplifier is to choose the most appropriate bias point as shown in **Figure 3**.

If we alter the gate and drain bias voltages, the transistor's output characteristics demonstrate the different regions of operation (ohmic, saturation, and cut-off) and transistor's transfer characteristics demonstrate the pinch-off voltage for definite drain bias voltage [4]. The drain voltage was altered from 0 to 30 volts, as shown in **Figure 4**.

We carried a DC bias point simulation out, in order to determine the bias point. The plot of the DC transfer characteristics for the transistor at a drain-source voltage of 26 V is illustrates in **Figure 4**.

We may notice from **Figure 5** that the transistor has to be provided with a gate bias voltage between 3.2 V and 4 V for Class F operation. A 3.8 V gate bias voltage was selected for this design. The maximum value of drain current is 340 mA, as observed. A drain voltage of VDS = 26 V was selected.

3.2. Input and Output Matching

Us Matching input and output can be provided by means of a simple discrete element matching network, like an L-network, T-network or pi-network. A pi-network, C2-L1-L2, was employed to match to 50 ohms. We applied a high pass L-network, L4-C5 for output matching to 50 ohms. The capacitive element in the output L-network works as a DC blocking capacitor too (**Figure 6**).

3.3. S-Parameter Simulation

Simulated S-parameters Class F power amplifier is represented in **Figure 7**. S21 is above 20 dB at 2.14 GHz, and input and output impedance matching (S11, S22) is below –10 dB at 2.14 GHz, as shown in **Figure 7**. **Figure 8** represents Noise Figure and shows that NF is close to 2.6 dB from 1 to 3 GHz. NFmin is below 1.94 dB at 2.14 GHz.

3.4. Harmonic Terminations

The second and the third order harmonics tuning should be integrated in the output network, in Class F amplifier, in order to enlarge output power and efficiency.

Designing appropriate harmonic traps is the most critical, also the hardest part of the design. The third harmonic trap is designed by applying a parallel L-C filter tuned at the third harmonic frequency of 6.42 GHz. Several L-C combinations which would resonate at this frequency were designed. The combination which resulted in the best performance applying an inductor as small as possible was selected. A series L-C filter tuned at the second

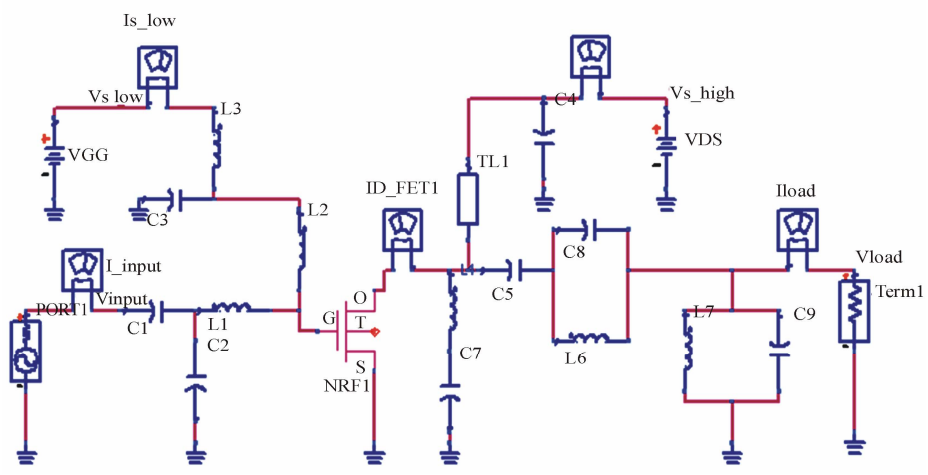

Figure 2. Schematic of the Class F power amplifier design.

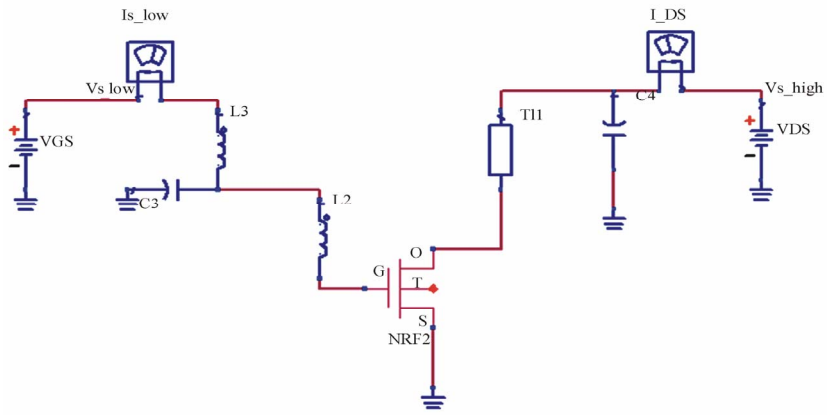

Figure 3. Schematic of DC bias for Class F power amplifier.

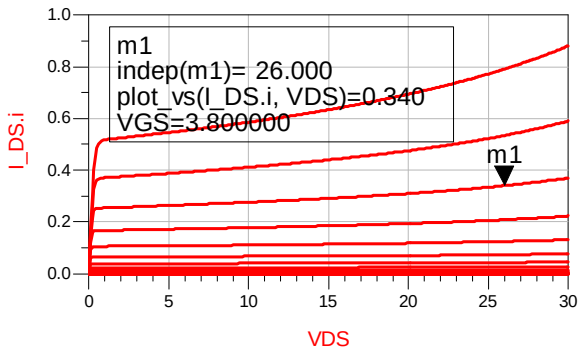

Figure 4. IDS vs VDS.

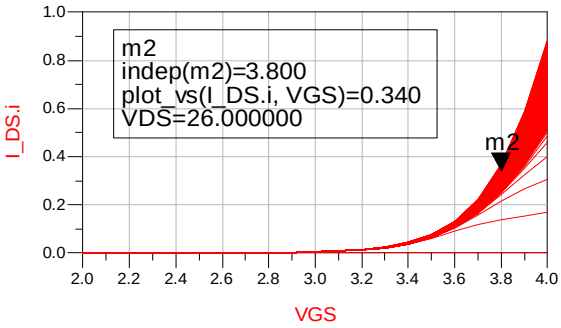

Figure 5. IDS vs VGS.

harmonic frequency of 4.28 GHz was primarily designed for the second harmonic trap. Yet, we noticed there was considerable fourth harmonic current in the circuit, which resulted in the loss of power. A transmission line of the length of one quarter-wavelength at fundamental frequency was tied to the drain of the transistor, and the other end of it bypassed to ground, in order to solve this problem. This was capable provided presenting a very good short circuit, not only at the second harmonic frequency, but also at the fourth, and even higher order frequencies. A similar method was tried, using a quarter-wavelength transmission line to provide an open circuit for odd harmonic frequencies, but it was detected that

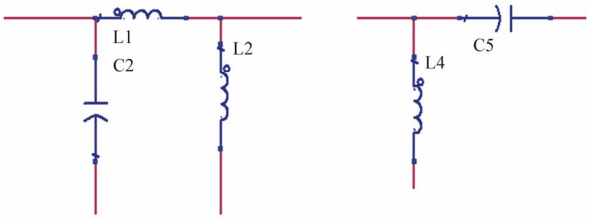

Figure 6. Input and output matching network.

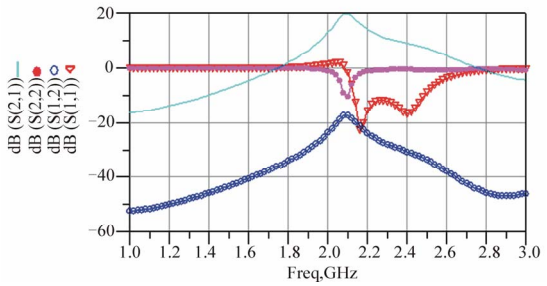

Figure 7. S-parameter of Class F power amplifier.

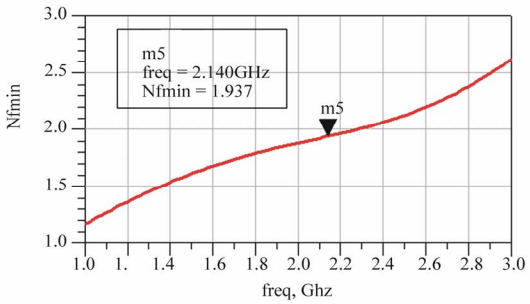

Figure 8. Noise figure of Class F power amplifier.

the transmission line was not able to generate a good open circuit. A potential work to be done in this field may be realizing the harmonic traps on-chip with the output matching done off-chip. A line of a quarter-wavelength at 2.14 GHz might be too long to fit inside a chip. Therefore, the third harmonic trap was recognized by applying discrete components. We can add harmonic traps for the fifth and other higher odd harmonics in order to enhance the performance at the expense of increased circuit complexity. The trade-off between the number of odd harmonic traps and circuit complexity is analyzed in [5], and it is figured out that, often, the third harmonic trap is sufficient for acceptable Class F performance. Additional harmonic traps, in addition to increasing the circuit complexity, might lead to loss when realized employing practical components. Moreover, it might be impossible to realize the design by means of practical components, at high operational frequencies. Bearing in mind the restrictions mentioned, it seems that the selected design scheme for the harmonic traps is the best solution.

Figure 9 shows the PAE plots of the Class F amplifiers respectively. There are Maximum PAE at 21 RFpower for which PAE = 75.85.

The gain plots for Class F amplifier are represented in **Figure 10**.

Figure 11 illustrates a plot of the power supplied to the load, in dBm, at each frequency of the Class F power amplifier.

Table 1 summarizes the performance of Class F power amplifier. **Table 2** is comparsion of performances of various Class F Pas.

4. Conclusions

A Class-F amplifier is designed and stimulated for this paper. The amplifier was simulated by employing a high frequency circuit simulator titled as the Agilent Advanced Design System (ADS). The feasibility of using a

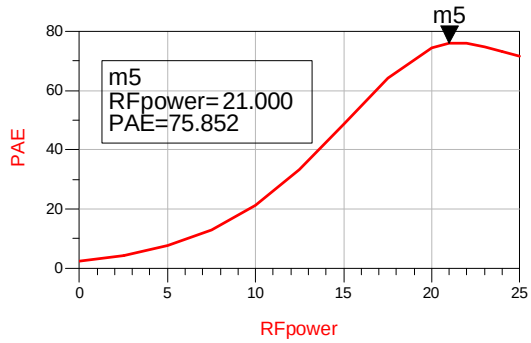

Figure 9. PAE (%) vs RF power (dBm).

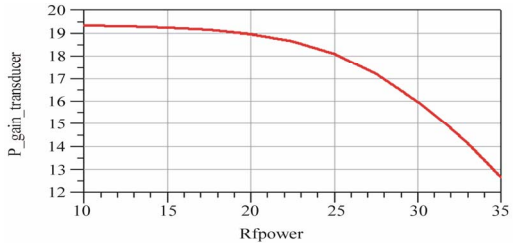

Figure 10. Transducer power gain (dB) vs RFpower (dBm).

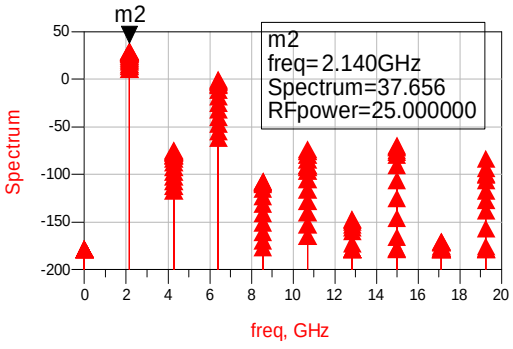

Figure 11. Output spectrum.

Table 1. Summary of the performance of the Class F.

Performance Parameter	Performance
Output Power P_{out} (dBm)	37.6
Gain (dB)	18
Power Added Efficiency @ Maximum Output Power (%)	75.8
DC Power P_{dc} (watts)	7.3
Thermal Dissipation (watts)	3.3
Input Power Pin (dBm)	24.8

Table 2. Comparsion of performances of various Class F Pas.

Reference	f_c (GHz)	PAE (%)	P_{out} (dBm)	Device
[6]	2	70.5	19.85	GaAs pHEMT
[7]	2	76	21	GaAs pHEMT
[8]	1.9	63	30	GaAs FET
[9]	2.4	59	22.2	GaAs MESFET
[10]	2.14	70	40.2	GaN HEMT
This Work	2.14	75.8	37.6	LDMOS

Class F amplifier for WCDMA applications is proved via simulation, by achieving an efficiency of 75.8% with good linearity. This research provided the opportunity of making some important contributions in this field of investigate. The idea of employing Class F amplifiers for improving efficiency without corrupting linearity is rather new, and there has been no significant published work which focuses on Class F amplifiers for WCDMA applications up to today. The actual performance of the designed amplifier might differ considerably.

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