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A Novel Integrated Circuit Driver for LED Lighting

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Abstract

A novel integrated circuit for driving LED lighting has been proposed, designed and fabricated. Besides the typical parts of LED driver, an integral part was added at the output terminal of error amplifier in the driver. In this way, a novel average current mode can be set up to take the place ordinary peak current control mode. In addition, a BUCK low-level topology was adopted, too. It can be used to drive up to eight 1 W HB LED lights with 350 mA constant current. In this way, the LED driver displays high performance, in which output current with less 1% error and total efficiency as high as 96%. The feasibility of the design has been verified by actual measurement on the fabricated chip.

Keywords

LED Lighting Driver, Integral Circuit, Low-Level Topology

1. Introduction

Contrasting to the traditional fluorescent lamp, high bright LED, being a potential lighting source, has the obvious advantage in energy saving, environmental protection, high efficiency, etc. [1]. So it has attracted much attention in academy and industry to push forward its utility. Based on the requirements of HB LED, some detailed limitations should be considered during the design of LED driver. For example, the life of LED will be dramatically decreased on the condition that there exists the driving current deviation [1]. So an ideal LED driver should have the constant output current with the high accuracy [1].

Currently, a peak current control mode has always been adopted in the existing LED driver to obtain constant current [2]. Based on statistical data [2], 30% error could be caused by this peak current control mode, which subsequently deteriorates LED life time dramatically, up to 20%.

The main reason for influencing the accuracy of output current at peak current control mode lies in the fact

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that the peak current is varied with the inductor in the driver circuit [3]. Here, an average current control mode was adopted, in this case it isn't influenced by the inductor value anymore. In this way, a higher accurate output will be obtained in LED driver to guarantee its lifetime.

Besides the above mentioned accuracy problem, power efficiency is also a key parameter to evaluate the driver's quality. The topology of driver circuit will determine the efficiency [3]. In this paper, an optimized topology will be used to reduce power consumption.

To solve the above issues, an integrated circuit driver with average current control mode was proposed and designed in this paper, to get accurate and stable output current, which will be introduced in the Section 2. A BUCK low-level topology will be adopted in the driver to get high efficiency. This will be introduced in Section 3. Section 4 shows the simulation results using CSMC 0.5 μm 40 V BCD model. Finally, the experimental results and discussion will be made to show design's advantage.

2. Chip Design with Average Current Control Mode

Traditionally, in order to reduce the cost and complexity of the chip, a peak current mode control mode is always used in LED driver chip [4] [5]. However, the limitation of this method is the output current is easily influenced by inductor L and input voltage. This current variation will lead to degeneration of accuracy. At the same time, the actual current provided for the HB LED is less than the peak current. For this mode, theoretically speaking, the value of inductor should be infinity to obtain an output current which is equal to the design value.

Figure 1 schematically shows the current in the peak current control mode in the common BUCK topology. It can be seen from this figure that different inductor corresponding to same peak current, but different average currents. The greater the inductance L is, the closer the average approaches to peak current. Because of practical limitations, the inductance value L can not large enough. So the actual current value flowing through the LED is always less than the peak current. Based on the above analysis, there are two shortcomings for the peak current control mode. The one is that its average current is always varied by the inductor and input voltage. It can't maintain stable all the time. The other shortcoming lies in the fact that the average current is different from the designed peak current. These two facts have an obvious influence on the output's accuracy.

Figure 2 shows the schematic of the average current control mode. It can be seen that the average current always maintain the same regardless of inductor L values. Comparing the two control modes shown in **Figure 1** and **Figure 2**, one conclusion can be made that the average current control mode can be an effective method to guarantee the accuracy of output current. So, in this work, the average current control mode will be fulfilled in the circuit design. An integrated circuit with this mode has been designed, which schematic is shown in **Figure 3**. The part within dashed line corresponds to the designed integrated circuit, which includes error amplifier (EA), pulse-width modulator (PWM), slope generator, RS flip-flop, output stage with power transistor, etc. Its structure is a typical PWM controller except there is an integral part at the output terminal of EA.

The integral part is composed by three components, c_1, c_2 and R_2. For the two input terminal of EA, positive one is connected to a voltage reference while negative one $V_{\text{sense}}(t)$, termed as the detection voltage, connected to outside sense resistor, as shown in **Figure 3**. When the power transistor is on-state, there will be a current flowing through the sense transistor, so the detection voltage will appear and moreover, it will be increased for the existence of an external inductor L, which is not displayed in this figure.

At beginning, detection voltage is smaller than reference, EA will have a positive output. Because the integral parts exist, capacitors c_1, c_2 will be charged so that the voltage at output terminal increases.

When the value of detection voltage is larger than the reference, output of EA should be negative. However, the integral part will try to maintain the original EA output voltage. So, there is a discharge phase during this period. There are two main work states: In the first state, when power transistor is on-state, the detection voltage will appear, increasing during the on-state, as shown in **Figure 4(a)**. The output of EA, $V_{\text{EA}}(t)$, as shown in **Figure 4(b)**, rises at the beginning. When the detection voltage equals to the reference, $V_{\text{EA}}(t)$ reaches to the maximum value. Afterwards, with detection voltage increasing, output of EA will be decreased.

In the second state, when N-MOSFET power transistor turns off, $V_{\text{EA}}(t)$ remains unchanged for the existence of integral circuit, as shown in **Figure 4(b)**. **Figure 4(c)** shows the waveform of slope, which is connected to PWM's negative input terminal, denoted as $V_{\text{slope}}(t)$. $V_{\text{EA}}(t)$ is connected to positive ones. The average value of detection voltage during on-state has been set to be equal to the reference voltage. **Figure 4(d)** shows the output of PWM modulator. So the system is operated in a fixed period of conduction control mode. As is shown in the dotted line area in **Figure 3**, it is the core circuit for the average current regulation mode.

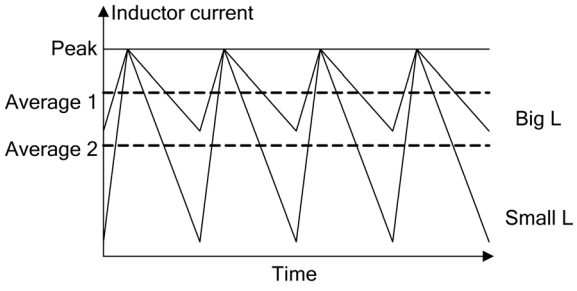

Figure 1. Schematic of peak current control mode.

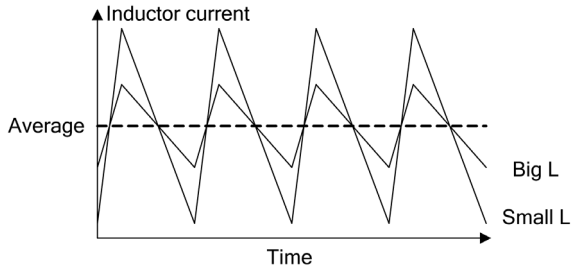

Figure 2. Schematic of average current control mode.

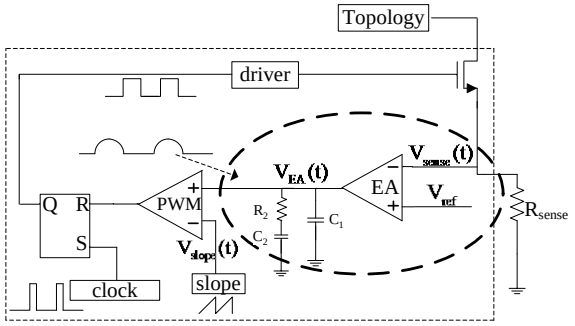

Figure 3. Schematic diagram of driving circuit.

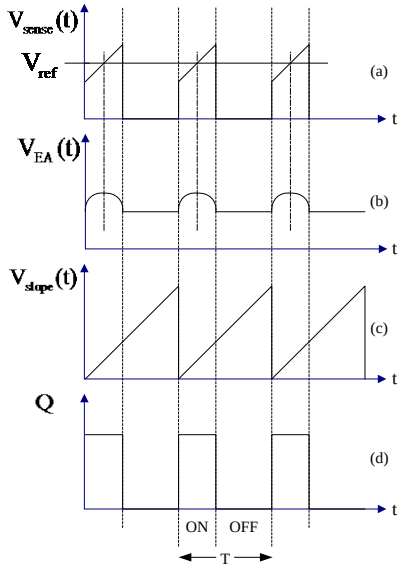

Figure 4. Timing diagram of driving circuit.

The traditional current regulator was designed as peak current control mode. It can't provide the actual average current regulation for the LED lamps. The traditional circuit uses an error amplifier to compare the difference between the transient value of detection voltage $V_{\text{sense}}(t)$ and the reference voltage. For the circuit shown in **Figure 3**, which is the average current mode and carries out the time integration about the error, the capacitors take the integration of the difference between the detection voltage $V_{\text{sense}}(t)$ and the reference voltage V_{ref}. Because the reference voltage V_{ref} is a constant value, that is to say, during the integration time $T*D$ (D is the switching duty cycle, T is the period time), it enables the difference between the average of $V_{\text{sense}}(t)$ and the reference voltage drop to a minimum value, so:

$$\int_0^{TD}\left[V_{\text{ref}}-V_{\text{sense}}(t)\right]\mathrm{d}t = V_{\text{ref}}*TD-\int_0^{TD}V_{\text{sense}}(t)\,\mathrm{d}t \tag{1}$$

Supposing Δv as the capacitance variation during Δt period, that is the increment of $V_{\text{EA}}(t)$. The equivalent output capacitance of EA is c, and the transconductance of EA is g_m. Following equation can be obtained:

$$\begin{aligned}\Delta V_{EA}(t) = \Delta v &= \frac{i\Delta t}{c}\\ &= \frac{\Delta t}{c}g_m\left[V_{\text{ref}}-V_{\text{sense}}(t)\right]\\ &= \frac{g_m}{c}\left[V_{\text{ref}}-V_{\text{sense}}(t)\right]\Delta t\end{aligned} \tag{2}$$

Based on Equation (2), when V_{ref} equals to $V_{\text{sense}}(t)$, the voltage on the capacitor reaches maximum value. When V_{ref} is less than $V_{\text{sense}}(t)$, the capacitor discharges, and then when V_{ref} is larger than $V_{\text{sense}}(t)$, the capacitor charges. So, during the TD period, $V_{\text{EA}}(t)$ increases at first. Then, it will decrease until the capacitor voltage equals to its initial value. When the state changes, the value of $V_{\text{EA}}(t)$ will remain the same during $T*(1-D)$ period. In this way, it repeats every cycle to form a stable average current.

It can also be noted that the output of EA is composed of a resistor R_2 and two capacitors c_1 and c_2, which forms two poles and one zero, and its frequency domain characteristics can be expressed as:

$$H(jw) = \frac{1+j\omega c_2\times R_2}{j\omega(c_1+c_2)+(j\omega)^2 c_1\times c_2\times R_2} \tag{3}$$

It can be seen that the corresponding zero point is $\frac{1}{c_2\times R_2}$ and the poles are 0 and $-\frac{c_1+c_2}{c_1\times c_2\times R_2}$. The zero can be inserted to eliminate the poor phase margin, which caused by the second pole, to increase the stability of the circuit.

3. Improved Topology

The common non-isolated BUCK topology is shown in **Figure 5**. V_{IN}, as the input voltage, is applied on drain terminal of power transistor. Based on the detection voltage of feedback resistor R, the power transistor is used to adjust conduction time.

In addition, the power transistor in **Figure 5** is located at high-level, and it adopts gate drive technology of the bootstrap circuit, ignoring the loss of power transistor. When V_{IN} is relatively high, gate voltage should be at least V_{IN} + V_{TH}. The transistor has high risk of breakdown. Compared with the topology shown in **Figure 5**, an improvement has been made in **Figure 6**, in which the power transistor is placed at low level. In this way, the low level N-MOSFET is much safer than high level ones.

As shown in **Figure 5**, in the traditional Buck topology, considering some key problem as the heat dissipation, maintenance or the module replacement, most components in controller are separated from HB LED. The current sense resistor R will be placed near the ground, and it only needs single-end detection circuit instead of complex differential detection circuit. So it can prevent electromagnetic interference.

In the system shown in **Figure 6**, the sensor resistor R is placed between source terminal and ground. Its power efficiency is increased compared to the circuit shown in **Figure 5** [6]. In addition, in **Figure 6**, the low-level N-MOSFET and sense resistor R can transmit inductive current only during part of the cycle, but the power loss of R in **Figure 5** occurs during the entire cycle, so the power loss of R in **Figure 6** equals to that of R in

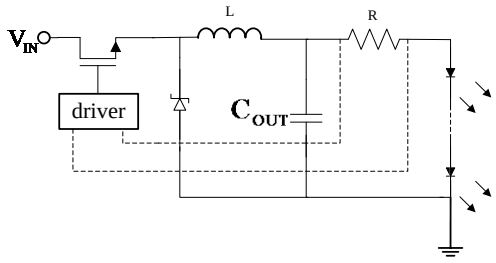

Figure 5. Traditional BUCK topology.

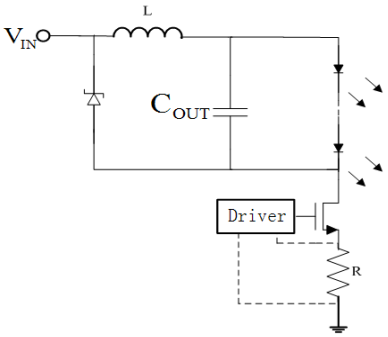

Figure 6. Optimized structure of LED driver.

Figure 5 multiplied by the switch duty cycle D, and the value of D is usually lower than one. Therefore, in **Figure 6**, the power loss of R will be reduced during a switching period $(1-D)T$, which can be shown as:

$$P = \frac{1}{T}\int_0^{DT} i_{\text{LED}}^2(t)R\mathrm{d}t \tag{4}$$

In **Figure 5**, the power loss of R can be expressed as:

$$P' = \frac{1}{T}\int_0^{T} i_{\text{LED}}^2(t)R\mathrm{d}t \tag{5}$$

The saved power can be expressed as:

$$\Delta P = \frac{1}{T}\int_0^{(1-D)T} i_{\text{LED}}^2(t)R\mathrm{d}t \tag{6}$$

According to the characteristic of the inductor, the above formula can be further shown as:

$$\begin{aligned}\Delta P &= \frac{1}{T}\int_0^{(1-D)T}\left(I_{\text{peak}} - \frac{V_L}{L}t\right)^2 R\mathrm{d}t \\ &= R(1-D)\left[I_{\text{peak}}^2 - \frac{V_L I_{\text{peak}}}{L}T(1-D) + \frac{1}{3}\frac{V_L^2}{L}T^2(1-D)^2\right]\end{aligned} \tag{7}$$

where T is the switching cycle, R is the sense resistor, and I_{peak} indicates the peak current of the inductor L, and V_L is the voltage across the inductor L. When the transistor is off-state, during $(1-D)T$, V_L equals the voltage drop across the LED lights. It can be seen from the above equation that placing the sense resistor on the low side will reduce the power loss.

The schematic shown in **Figure 7** is a complete LED driver circuit structure. It uses the average current control mode as shown in **Figure 3**, which increases the accuracy of the output current. At the same time, the optimized topology as shown in **Figure 6** will reduce the overall power loss.

4. Simulation Result and Layout Design

This design is implemented in CSMC 0.5 μm 40 V BCD technology. **Figure 8** is the simulation result of gain

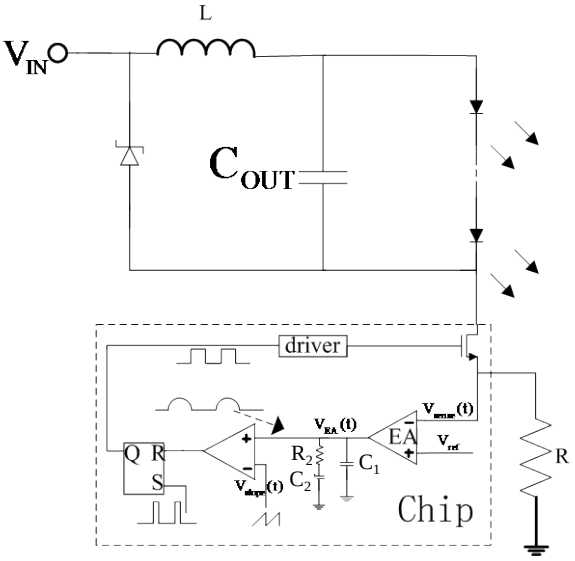

Figure 7. Complete LED driver circuit structure, the part shown within dashed line denotes the designed integrated circuit.

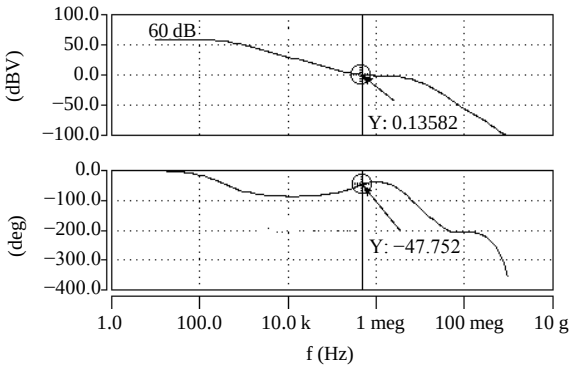

Figure 8. Bode plot of the core circuit.

and phase margin of error amplifier. By the reasonable settings of c_1, c_2, R_2 in **Figure 3** to adjust the location of zero, the stability of the circuit is enhanced. From the diagram it can be seen that the gain of the error amplifier is 60 dB, and the phase margin, which ranges from 180 to 47.75 degrees, is about 132 degree.

Figure 9 shows the driving current curve through the LED lamp. Based on the BUCK topology in **Figure 6**, a suitable inductor L should make the ripple current amplitude as small as possible. The greater inductor will produce more accurate output current. However, in order to minimize the physical size of the circuit, the value of inductor should be selected to enable the circuit working in continuous conduction mode. At the same time, it should be guaranteed that the peak current of the inductor does not exceed its saturation current. Calculation result shows that the value of L is over 22 μH. As shown in **Figure 9**, in which L equals to be 22 μH, C_{out} equals 10 μF, V_{in} equals 32 V, and eight 1 W of HB LED lights acting as load. It can be seen from **Figure 9** that the ripple of transient output current is 4.8 mA and the error is about 0.68%, indicating that the output current is stable and has high accuracy.

Figure 10 corresponds to the situation as same as that in **Figure 9** except that L equals 44 μH. The ripple of the transient output current is 1.6 mA, the error is about 0.23% with unchanged average current.

Based on the values shown in **Figure 9** and **Figure 10**, although the difference of the inductance value is twice, its average current remains constant, and the ripples are small. For the traditional peak current mode, its average current and ripple depend heavily on the value of inductor L. So, the average current mode has good stability to the output current, not changing with the value of the inductor L.

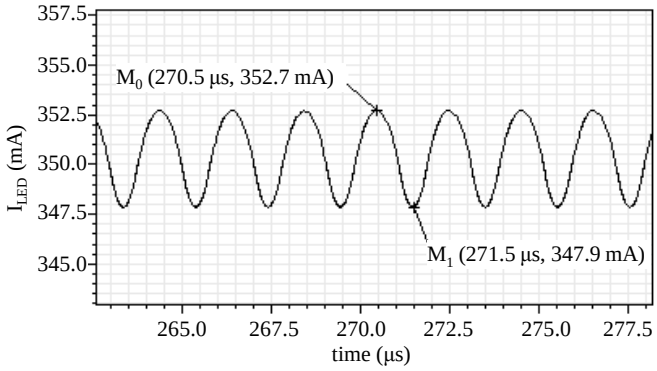

Figure 9. Output drive current ripple when L = 22 μH.

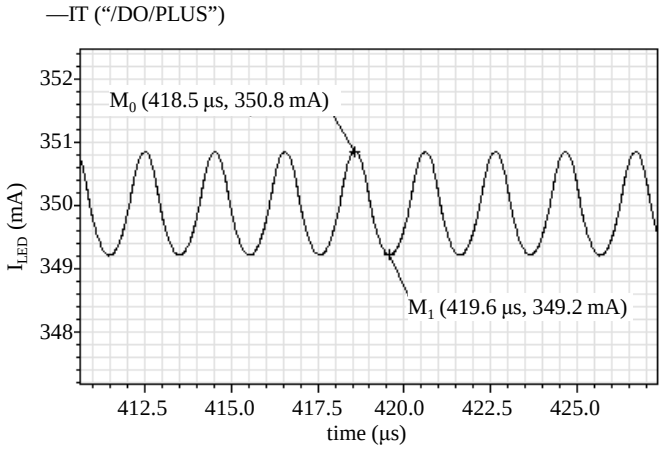

Figure 10. Output drive current ripple when L = 44 μH.

Figure 11 shows the efficiency of HB LED driver circuit. Taking into account the heat dissipation problem of HB LED lights, the simulation curve displays the efficiency when the ambient temperature is 90 degrees celsius. The abscissa denotes the input voltage V_{in}, and the vertical axis is the efficiency. Three curves corresponds different loads from top to bottom, which are eight LED lights, six LED lights and two LED lights. It can be seen that all efficiency are above 91% and the highest is above 96%.

Figure 12 shows the layout of this design. Because the power transistor is integrated into the chip, its power consumption is converted into heat during normal working. During the chip layout, the power MOS transistor should be placed at the edge of chip and an isolation belt has been placed to decrease interference to other circuits. The power supplies of digital and analog circuits should be separated. Considering its larger transient voltage and current in digital circuit, in order to reduce its interference in analog circuits, it is necessary to separate the power supply. It is also paid attention to the total match of difference pair, and the match between resistors and capacitors and so on. The final layout size is 1.4 mm × 1.4 mm.

Using the LED driver chips used in the external topology, the system is verified, mainly focusing on the accuracy of output current and the efficiency at different L values, varied from 22 μH to 55 μH. The number of LED lights remains eight all the time while V_{in} remains 32 V and C_{out} is fixed to be 10 μF. The measured result is shown in **Figure 13**. The output currents remain almost same under different inductors, totally within 0.3% error.

Table 1 shows the test results of the average current and efficiency, in which L = 22 μH, C_{out} = 10 μF, V_{in} = 32 V, and the numbers of 1 W LED lights are 2, 6, 8, respectively.

The average currents, corresponding to different number of LED, are larger than expecation value. The error is less than 1%, which may be caused by the process variation and thermal factors, etc.

The efficiency is 96% with 8 LED lights, 95% with 6 lights and 92% with 2 lights, respectively. The data shows the high efficiency of the designed integrated circuit and the application topology.

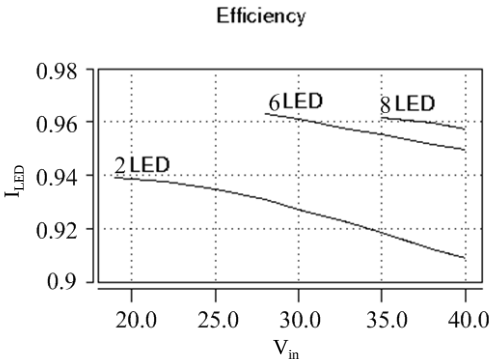

Figure 11. The efficiency of HB LED driver circuit.

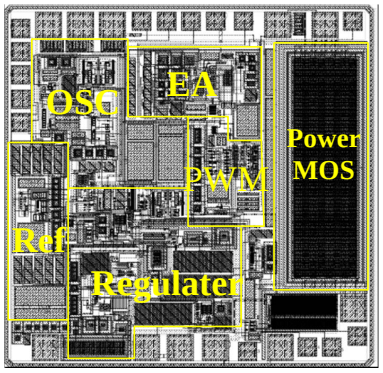

Figure 12. Layout design of the chip.

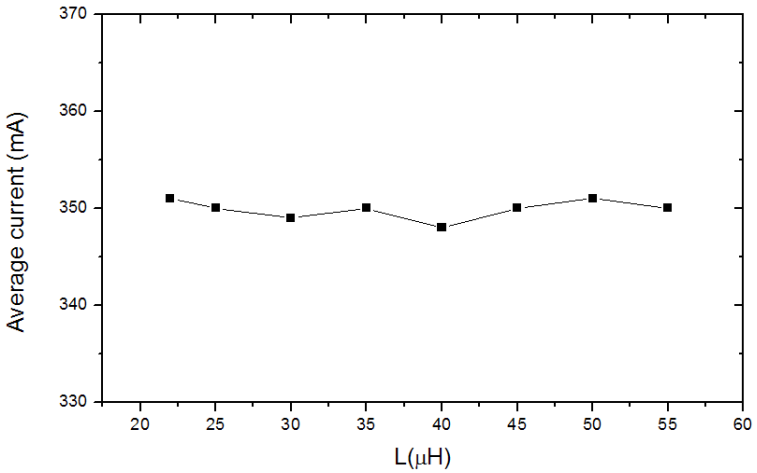

Figure 13. Relationship between average current and the inductance *L*.

Table 1. Main parameters of the test results.

Test parameters	Num. of LED lights	Size	Unit
Average current	2	352	mA
	6	351.5	
	8	350.6	
Efficiency	2	92	%
	6	95	
	8	96	

5. Conclusion

A LED lighting driver has been designed, including an integrated circuit with integral part and the buck converter topology with low-level switch and low-side sense resistor. The integrated circuit has been fabricated based on the CSMC 0.5 μm 40 V BCD process. In this way, the driver with high accurate output current and high efficiency can be obtained. The final result shows that the output current error is less than 1% and the efficiency is above 96%. Since a significant improvement has been obtained, the circuit is potentially applicable for future LED lighting.

Acknowledgements

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