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A 1-GHz, 7-mW, 8-Bit Subranging ADC without Resistor Ladder Using Built-In Threshold Calibration

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Abstract

A subranging analog-to-digital converter (ADC) features high-speed and relatively low-power. The limiting factors of power reduction in subranging ADCs are the resistor ladder and the comparator. We propose an ADC architecture combining a capacitive digital-to-analog convertor and built-in threshold calibration to eliminate the resistor ladder, resulting in a low-power subranging ADC. We also propose a calibration technique comprising of metal-oxide-metal capacitor, MOS switch, and scaling capacitor to reduce the power consumption of the comparator and an offset drift compensation technique to enable precise foreground calibration. We designed an 8-bit, 1-GHz subranging ADC by applying these techniques, and post-layout simulation results demonstrated a power consumption of 7 mW and figure of merit of 51 fJ/conv.-step.

Keywords

Analog-to-Digital Convertor; Subranging Architecture; Resistor Ladder; Foreground Calibration; Offset Drift

1. Introduction

Power reduction in a medium resolution (6 - 8 bit) and high-speed (~1 GHz) analog-to-digital convertor (ADC) is strongly required for front end of wireless systems and read channels of disk systems. To meet this requirement, two approaches have been used so far. The first is based on parallel architecture suited for high-speed operation [1]-[7]. The main challenge in this approach is how power can be reduced while maintaining high-speed

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performance. The second approach is based on successive approximation register architecture suited for low-power operation [8]-[11]. The main challenge in this approach is how operation speed can be improved while maintaining low-power operation. We previously studied the subranging architecture by using the latter approach and proposed a reference voltage precharging architecture [7] and a low-power high-resolution comparator using charge-steering amplifier [4]. There have been studies on high-performance subranging ADCs, e.g., a combination with the time-interleaving technique [5], a reference voltage generator using a capacitive digital-to-analog converter (CDAC) [12] [13] and a low-power comparator using a digital foreground calibration technique [6] [14]. These studies resulted in high-speed and low-power 8-bit subranging ADCs with a sampling frequency of 1 GHz and figure of merit (FOM) of approximately 100 fJ/conv.-step [4] [6]. There are two power-determining factors in state-of-the-art subranging ADCs. The first is a resistor ladder as a reference voltage generator. A resistive ladder requires a large bias current to alleviate the effect of kickback noise from comparators; therefore, reducing the power dissipation is difficult [4]. The second is a comparator. Recently, low-power comparators could be realized using digital foreground calibration; however, there is room for further power reduction because power is wasted due to the large parasitic capacitance of the variable capacitor. Moreover, the digital foreground calibration has an issue of resolution degradation due to the offset drift. Recalibration is required when the temperature changes after calibration. Some applications cannot accept recalibration because AD conversion is suspended during recalibration.

We discuss two power-determining factors in a conventional technique in Section 2. We then propose a low-power ADC architecture without a resistor ladder in Section 3 and propose circuit implementation techniques in Section 4. Finally, we explain the performances of a designed subranging ADC using the proposed techniques through post-layout simulations.

2. Conventional Technique

A block diagram of a conventional subranging ADC [15] is shown in **Figure 1**. This ADC comprises coarse and fine ADCs (CADC and FADC) and converts analog input (V_{in}) into digital outputs (C_{out} and F_{out}) in two stages. The analog input is sampled using a track and hold circuit (TH) and the sampled signal is first converted into an upper digital code by the CADC. The reference voltages for the CADC are generated using a coarse resistor ladder (RLC). Then, appropriate reference voltages (V_{refT} and V_{refB}) are selected using analog multiplexers (AMUX) on the basis of the CADC outputs. The reference voltages for the FADC are generated using a fine resistor ladder (RLF) from V_{refT} and V_{refB} and the FADC generates lower digital codes. The number of comparators is much smaller than that in a flash ADC because the conversion is executed in two steps; therefore, the power dissipation and the chip area can be reduced compared with a flash ADC. There are two bottlenecks to reducing power dissipation. The first is the resistor ladder. A large bias current is required for the resistor ladder to alleviate the effect of kickback noise from the comparators. Recently, a comparator has often comprised only an analog latch without preamplifiers to reduce the power dissipation. In this case, larger bias current is required because large kickback noise is generated by the analog latch. These situations prevent the resistor ladder from reducing power dissipation.

To overcome this problem, a built-in threshold technique using a capacitor [14] and reference voltage generation technique using a CDAC [12] [13] were proposed. With the latter technique, however, the input range was limited because adjustment range of the threshold voltage was small. The input range was only 200 mV [14]. The challenge in reference voltage generation using a CDAC is the gain variation of the CDAC. It has been reported that a gain variation of 15% degenerates the effect number of bit (ENOB) by 0.5 bit [16]. In this study, the ADC generated voltages corresponding to the top and bottom of the FADC input range by the CDAC, and the reference voltages for the FADC were generated by interpolating the top and bottom voltages. As shown in **Figure 2**, this 6-bit ADC comprises a 4-bit CADC and 3-bit FADC, and one-bit is for range overlapping. This ADC has two sets (ch.A and ch. B) of a CDAC and FADC for operation in two-way interleaving. The CDAC outputs the differences (V_{INPa} and V_{INPb}) between the input signal V_{INP} and reference voltages (V_{REFPa} and V_{REFPb}) located up and down theV_{INP}. The threshold voltage of the FADC is generated by interpolating V_{INPa} and V_{INPb}. Interpolation is done by changing the gate width of the input transistors (MPa and MPb) of the comparator. The interpolation relaxes the error due to the gain variation of the CDAC in this architecture. However, this ADC requires four CDACs in total; therefore, the overhead of the chip area and power dissipation is large.

The second bottleneck to power reduction is the comparator. The offset voltage of the comparator is determined by the threshold voltage mismatch of the input differential pair. The threshold voltage mismatch can be

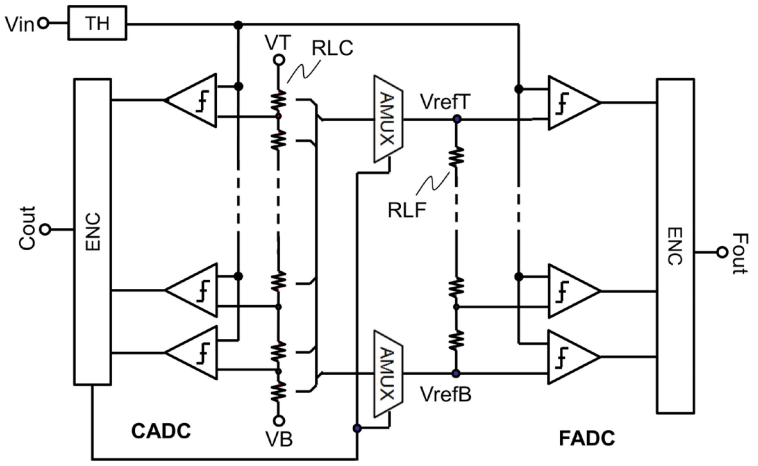

Figure 1. A block diagram of a conventional subranging ADC.

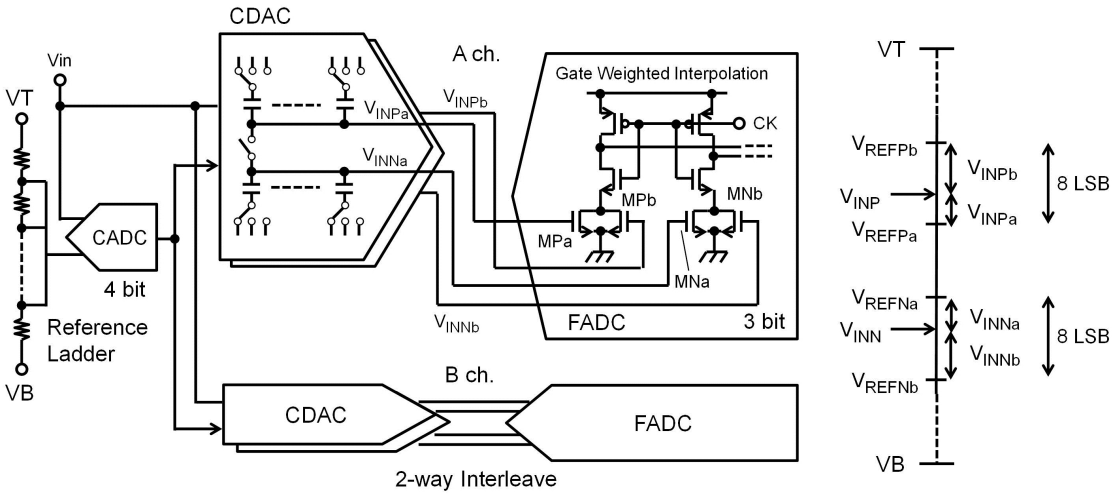

Figure 2. A block diagram of a conventional subranging ADC using capacitive DAC.

reduced by enlarging the gate area; however, the gate area should be very large because the threshold voltage mismatch has only weak dependence on the gate area (proportional to gate area$^{-1/2}$). Therefore, the digital calibration techniques were proposed to compensate for the offset of the comparator. Digital calibration cancels the mismatch due to process variation by intentionally introducing the opposite mismatch. Various mismatch introductions were proposed such as current, capacitance, and back bias [14] [17] [18]. The capacitance mismatch introduction is often used because of small noise and area. However, the comparator with this technique has large power dissipation and a narrow compensation range because the MOS variable capacitor has large parasitic capacitance.

3. Proposed ADC Architecture

The block diagram of the subranging ADC designed using the proposed architecture is shown in **Figure 3**. The ADC comprises a 4-bit CADC and 4.2-bit FADC and converts an analog input V_{in} into 8-bit digital codes *DO*<7:0>. The FADC has 19 comparators for a range overlapping of 2 LSB, each at the top and bottom of the input range of the FADC. The resistor ladder is eliminated; the threshold voltages of the comparators in the CADC and FADC are defined by the built-in threshold technique instead. The input signal of the FADC is generated by the CDAC. The CDAC samples the analog input signal then generates the residue signal subtracted the conversion result of CADC from the analog input signal. The residue signal is converted into lower 4-bit digital codes by the FADC. The timing chart of the designed ADC is also shown in **Figure 3**. The ADC has two sets of

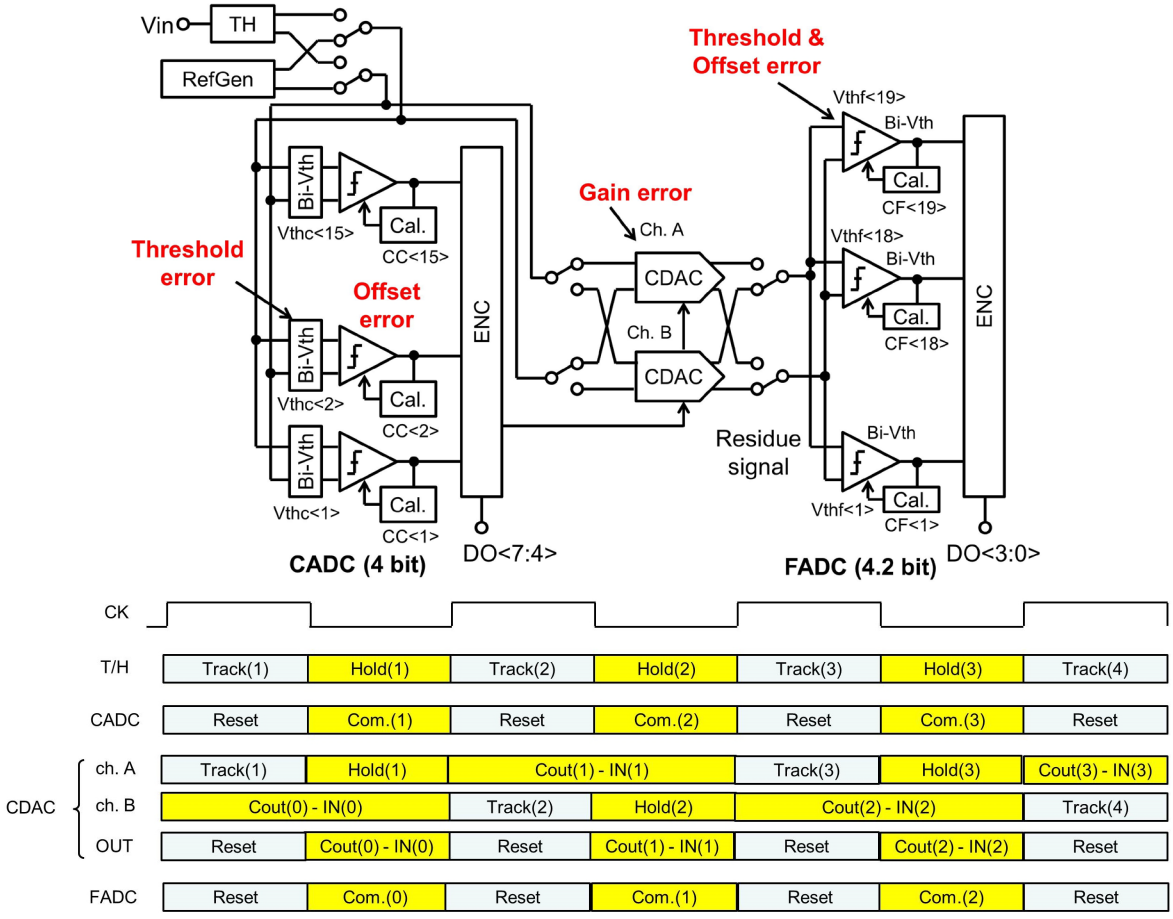

Figure 3. A block diagram and timing chart of proposed ADC.

CDACs (ch.A andch. B) and they operate in two-way interleaving. Therefore, the CADC, CDAC and FADC can use the half the cycle time, resulting in a sufficient timing margin. The error sources in this architecture are the gain error of the CDAC, the offset error of the comparator, and the built-in threshold error. Previous studies compensated for the gain error by using the interpolation technique; however, four CDACs were required to address the interpolation, resulting in large area overhead.

We solve this problem by adjusting the threshold voltages of the FADC in accordance with the gain error of the CDAC by using built-in threshold calibration technique. The calibration sequence in designed ADC is shown in **Figure 4**. Calibration is done individually for the comparators of the CADC and FADC. The TH is first disconnected from the CADC and FADC then a reference voltage generator (RefGen) is connected. The RefGen outputs $V_{thc<1>}$ which is the threshold voltage of the 1st comparator of the CADC (CC<1>). The calibration circuit of CC<1> is then selectively activated. The calibration circuit adjusts the variable capacitor included in the comparator so that the threshold voltage of CC<1> is equal to $V_{thc<1>}$. Next, the RefGen outputs $V_{thc<2>}$ which is the threshold voltage of the 2nd comparator CC<2>, and the same operation is repeated. Therefore, all comparators of the CADC are adjusted to the desired threshold voltage. With this technique, both the error due to the built-in threshold and the offset error are also adjusted, resulting in a precise threshold voltage. After CADC calibration, FADC calibration begins. The RefGen outputs $V_{thf<1>}$ which is the threshold voltage of the 1st comparator of FADC (CF<1>) and the calibration circuit of CF<1> is selectively activated. At this time, all of the gain error of the CDAC, built-in threshold error and the offset error of CF<1>, are compensated because $V_{thf<1>}$ passes through the CDAC. Therefore, the proposed ADC requires only two CDACs, resulting in a small chip area and low-power operation because interpolation is not required. Furthermore, the RefGen comprises a resistor ladder and selector circuit, and the bias current of the resistor ladder is provided only in the calibration mode. Therefore, the RefGendoes not consume power in normal operation.

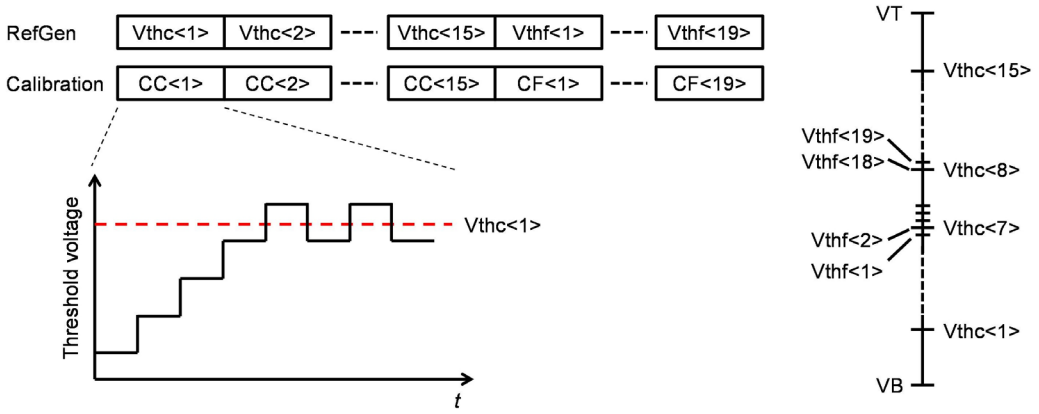

Figure 4. Sequence of built-in threshold calibration.

4. Circuit Implementation

4.1. Built-In Threshold Circuits

Built-in threshold is not a novel technique because a flash ADC using this technique has been already reported [14]; however, some considerations are required to apply it to subranging ADCs. A subranging ADC comprises a CADC with a wide input range and FADC with a narrow input range; therefore, appropriate built-in threshold implementation should be selected for each ADC. The method for changing the ratio of the sampling capacitance is used for the CADC and the method for changing the load capacitance is used for the FADC. Aschematic of the comparator with built-in threshold for the CADC is shown in **Figure 5**. The built-in threshold for the CADC is implemented by splitting the sampling capacitance into C_T and C_B and changing the ratio of $(C_T-C_B)/(C_T+C_B)$ to handle a wide input range. The input signals *INP* and *INN* are connected to the sampling capacitors C_T and C_B in the sampling phase; therefore, the input signal is sampled by the sampling capacitors. The gate voltages of the input differential pair are set to a common voltage V_{com} at this time. In the comparison phase, the switches are connected to V_T and V_B, which are the top and bottom voltages of the input range. Charge redistribution occurs at this time and the gate voltages of the input differential pair are changes around V_{com} depending on the input signals. The threshold voltage is determined as follows.

$$V_{th} = \frac{C_T - C_B}{C_T + C_B}\left(V_T - V_B\right) \tag{1}$$

The threshold voltage can be changed in the range of V_T–V_B by changing C_T and C_B. The sampling switches do not consume power; however, the clock driver dissipates some power. The power dissipation of a comparator including the clock driver is only 30 μW at the operating frequency of 1 GHz.

The built-in threshold of the FADC can be obtained using a simpler method compared with the CADC, as shown in **Figure 6**, because the input range of the FADC is much smaller than that of the CADC. A capacitor C_{bi} is connected to one side drain node of the input differential pair. Positive threshold is generated when the C_{bi} is connected to the drain of the *INP* side. The threshold voltage is expressed as

$$V_{th} = \frac{C_{bi}}{C_{bi} + 2C_p} V_{OD} \tag{2}$$

where C_p is the parasitic capacitance of the drain node and V_{OD} is the overdrive voltage of the differential pair. The power dissipation increases in proportional to C_{bi}; however, the required C_{bi} is approximately 3 fF at most because the variable range of the threshold voltage of the FADC is ±25 mV. Therefore, power dissipation is sufficiently small (less than 20 μW).

4.2. Low-Power and High-Resolution Threshold Voltage Adjustment Technique

Various threshold voltage adjustment techniques for digital calibration have been proposed [19]. The common principle of these techniques is that the threshold voltage can be adjusted by introducing a kind of asymmetry

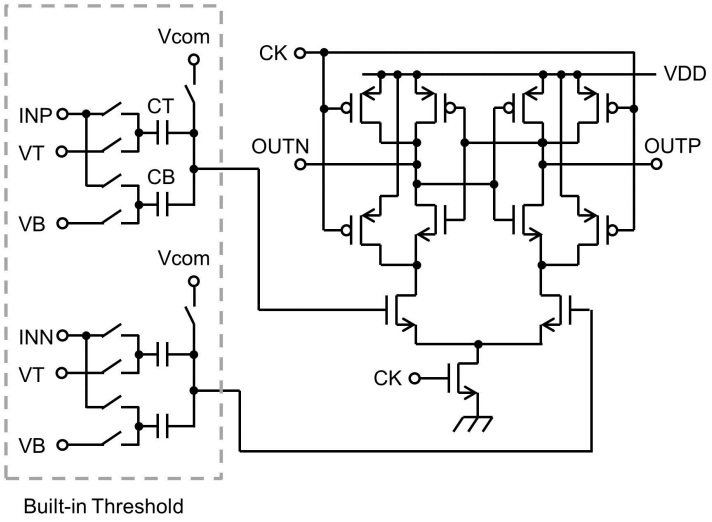

Figure 5. Schematic of built-in threshold circuit for CADC.

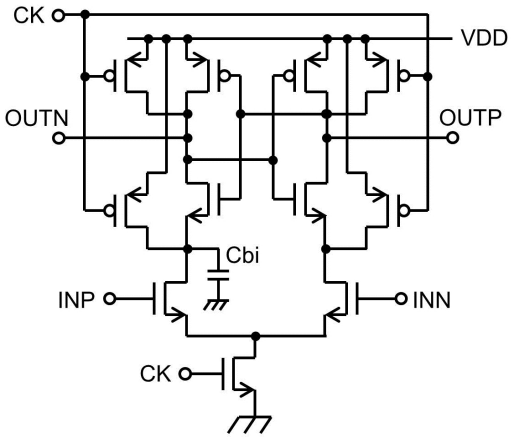

Figure 6. Schematic of built-in threshold circuit for FADC.

into the comparator. For example, the introduction of asymmetry of the load capacitance [14] and the current [17] were proposed. The introduction of asymmetry of the current is not suitable for high-precision ADCs because due to large amount of noise. The introduction of asymmetry of the load capacitor increases the delay time; however, these increase are negligible up to approximately 1 GHz. Therefore, this technique is commonly used in parallel ADCs.

A schematic of a comparator with the threshold voltage adjustment circuit is shown in **Figure 7**. The variable capacitors C_{calP} and C_{calN} are connected to the drain nodes of the input differential pair. The capacitance of the variable capacitor can be changed by the digital control signal (calibration code x). For example, C_{calP} is set to the minimum capacitance and C_{calN} is adjusted to an appropriate value when the threshold voltage of the *INP* side MOS transistor is higher than the nominal value. The minimum value of the variable capacitor is determined by the parasitic capacitance of the MOS transistor. The threshold voltage shift of the comparator can be expressed as

$$\Delta V_{th} = \frac{C(x)}{C(x)+2C_p} V_{OD}, \tag{3}$$

where V_{OD} is the overdrive voltage of the input differential pair and C_p is the minimum value of the variable capacitor. From Equation (3), the adjustment range of the threshold voltage is

$$\Delta V_{th(\max)} = \frac{C_{\max}}{C_{\max} + 2C_p} V_{OD} = \frac{1}{1 + 2C_p / C_{\max}} V_{OD}, \quad (4)$$

where C_{max} is the maximum adjustment range of the variable capacitor, and $\Delta V_{th(\max)}$ can be increased by decreasing C_p/C_{max}.

The MOS variable capacitor is commonly used, as shown in **Figure 8**. The PMOS transistors have binary weighted gate width and the gate capacitance changes according to the gate voltage. The minimum gate width is determined by the fabrication technology, for example, the minimum value is approximately 0.2 μm for 65-nm CMOS technology. The calculated capacitance of the variable capacitor and the threshold voltage of the comparator are also shown in **Figure 8**. The minimum capacitance is very large; more than 40 fF, because the MOS capacitor has parasitic capacitances of the overlapping capacitance and source/drain capacitances. On the contrary, C_{max} is only 15 fF; therefore, C_p/C_{max} is a large value of 3.1, resulting in a small threshold adjustment range of 20 mV. The power consumption in the case of maximum capacitance is also very large; 64 μW at the operating frequency of 1 GHz, due to large capacitance.

Another implementation of a variable capacitor is shown in **Figure 9**. This comprises metal oxide metal (MOM) capacitors and MOS switches. The capacitance can be changed by connecting and disconnecting the MOM capacitors using the MOS switches. A MOM capacitor has smaller parasitic capacitance compared with a MOS capacitor; therefore, C_p/C_{max} can be reduced. The simulation results show that the capacitance increases as the calibration code like stairs; that is, the capacitance jumps every 16 codes. This is due to the parasitic capacitances of the MOS switches. The capacitance change is shown in **Figure 10** when the calibration code changes from 15 to 16. The MOM capacitors are connected to GND when the MOS switches are on. However, the

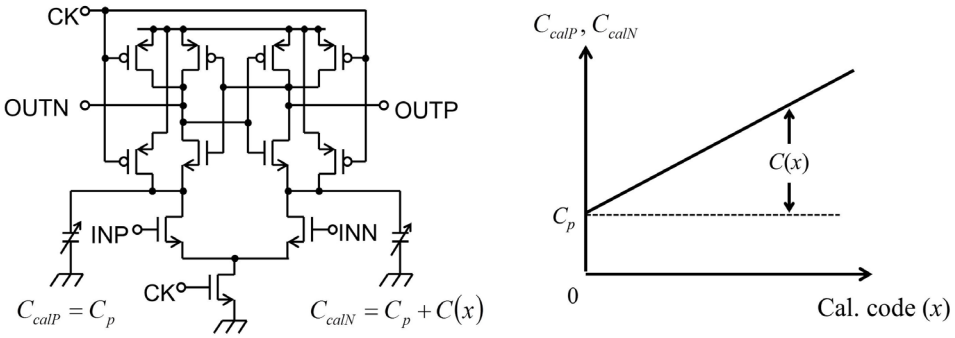

Figure 7. Schematic of a comparator with the threshold voltage adjustment circuit.

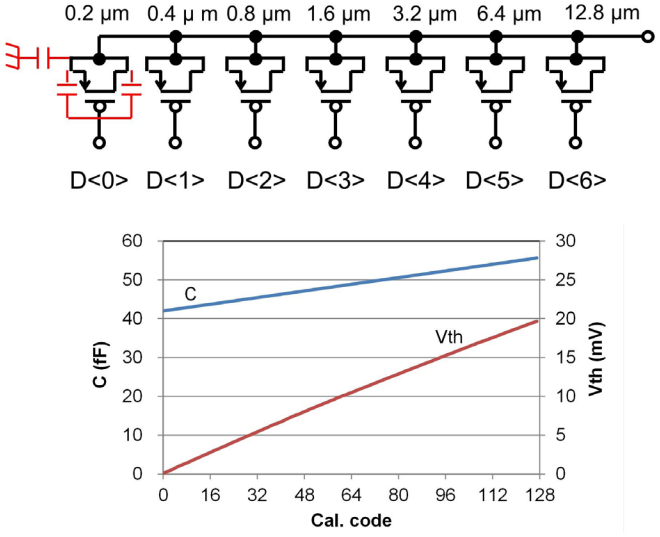

Figure 8. MOS variable capacitor.

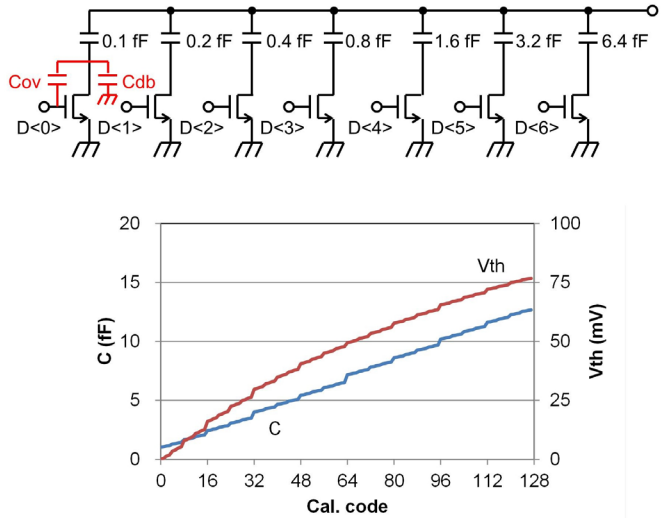

Figure 9. Variable capacitor comprised of MOM capacitors and MOS switches.

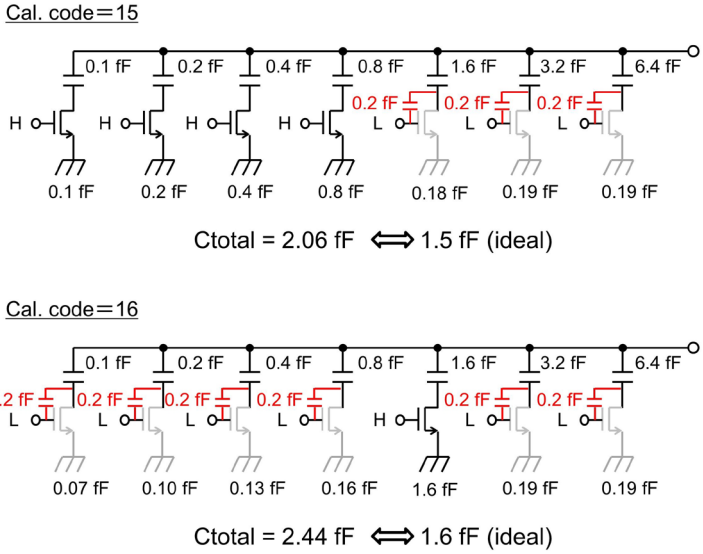

Figure 10. Capacitance change in variable capacitor.

overlapping capacitance (C_{ov}) and drain-body capacitance (C_{db}) are connected to the MOM capacitors in serial when the MOS switches are off; therefore, the MOS capacitors cannot be disconnected completely. The parasitic capacitance (C_{ov} + C_{db}) is approximately 0.2 fF when the gate width of the MOS switch is 0.2 μm. For example, the capacitance decreases by only 30% in the case of smallest capacitance (0.1 fF) when the MOS switch is off because the parasitic capacitance is larger than the MOM capacitance. This causes a large jump in the total capacitance when the calibration code changes from 15 to 16, as shown in **Figure 10**. The large jump in the total capacitance causes a large threshold voltage change (3.5 mV in the case of **Figure 10**), resulting in low-precision calibration.

We propose the low-power and high-resolution threshold voltage adjustment technique, as shown in **Figure 11**. This variable capacitor comprises MOM capacitors and MOS switches. A relatively large MOM capacitance (2.1 fF) is selected to reduce the effect of the parasitic capacitance of the MOS switches. This enables the capacitance to decrease by 90% when the switch is off; however, larger MOM capacitance increases power dissipation. Therefore, scaling capacitors (4.1 fF and 17.4 fF) are introduced in serial. Scaling capacitors effectively reduce the total capacitance; therefore, a variable range of 3.7 to 8.7 fF can be achieved, resulting in small

C_p/C_{max} of 0.7. The threshold adjustment range is 40 mV and the maximum threshold jump is 1.0 mV. The power dissipation is only 19 μW when the variable capacitance is maximum value.

4.3. Offset Drift Compensation Technique

One of the issues in putting foreground calibration to practical use is the offset drift due to temperature change. Foreground calibration measures the offset at a certain temperature and compensates for it; therefore, the offset cannot be perfectly compensated when the temperature changes after calibration because the offset changes depending on the temperature. We analyze the mechanism of offset drift using a simple model and propose a drift compensation technique. The analysis model of the offset drift is shown in **Figure 12**. The offset in a comparator is approximately determined by the mismatch of the differential pair; therefore, we developed an offset drift model focusing on the differential pair. The various mismatches in the differential pair cause offset voltage. We consider the mismatch of the threshold voltage and transistor size. The offset voltage can be expressed as

$$V_{off} = -\Delta V_{TH} + \frac{V_{com} - V_{TH}}{2}\frac{\Delta(W/L)}{(W/L)}, \tag{5}$$

where V_{com} is the input common level. The first term is the mismatch of the threshold voltage, which mainly occurs due to the variability of the channel dopant concentration. The second term is due to the variability of the channel size. The offset drift can be obtained by differentiating this equation with respect to temperature.

$$\frac{dV_{off}}{dT} = -\left[\frac{d\Delta V_{TH}}{dT} + \frac{1}{2}\left(-\frac{dV_{com}}{dT} + \frac{dV_{TH}}{dT}\right)\frac{\Delta(W/L)}{(W/L)}\right] \tag{6}$$

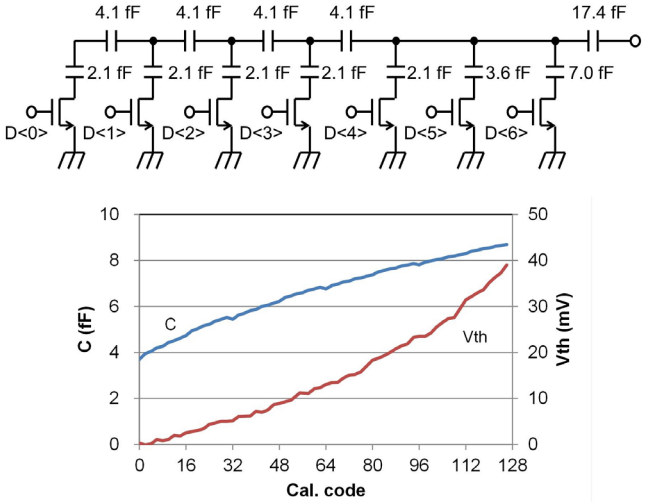

Figure 11. Proposed variable capacitor.

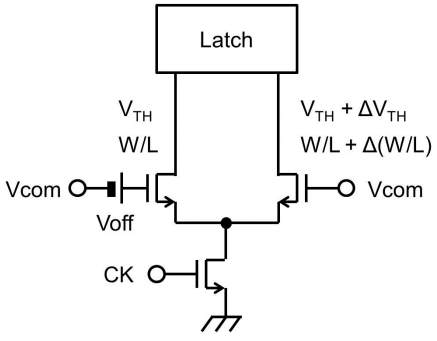

Figure 12. Offset drift model.

The first and second terms fluctuate without correlation because their physical factors of variability are completely different. Therefore, the offset drifts of two comparators are different even when they have the same initial offset voltage because the breakdown of the offsets (the amount of the first and second terms) is different. Therefore, the offset drift compensation on the basis of the initial offset fails. However, the offset drift can be reduced if dV_{com}/dT equals dV_{TH}/dT because this condition nullifies the second term. **Figure 13** shows the dV_{com}/dT dependence of the offset variation. Calibration was done at 25˚C, then the temperature was raised to 85˚C and the offset change was simulated. The offset voltage immediately after calibration was 0.29 mV. The offset voltage at 85˚C increased by 0.8 mV when $dV_{com}/dT = 0$. The offset voltage change, however, could be suppressed to 0.1 mV when $dV_{com}/dT = -0.6$ mV/˚C.

5. Post-Layout Simulation Results

The proposed ADC has been designed in a 65-nm digital CMOS technology. **Figure 14** shows a layout plot of the ADC. The CDAC is located between CADC and FADC to shorten the analog input signal line. The core area excluding the output buffer is 520 × 370 μm. The supply voltage is 0.8 V and power dissipation is 7 mW at a sampling frequency of 1 GHz. **Figure 15** shows the simulated input frequency dependence of the signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR). The simulation was conducted using the netlist extracted from the layout pattern. The SNDR and SFDR were approximately constant from 10 MHz to 1 GHz. **Figure 16** shows the simulated sampling frequency dependence of the SNDR and SFDR. The SNDR dropped when the sampling frequency exceeded 1 GHz. The reason performance degraded over 1 GHz was the timing margin failure in the encoder. **Figure 17** shows the simulation results of calibration. A large error occurred due to mismatch before calibration, resulting in a poor SNDR and SFDR of 23.7 and 35.5 dB, respectively. The calibration greatly improved the SNDR and SFDR to 45.5 and 53.8 dB, respectively. **Table 1** summarizes the ADC performance and the recently developed ADCs in similar target specifications [4] [6] [20] [21]. Our ADC demonstrates the lowest FOM of 51 fJ/conv.-step in the subranging ADCs. The SAR ADC [20] exhibits very low FOM; however, good performance is possible using 32-nm CMOS technology.

Table 1. Performance comparison.

	This work (Post-layout sim.)	A-SSCC 12 K. Ohhata [4]	VLSI 11 Y.-H. Chung [6]	ISSCC 13 L. Kull [20]	VLSI 13 S. W. Chiang [21]
Architecture	Subranging	Subranging	Subranging	SAR	Pipeline
Technology (nm)	65	65	55	32	65
Resolution (bit)	8	8	8	8	10
Fs (MS/s)	1000	1000	1000	1200	800
SNDR (dB) @Low freq.	45.0	45.2	43.5	39.4	55.0
SNDR (dB) @Nyquist freq.	44.5	42.4	39.2	39.3	52.2
Supply voltage (V)	0.8	1.0	1.2	1.0	1.0
Power (mW)	7.0	17.5	16.0	3.1	19.0
FOM (fj/conv.-step)	51	118	125	34	53
Area (mm^2)	0.19	0.25	0.2	0.0015	0.18

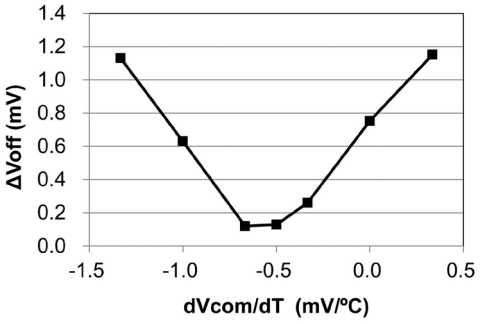

Figure 13. dV_{com}/dT dependence of the offset variation.

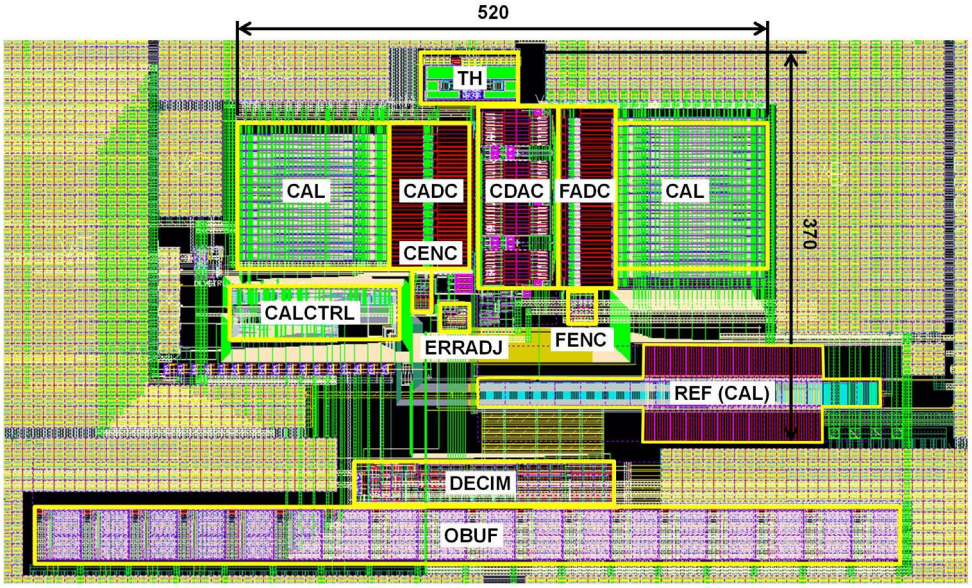

Figure 14. Layout plot of designed ADC.

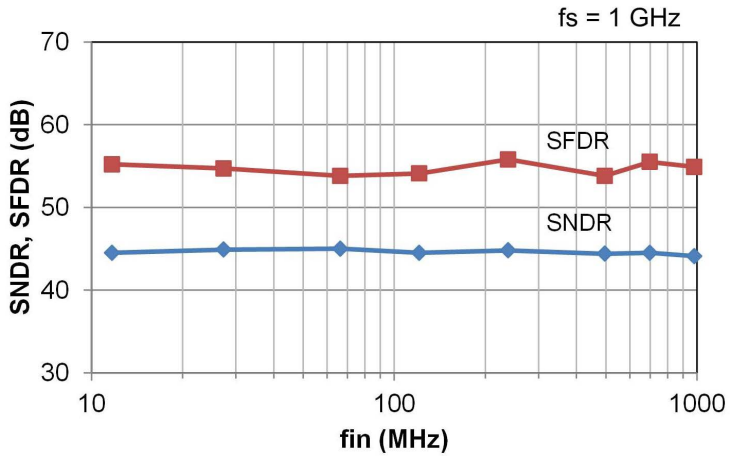

Figure 15. Simulated input frequency dependence of SNDR and SFDR.

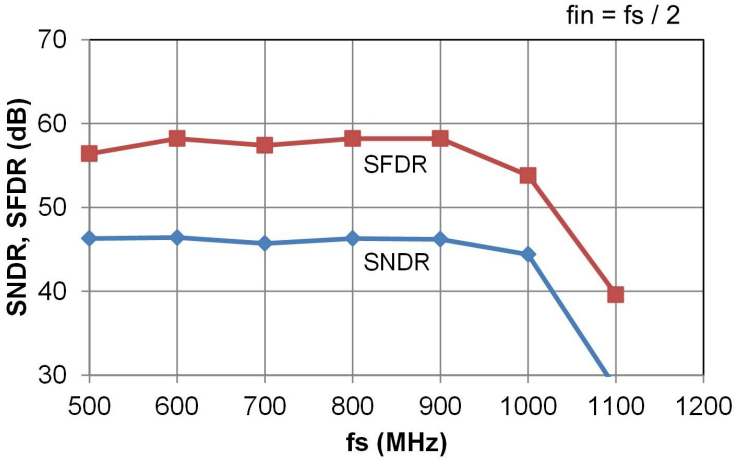

Figure 16. Simulated sampling frequency dependence of SNDR and SFDR.

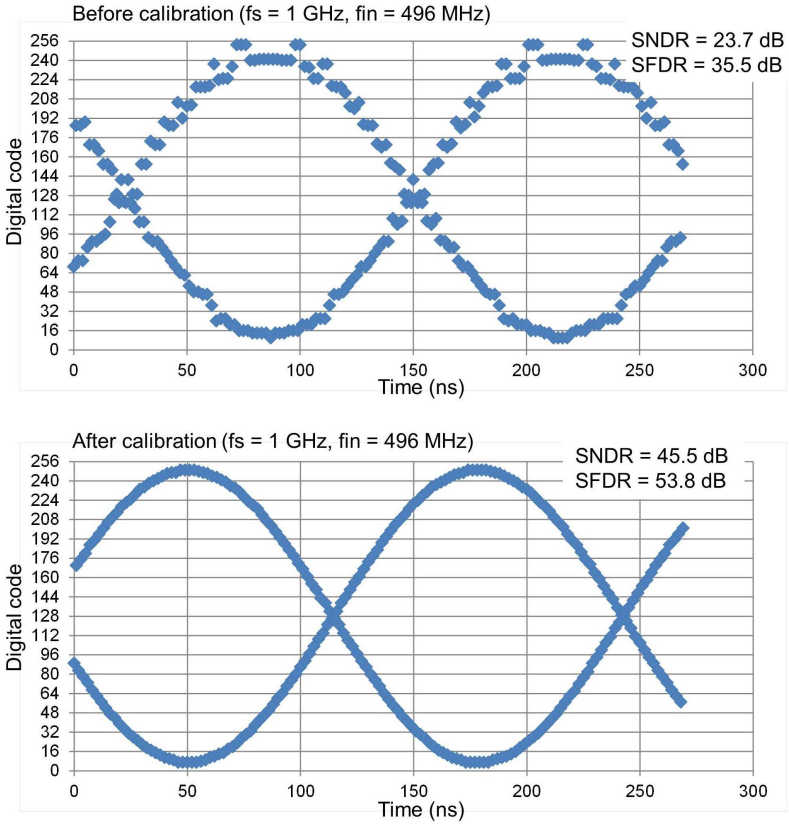

Figure 17. Simulation results of calibration.

6. Conclusion

We proposed an ADC architecture combining a capacitive DAC and a built-in threshold calibration to eliminate the resistor ladder, resulting in a low-power subranging ADC. We also proposed a variable capacitor using scaling capacitance to reduce power dissipation of the comparator and an offset drift compensation technique for high-precision foreground calibration. The designed ADC combining these techniques achieves a high sampling frequency of 1 GHz and low power dissipation of 7 mW, resulting in an FOM of 51 fJ/conv.-step.

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