Circuits and Systems, **2013, 4, 304-315**
http://dx.doi.org/10.4236/cs.2013.43042 Published Online July 2013 (http://www.scirp.org/journal/cs)

A Low Phase Noise Ring-VCO Based PLL Using Injection Locking for ZigBee Applications

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Received April 26, 2013; revised May 27, 2013; accepted June 4, 2013

ABSTRACT

A low power low phase noise frequency synthesizer with subharmonic injection locking is proposed for ZigBee applications. The PLL is based on a ring VCO to decrease area and production cost. In order to improve phase noise performance, a high frequency injection signal of which frequency varies with channel number is used. The circuit is designed in TSMC 0.18 μm CMOS technology and simulated in ADS (Advanced Design System). The phase noise at 3.5 and 10 MHz offsets is −116 and −118 dBc/Hz, respectively, and total circuit consumes 2.2 mA current.

Keywords: ZigBee; Frequency Synthesizer; Phased Locked Loop; Injection Locking Technique

1. Introduction

The necessity for mobile computing and networking has led to the development of various wireless standards over the last decade. One of these standards is IEEE 802.15.4/ ZigBee that has been recently developed to provide the needs of low power, low data rate, low production cost, and short range wireless networks. This new standard is specifically related to applications such as data monitoring, industrial control and sensor networks [1].

To reduce production cost, single chip solutions are required. To cater this need, great efforts are made to develop those systems using highly scaled advanced CMOS processes. These processes are advantageous to some circuits and applications such as analog-to-digital (A/D) and digital-to-analog (D/A) converters and digital baseband circuits. However, it is very difficult to reduce the scale of RF/analog circuit blocks, such as voltage-controlled oscillators (VCOs), phase-locked loops (PLLs) and power amplifiers, because of the presence of inductors that does not scale with advancements in technology [2].

PLLs are one of the most important building blocks in RF transceivers, because they provide a precise frequency for transmit and receive data paths. PLLs use two types of oscillators: Ring and LC VCOs. Ring-type VCOs (ring VCOs) are more attractive than LC-type VCOs (LC VCOs) because ring VCOs have more scalability and wide-band operation. However, they suffer from poor phasenoise, which is one of the most important parameters in designing a frequency synthesizer. Therefore, ring VCOs cannot be used for some applications, such as wireless LANs and cellular phones. However, if there is a method that can alleviate the poor phase noise problem, the ring VCOs can be introduced as a good option for many applications. One of these ways is using injection locking technique [3].

Many authors [4-6] have studied the behavior of injection locked oscillators so far. In addition, there are many papers and publications that have explained the specifications of injection locked PLLs [7-10]. The injection locking technique is also implementable on some other circuits such as clock and data recovery (CDR) circuits, injection locked frequency dividers (ILFD), and injection locked frequency multipliers (ILFM).

This paper presents a frequency synthesizer for ZigBee applications. The proposed frequency synthesizer is composed of two PLL stages. Since an oscillator with low output frequency may have desirable phase noise specification in all offset frequencies [11], we design a low frequency and low phase noise ring VCO in the first stage PLL (PLL1), and in the second stage PLL (PLL2) we use injection locking technique so that to obtain the same phase noise specification in the PLL2 output (with little degradation that is negligible). It is obvious that with single stage PLL that has a high frequency and inferior phase noise specification, this goal could not be achieved.

2. Proposed Structure

Figure 1 shows the structure of the proposed frequency synthesizer. It consists of two stages PLL. First stage PLL (PLL1) has a reference frequency of 1.25 MHz and a divider with variable division ratio that works in swallow way and divides the output frequency of the PLL to 481 - 496. Consequently, the output frequency of this PLL varies between 601.25 MHz to 620 MHz. The channel for data transmission is determined by this stage. The second stage uses the output frequency of PLL1 as its reference signal. The divider of this PLL has a fixed division factor of 4, therefore the output frequency of this stage varies between 2405 MHz to 2480 MHz with 5 MHz steps. Consequently this frequency synthesizer covers all of the ZigBee channels.

In fact, if the oscillation frequency is low, achieving low phase noise and high Q (Quality factor) specification in oscillators will be easier, especially in ring oscillators. So we design a low phase noise and high Q ring oscillator with a center frequency of 610 MHz for PLL1, and in PLL2 we use the injection locking technique to have similar low phase noise in the output signal of frequency synthesizer with a little degradation.

One serious issue related to the injection-locked PLLs is the possible conflict between the two locking signal references: the phase locking (from the reference signal for the loop) and the injection locking (from the injection signal). In practice, the injection-locked PLL would automatically adjust the phase relationship to maintain the stability and accomplish the noise suppression [7]. To resolve this issue, a delay block (ΔT) must be put in the path of injection signal to adjust the proper phase for it, in otherwise PLL can't lock onto two reference signals. If PLL can't lock onto two signals, PLL only locks onto the reference signal for the loop and the injection signal acts as a noise on the control voltage of the VCO, consequently degrades the phase noise. It is necessary to mention that this case occurs usually when division factor of the divider, or in other words, division ratio between reference signal and output signal of the PLL, is very large. Consequently, it is impossible to use injection locking technique for PLL1 with division ratio of 481 - 496.

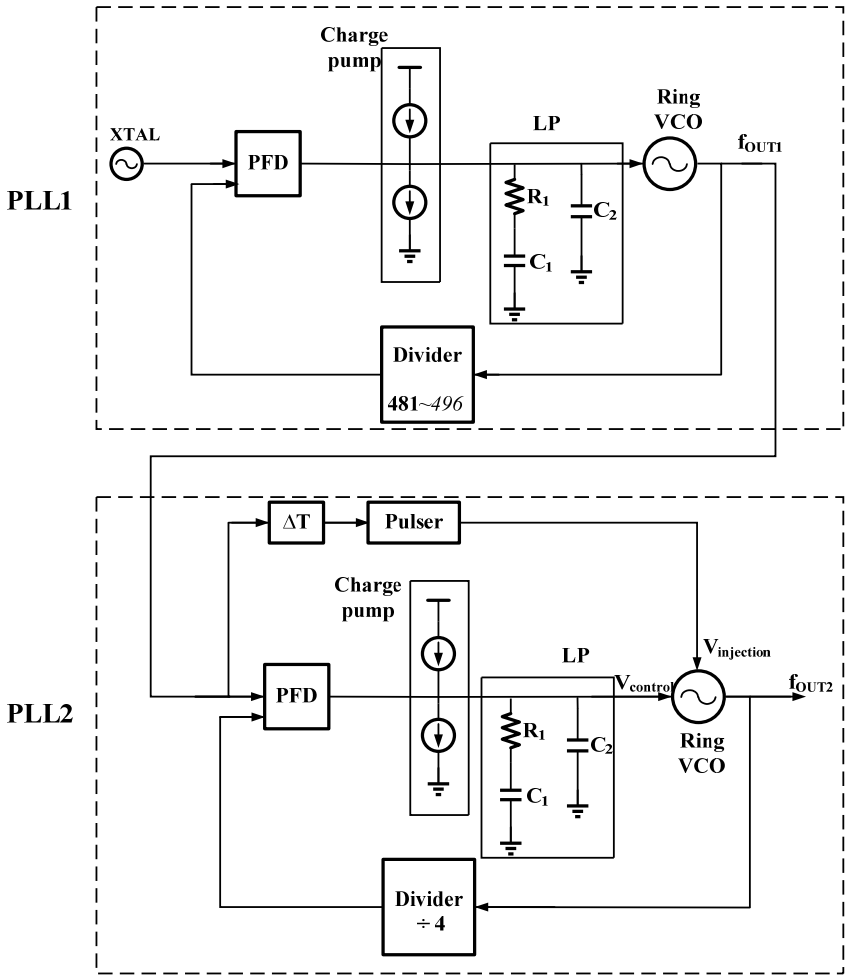

Figure 1. Proposed structure for frequency synthesizer.

3. Phase Noise Reduction with Injection Locking

Figure 2 demonstrates the reason that in injection-locked PLLs, the jitter, namely phase noise characteristics, can be reduced. The jitter will be spread over time when a VCO is in the free-running situation (**Figure 2(a)**). When a pulse signal is injected to the VCO at T_{inj} (**Figure 2(b)**), the phase of the VCO output aligns with the injected signal phase. In this condition, the phase correction occurs at T_{inj} and the jitter will be reduced because the clean edge of the injected pulse replaces the noisy edge of the VCO output as shown in **Figure 2(b)**. **Figure 2(c)** shows the jitter specification of a typical PLL output [12]. Consequently, we can see that the best phase noise operation is in the injection locked PLLs (**Figure 2(d)**).

As ring oscillators have poor phase noise characteristic, if they want to work in high frequencies, should be used in PLLs with high frequency references. However, there is a tradeoff between the stability and bandwidth of PLLs. To guarantee the stability, the bandwidth of PLL is roughly chosen as one tenth of input frequency in typical designs.

The low frequency phase noise of VCO is filtered out by the PLL from DC to the bandwidth of PLL. So, increasing the PLL bandwidth reduces the phase noise, but at the same time, reduces the stability, as explained above. Consequently, there is limitation on lowering the phase noise in ring-VCO-based charge-pump PLLs (CP PLLs). The phase noise characteristic of a PLL is shown in **Figure 3**.

In this case, the charge-pump noise of the PLL is assumed to be sufficiently small and can be neglected. In this figure, the noise filtering of the loop has suppressed the phase noise up to the loop bandwidth (ω_{-3dB}) [3].

Injection locking technique is an effective way for reducing the phase noise of oscillators specially ring types, since ring VCOs have a wide locking range with injection locking compared to LC VCOs because of their low quality factors due to topologies [3].

In subharmonically injection-locked oscillators, the frequency of injection signal is $1/N$ of the output frequency of oscillator. The lock range is determined by the power of the N^{th} superharmonic of the reference signal as

$$\omega_L = \frac{\omega_{out}}{2Q} \cdot \sqrt{\frac{P_{inj,N}}{P_0}} \quad (1)$$

where Q is the quality factor of the oscillator, ω_{out} represents the output frequency of the oscillator under the injection locked condition, $P_{inj,N}$ is the N^{th} harmonic power of the reference signal, and P_0 is the free-running output power of the oscillator [3].

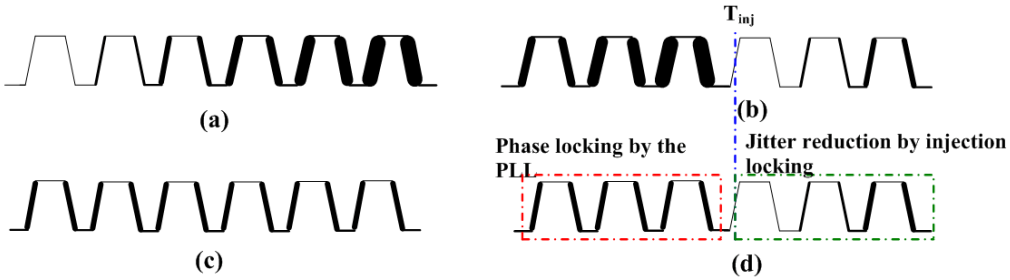

Figure 2. Conceptual phase evolution over time in an injection locked PLL [12]. (a) Freerunning VCO; (b) Injection locked VCO; (c) Conventional PLL; (d) Injection locked PLL.

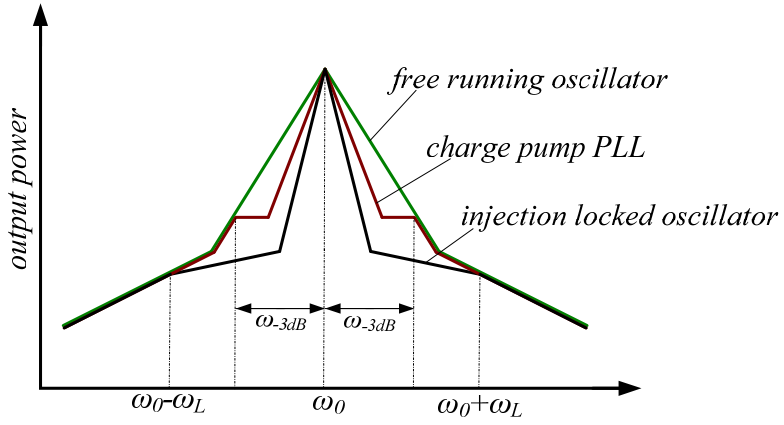

Figure 3. Phase noise reduction with injection locking [3].

Locking range determines the phase noise characteristics of the injection-locked PLL. When the bandwidth of the PLL is sufficiently wider than the locking rang, injection locked PLL behaves like a simple PLL that only is locked onto the reference signal for the loop. In this situation, phase noise is determined by phase lock operation. On the other hand, when the locking rang is sufficiently wider than the loop bandwidth, the phase noise is determined by injection locking operation. This is occurred in ring VCO-based PLL [7].

4. Injection Signal Specifications

There are several ways to inject a signal to the VCO. One of them is to use an NMOS switch that connects the differential nodes of the VCO. When injection pulse becomes high, the switch turns on and differential nodes are shorted together, consequently phase noise reduction occurs [13].

Since this way uses the shortening between the differential nodes, duration of the correcting pulse has some limitations. In reality, oscillation period makes this limitation so that pulses with widths smaller than rise/fall time of the output signal of the VCO is suitable for injecting. In otherwise, if injection pulse width is too small, a small current flows through the switch and injection locking doesn't have enough energy for correcting the phase, even locking process may be failed. On the other hand, if width of injection pulse is larger than the rise/fall time of output signal of PLL, a large amount of current will be injected to the differential nodes and a large rotation in phase signal or a large spurious level may be occurred [3].

Moreover, the oscillation may prevent due to addingin-phase energy to the oscillators by injection and weakens the negative conductance circuits [3,5].

In the proposed PLL, since correction signal is injected to second stage PLL and its output frequency is 2.4 GHz, the injection pulse width is 50 ps. This signal is produced by the circuit is shown in **Figure 4** [7]. Output frequency of this circuit is double of its input frequency that makes injection locking process more effective.

5. Building Blocks of Frequency Synthesizer

5.1. VCO

Figure 5 shows the block diagram of the Ring VCO that is used in PLL1 (VCO1) and PLL2 (VCO2). **Figure 6** shows the delay cell schematic of each one. Performance and function of this type of ring VCO is explained in [14] in detail. The delay cell includes an NMOS transconductance pair, a PMOS cross-coupled load, a PMOS diode pair for the best power-consumption efficiency [14].

Based on the three stage topology for the VCO2 the oscillator loop gain can be expressed as

$$H(s) = -\left(\frac{g_{mn1}}{\left(G_{ds} + g_{mp2} - g_{mp1}\right) + sC_L}\right)^3 \quad (2)$$

where $G_{ds} = g_{dsn1} + g_{dsp1} + g_{dsp2}$ is the resistive load because of the channel-length modulation. The negative sign is due to changing polarity of the three stages. Based on the *Barkhausen* criteria, each delay cell provides 60˚ phase shift and a unit gain at the oscillation frequency. Satisfying the phase condition requires $G_{ds} + g_{mp2} - g_{mp1}$ be much smaller than sC_L [14].

But this structure has a very high VCO gain (K_{VCO}). As K_{VCO} increases, PLL performance characteristics, such as the stability of the loop, and spurious levels in VCO output signal are degraded. Large loop filters are needed to resolve these problems [3]. The circuit shown in **Figure 7** is used to decrease the VCO gain and increase the linearity of K_{VCO}. By adjusting R_1 and R_2 the desired K_{VCO} is provided. In addition, this circuit is used

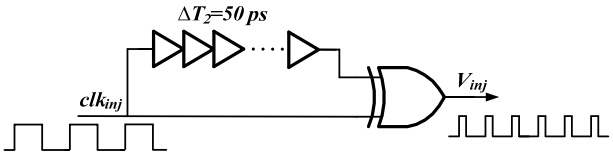

Figure 4. Injection pulse generator circuit.

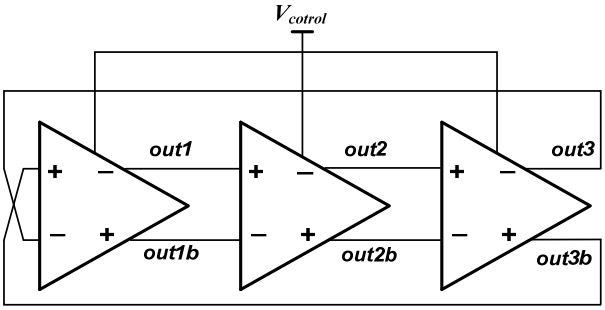

Figure 5. The block diagram of the Ring VCO used in PLL1 (VCO1) and PLL2 (VCO2).

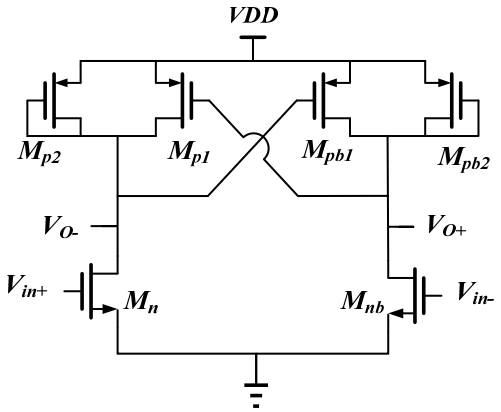

Figure 6. The delay cell schematic of ring oscillators.

to provide the supply voltage (V_{ctrl}) for the VCO.

VCO2 has the same general function of VCO1 except that it uses a very small capacitor to decrease the oscillation frequency and improve the phase noise characteristic.

5.2. Phase-Frequency Detector and Charge Pump

Both of the two stage PLLs, PLL1 and PLL2 use the phase-frequency detector (PFD) proposed in [15]. This is a novel PFD that prevents generating the reset signal when the input phase error is out of the range of $[-\pi, \pi]$. As a result, this PFD eliminates the "blind zone" completely and so reduces the settling time of the loop [15].

Figure 8 shows the logic schematic of this PFD. It is an improved model of the classical PFD, that uses two more OR gates and an additional *Start* signal in its structure and its mechanism is explained in [15] completely.

Two stages of PLLs use a simple charge pump that is introduced in [11]. The circuit of this charge pump is shown in **Figure 9**.

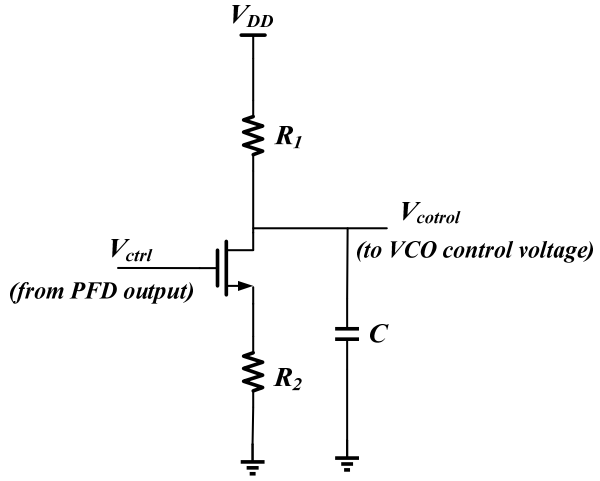

Figure 7. The circuit is used to decrease the VCO gain and increase the linearity of K_{VCO}.

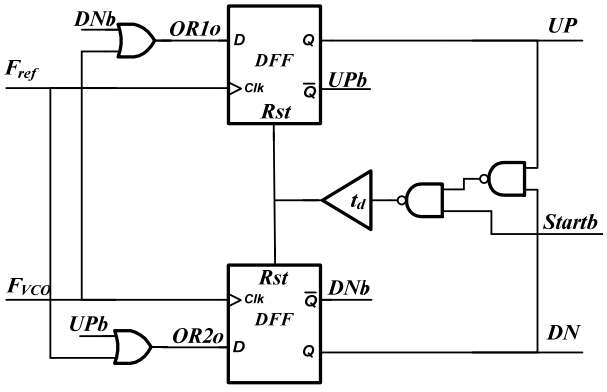

Figure 8. PFD schematic [15].

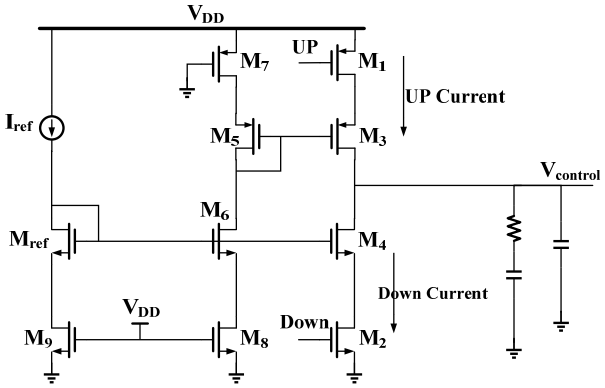

Figure 9. Charge pump circuit [11].

5.3. Frequency Divider

PLL1 uses a new low power frequency divider proposed in [16]. This frequency divider consists of a dual modulus prescaler and a divide-by-64. In order to reduce the power consumption, Swallow counter has been replaced by a simple digital circuit [16]. **Figure 10** shows the proposed frequency divider.

Figure 11 shows the dual modulus prescaler and **Figure 12** shows the integrated program and swallow counter of the proposed divider. For more details division process refer to [16].

It divides the input frequency to 481 - 496 and so covers all of the ZigBee channels.

PLL2 uses a simple divider with divide ratio of 4 that is composed of two TSPC D-flip flops. **Figure 13** shows this divider.

6. PLL Design

All of the building blocks of the two PLLs are explained in the previous sections. This section explains the low pass filter design. A second order filter is used for the two stages (the schematic of this filter is shown in **Figure 1**). The values of the resistors and capacitors for the two stage PLLs are:

PLL1: R = 353 kΩ, C_1 = 20 pF, C_2 = 4 pF.

PLL2: R = 36 kΩ, C_1 = 4 pF, C_2 = 1.5 pF.

7. Simulation Results

This frequency synthesizer is designed in TSMC 0.18 μm CMOS technology and simulated in ADS. Simulation results are presented for channel 12 with frequency of 2.46 GHz. In this condition, PLL1 output frequency is 615 MHz.

Figure 14 shows the spectrum of PLL1 output frequency. The spur rejection at 5 and 10 MHz is −54 and −62.4 dB, respectively that remarkably satisfies ZigBee specifications remarkably. ZigBee requires at least −13 and −43 dB spur rejection at 5 and 10MHz offsets, respectively. Of course, it is the spur rejection for the first

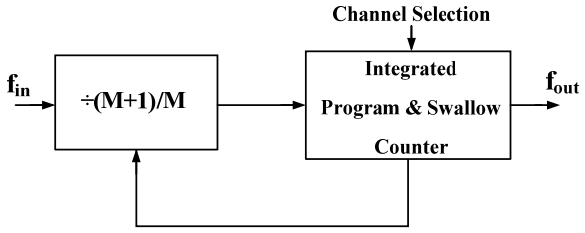

Figure 10. The frequency divider for PLL1 [16].

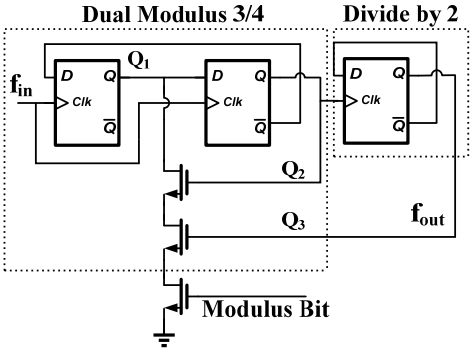

Figure 11. 7/8 dual modulus prescaler [16].

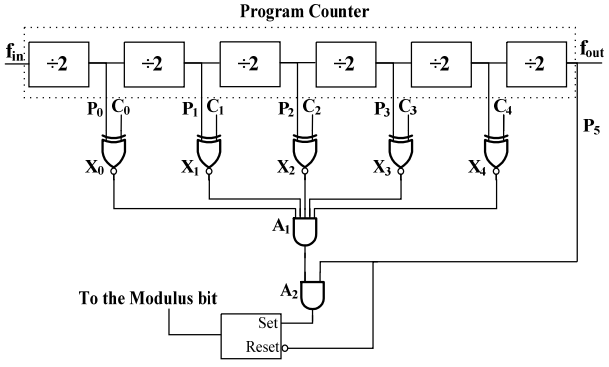

Figure 12. The integrated program and swallow counter.

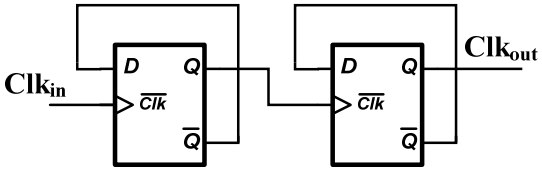

Figure 13. The PLL2 divider.

stage PLL, but as second stage has a reference signal with center frequency of 610 MHz and 1.2 GHz injection signal, their spurs are occurred at 610 MHz and 1.2 GHz frequencies and the spurs of the first stage output spectrum emerge at the harmonics of these two frequencies, in other words, roughly at the harmonics of 610 MHz.

Figure 15 shows the phase noise of free running VCO and PLL1. As depicted in this figure, after frequency offset of about 1 MHz the phase noise characteristic of the VCO matches that of the PLL. PLL1 output phase noise at 1 MHz offset frequency is −106.8 dBc/Hz.

As mentioned before, output signal of the first stage is used both as the second stage reference signal and as the injection pulse. Simulation tools such as ADS are not able to exactly calculate phase noise of injection locked PLLs. But as PLL2 uses a low Q ring-VCO, it has a wide locking range with respect to its loop bandwidth. Therefore, its phase noise characteristic is determined by injection pulse phase noise shape, in other words it works such as a single VCO with the injection locking condition. So simulating the single VCO with the injection locking has a result similar to simulating injection locked PLL.

For simplicity a single clock source with equivalent jitter to the output phase noise of PLL1 (rms jitter = 3.6 picoseconds that is calculated by integrating phase noise over 10 Hz to 100 MHz offset frequencies) is used instead of PLL1 in simulating PLL2. **Figure 16** shows phase noise characteristics of VCO2 with and without injection. The phase noise at 3.5 and 10 MHz offset frequencies is −116 and −118 dBc/Hz respectively that shows about 15 dBc/Hz improvement in phase noise at 3.5 MHz offset (without injection locking phase noise at 3.5 MHz offset is −101.5 dB/Hz).

Figure 17 shows the output signal spectrum of PLL2 without injection locking and **Figure 18** shows it with injection locking.

As the reference signal (with 615 MHz frequency) and injection pulse (with 1.23 GHz frequency) for PLL2 have high frequency, output signal of frequency synthesizer has no important spurs at offset frequencies near the main frequency (at 5 and 10 MHz offsets) and the filters in the transceiver eliminate these spurs. The general form of an injection locked PLL output spectrum and its spurs can be seen in **Figure 18** obviously.

Figure 19 shows the V_{cont} (control voltage) signal for PLL2 and transient behavior of it. PLL1 has 25 μs and PLL2 (with injection locking) has 3 μs settling time, so total frequency synthesizer has 28 μs settling time that notably provides ZigBee specification.

PLL1 and PLL2 draw 2 mA and 2.2 mA form a 1.8 V supply, respectively. Therefore, total power consumption is 7.5 mw for the complete frequency synthesizer.

As frequency synthesizer subsystems such as PFD, charge pump, LPF, and frequency divider are not sensitive to temperature and process (in this application), and VCO is the most sensitive subsystem, for testing synthesizer in technology corners, just VCO is simulated. **Figure 20** shows VCO1 behavior in the process corners. As depicted in this figure, the value of K_{VCO} has a little change in the four corners, but the frequency has about 20% change in the corners of fast-fast and slow-slow. These variations are not very important because by varying V_{ctrl} (*i.e.*, supply voltage) the frequency can be set to desirable value.

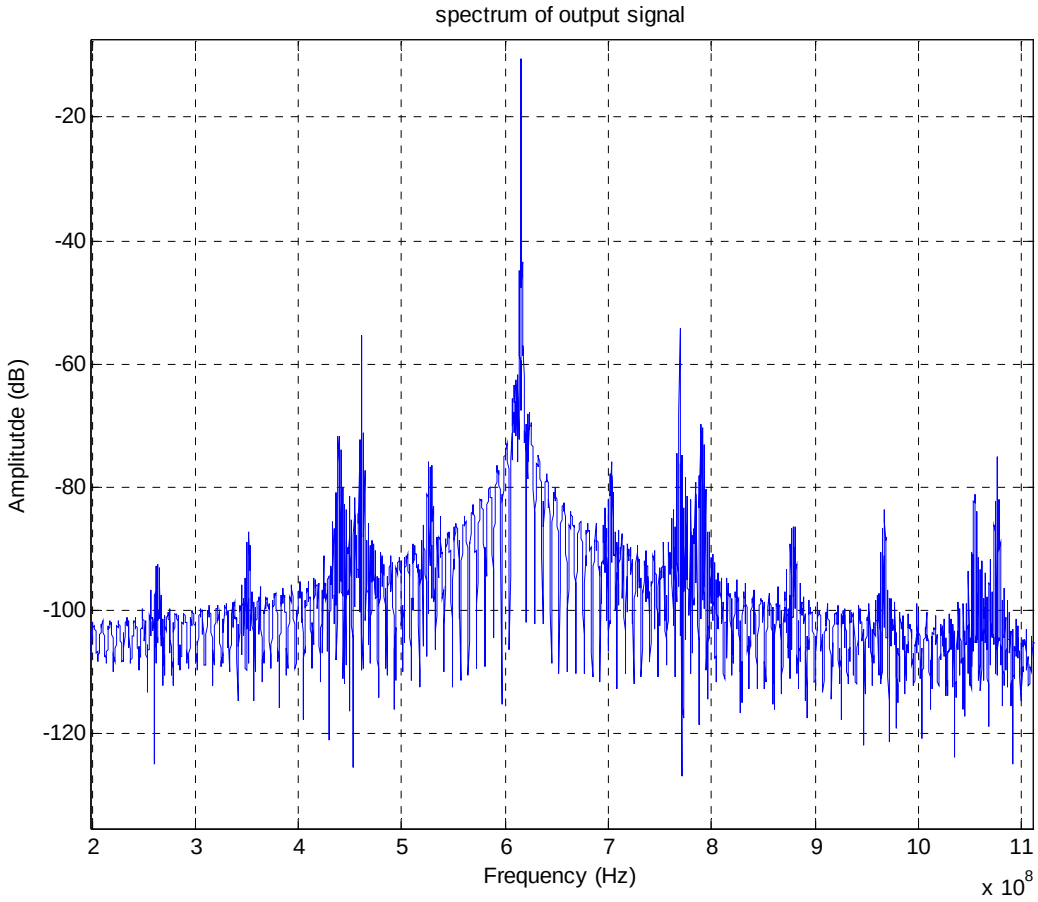

Figure 14. The spectrum of PLL1 output frequency.

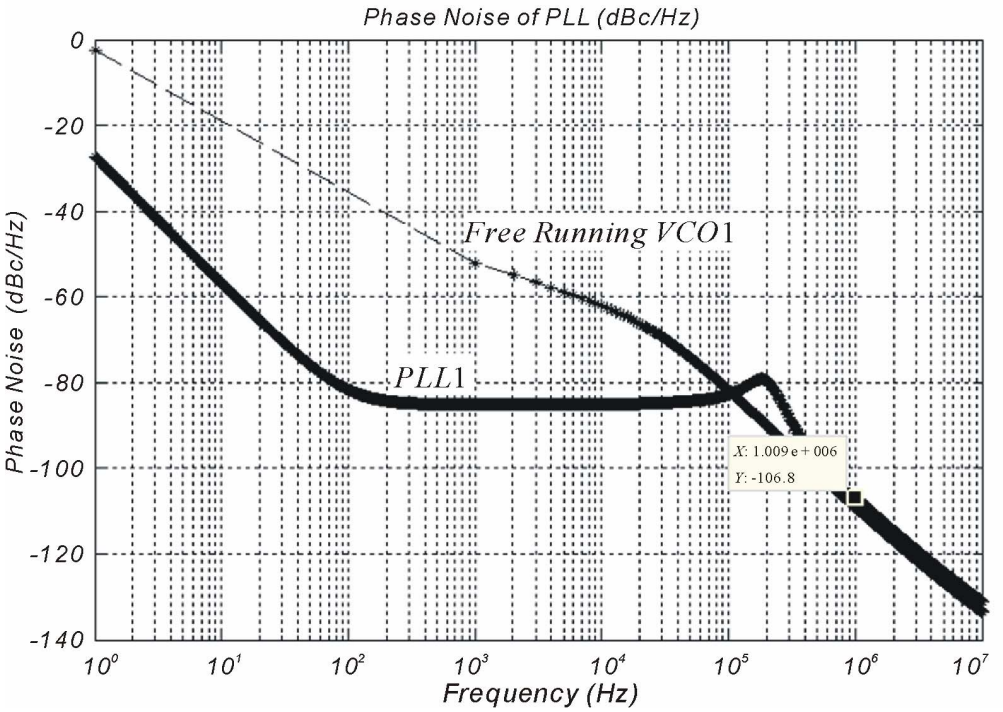

Figure 15. The phase noise of free running VCO1 and PLL1.

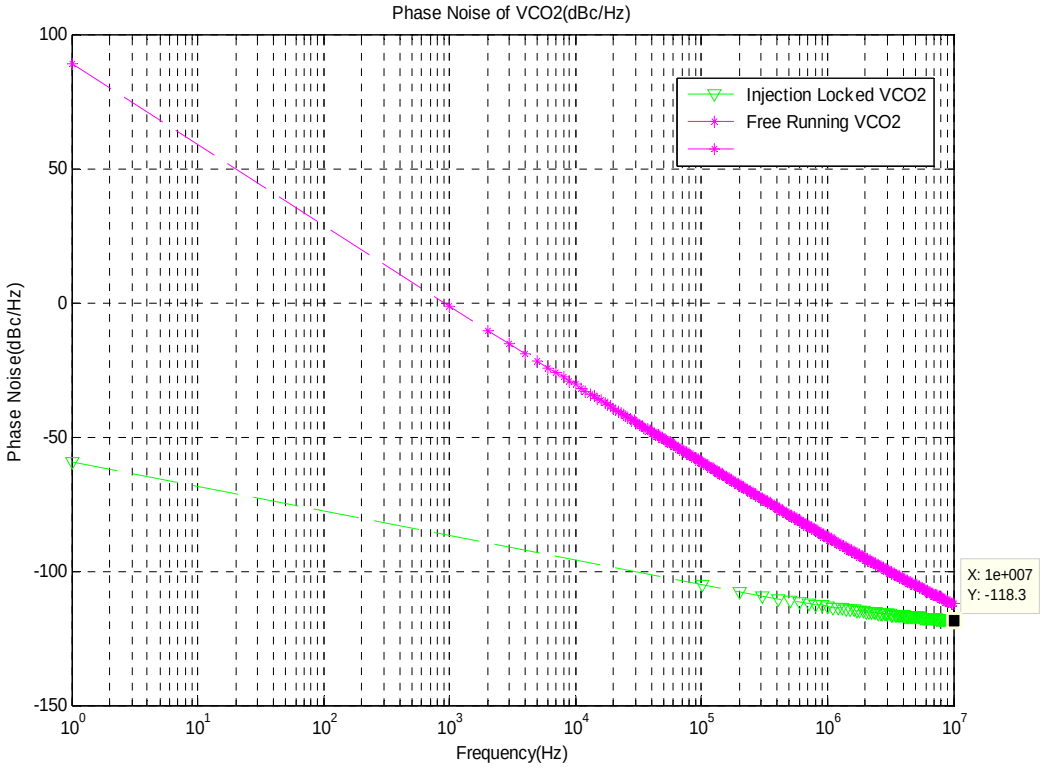

Figure 16. Phase noise characteristics of VCO2 with and without injection.

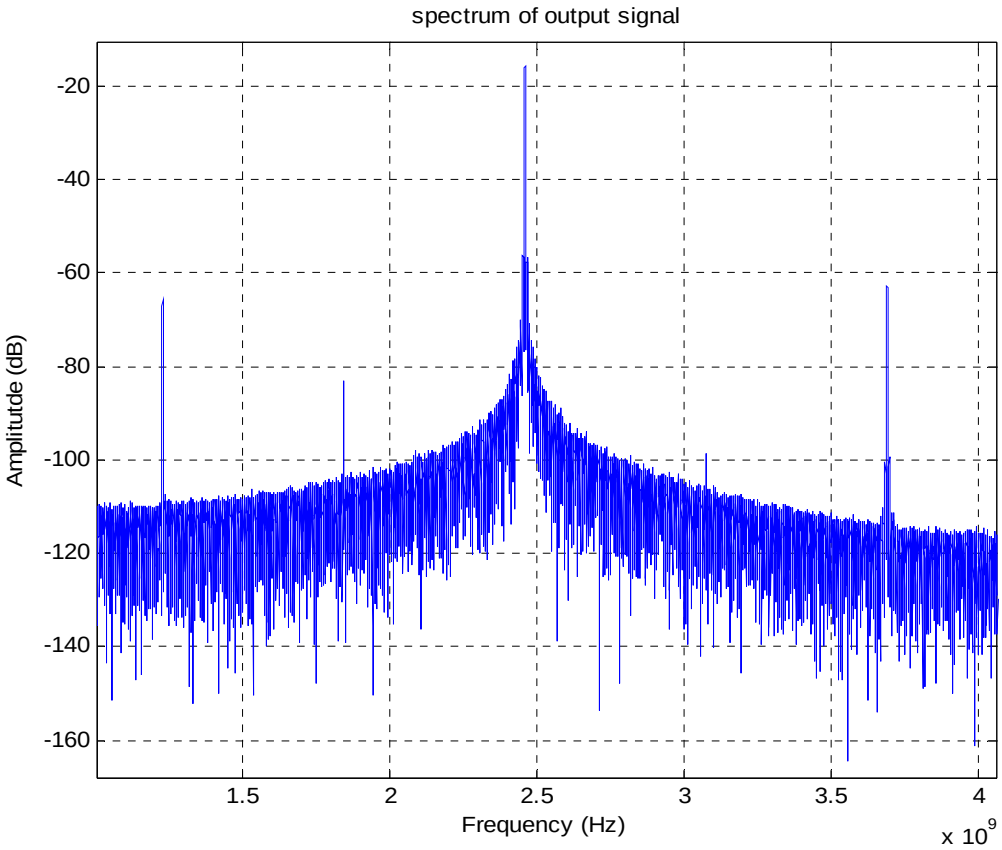

Figure 17. The output signal spectrum of PLL2 without injection locking.

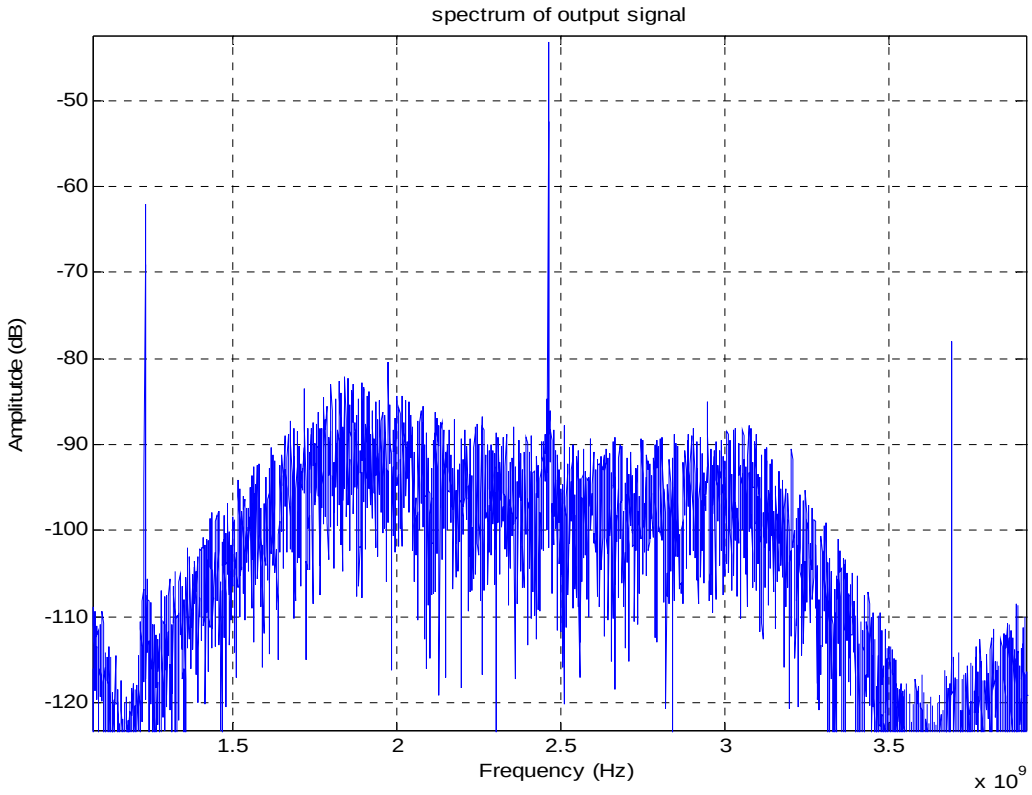

Figure 18. The output signal spectrum of PLL2 with injection locking.

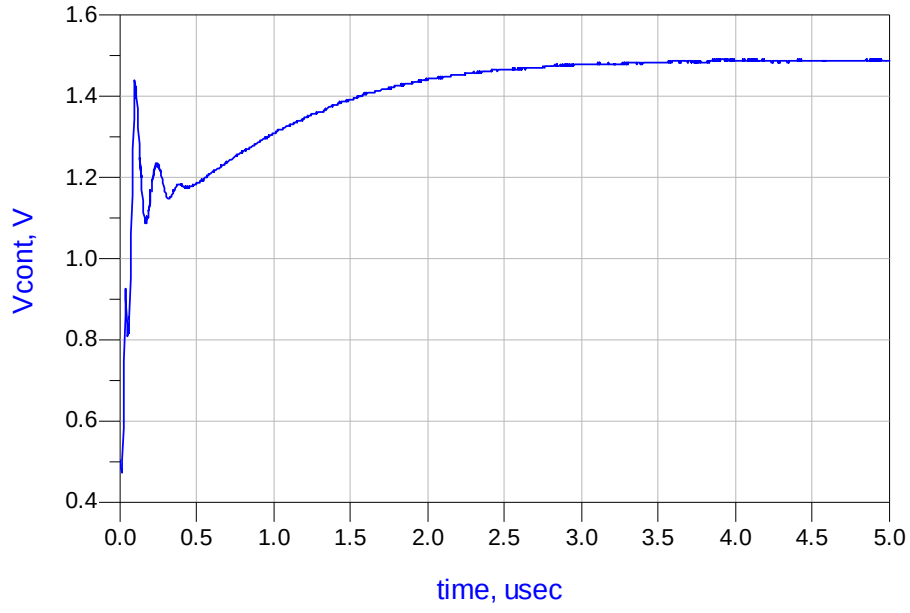

Figure 19. The V_{cont} (control voltage) signal for PLL2.

Figure 21 shows VCO2 behavior in the corners of technology. As mentioned before about VCO1, in this case the K_{VCO2} is almost without change in the technology corners and just the values of the frequency at fast-fast and slow-slow corners vary around 20%. This variation is compensable by a little change in the supply voltage value.

Table 1 demonstrates a performance summery and a comparison of the proposed frequency synthesizer with other ZigBee synthesizers. This frequency synthesizer has similar performance as other synthesizers, but its most important specification is using a ring oscillator that

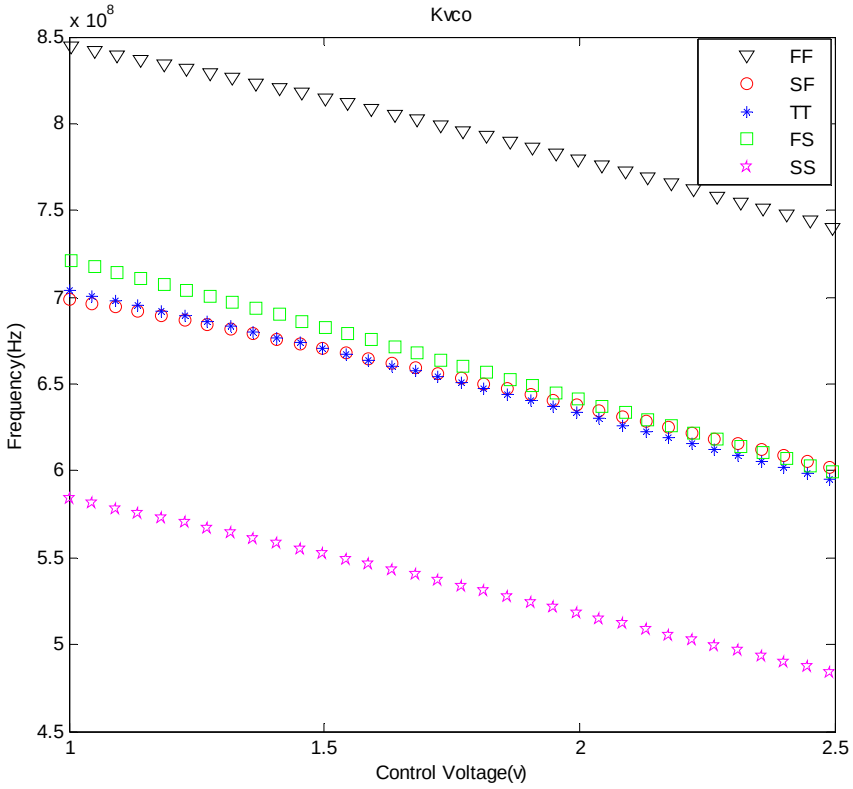

Figure 20. VCO1 behavior in the technology corners.

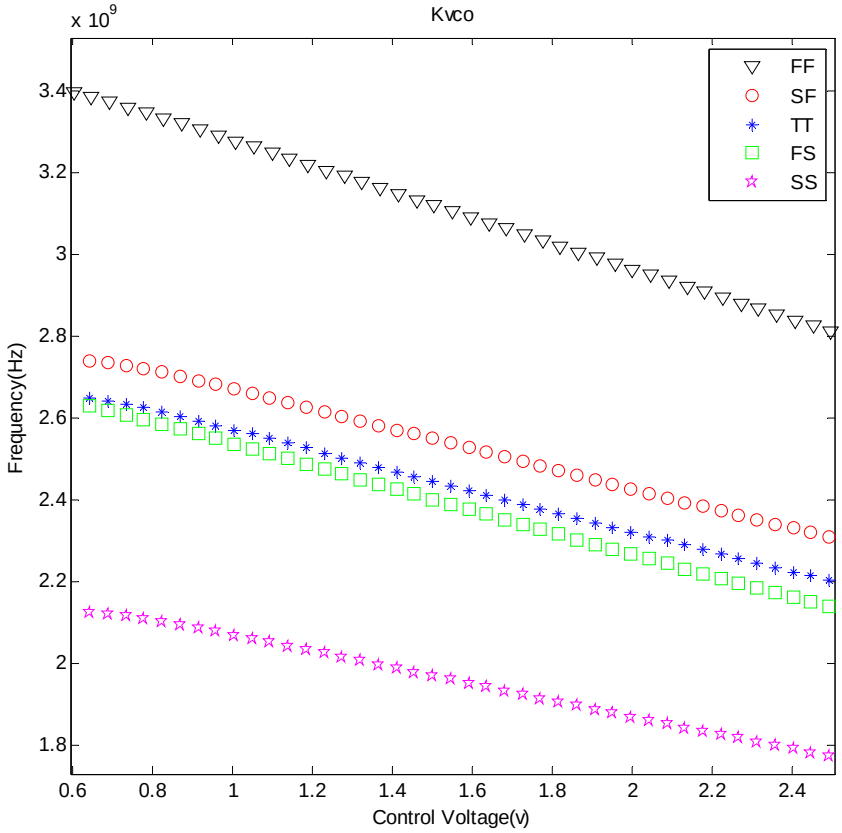

Figure 21. VCO2 behavior in the corners of technology.

Table 1. Performance summery and comparison of proposed frequency synthesizer with other ZigBee synthesizers.

	This work	[17]	[18]	[19]
Frequency (GHz)	2.4 - 2.48	2.4 - 2.48	5	2.4 - 2.48
Technology (μm)	0.18	0.18	0.18	0.18
Supply voltage (volts)	1.8	1.2	1.8	1.8
VCO type	Ring	LC	LC	LC
Settling time (μs)	28	500	-	25
Phase noise (dBc/Hz)	−116.3@ 3.5 MHz −118.3@ 10 MHz	−112 @1 MHz	−135 @3 MHz	−108.55 @1 MHz
Spur rejection (dB)	−54@5 MHz −62.4@10 MHz	−60 @5 MHz	−64 @2 MHz	−40.84 @5 MHz
Power consumption (mW)	7.5	3.5	19.8	7.95

has small dimension, is low cost, and is scaled with technology and has lower tolerance in fabrication, due to the lack of inductor.

8. Conclusion

In this paper we proposed a low power low phase noise ring-VCO based frequency synthesizer with injection locking technique for reducing phase noise. The output phase noise at 3.5 and 10 MHz offsets is −116 and −118 dBc/Hz, respectively and the complete frequency synthesizer has 7.5 mW power consumption. This circuit was simulated in ADS and its behavior was examined at technology corners. The simulations show that the circuit satisfies the ZigBee specifications.

9. Acknowledgements

The authors are willing to thank Research Institute of Information and Communications Technology for financial support of this research.

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