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A Modified PFD Based PLL with Frequency Dividers in 0.18-μm CMOS Technology

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Abstract

This paper introduces a modified design of CMOS dynamic Phase Frequency Detector (PFD). The proposed PFD circuit (PPFD) is designed, simulated and the results obtained are analyzed. In order to reduce dead zone, internal signal routing is used in the PPFD circuit. To extend, Phase Locked Loop (PLL) is designed and it is verified with two different Frequency Divider (FD) circuits. There is a decrease in area of the PPFD circuit with 16 transistors and dissipates power of 40.8 pW for 1.2 V power supply. The pre-layout simulation result shows that the PPFD circuit has an elimination of a dead zone. Further, it works with the high speed and reduced power operated in the reference frequency of 50 MHz and the feedback frequency up to 4 GHz.

Keywords

PFD, Dead Zone, VCO, Power, PLL

1. Introduction

A Phase Locked Loop is a closed loop feedback control system which is capable of generating a clock signal that has a fixed relationship to the reference clock signal. It causes a particular system to track with another one [1]. The PLL technique is active around for a long time. It has various applications include keeping power generators in phase, synchronizing to the pulse in a TV set [2], clock recovery from asynchronous data, demodulating an FM modulated signal and so on. Although there are legitimate applications, the primary use is frequency synthesis. The General block diagram of the PLL is illustrated in Figure 1. The primary function of the PLL is the VCO's output using externally present reference signal and output of the frequency divider. Both signals are in phase with each other. Further, the VCO's output indicates that the phase difference

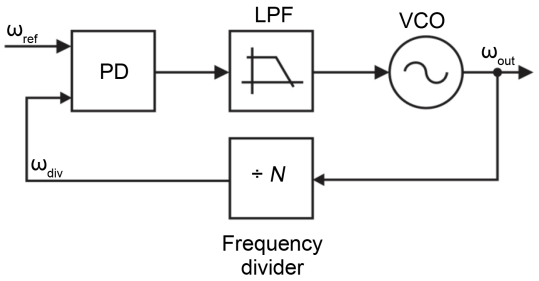


Figure 1. Block diagram of the PLL.

between both the signals is constant with respect to time.

An essential module in the PLL is the Phase Detector (PD) or PFD. It compares the reference frequency signal with the signal fed back from output of the VCO, and the difference signal is used as an input to both the loop filter and the VCO. In digital PLL (DPLL), the logical element is the PFD and the competence of the PFD produces a zero dead zone that leads to an attractive recording and locking performance in the PLL.

There are various modules in the charge pump (CP) based PLL. The first module in the PLL block is the PD circuit. It performs a phase comparison between reference and output signals. It operates at the edges of inputs and achieves the fast transition edges. The analog PD is implemented utilizing a simple mixer. It includes sinusoidal input and operates at a high frequency. The input amplitude affects the output, gain and dynamic behavior of the circuit. The simple PD circuit is the one which uses XOR gates, but the circuit consumes high power. The performance shows that the gain and the input amplitude are independent where as the output frequency is twice than the reference frequency. There are various limitations for XOR-based PD, which include slow frequency acquisition and the phase error is about 90 degrees. There are limitations in the frequency range while getting the output of the VCO, as the PD needs an input signal with high harmonics and the divider output locks to its reference harmonic signal.

Bang Bang PD has less sensitivity to data patterns and also it has high output jitter [3]. Alexander phase detector maintains the VCO frequency with no data transition and has high output jitter [4]. It retimes the data. Hogge PD has low output jitter, but the static phase error of clock is greater than the output of the flip-flop [5]. In JK Flip-flop PD, phase error lies between −180 and +180 degrees. It also has a larger phase tracking range. The PFD circuit overcomes all the disadvantages in the PD. It analyzes the phase and frequency of the reference and the output signal. Further, during the PLL frequency acquisition, the PFD input frequency, phase difference falls into a dead zone. The factors which cause false phase lock in PLL [6] [7] include delivery of incorrect phase information in the charge pump and shift in the positional direction. This will disturb the cycle slips and prolong the frequency pull-in time.

One of the ways to remove the dead zone in PLL system is by adding delay to the PFD reset path and then slowing down the reset path than the switching time of the CP current [8]. Next, stimulating UP and DOWN signals at the same time just for a short duration, it eventually turns on the CP's switches for charging/discharging the load capacitance [6] [7] [9]. The PLL operates at a high frequency, and then the circuit delivers

more power, and thereby it increases the area. In order to reduce dead zone, three modified circuits were designed, simulated and the results were observed based on pass transistor logic [10]. Now, a modified PFD is proposed to obtain null dead zone. In addition the circuit is designed in such a way it should operate at a high rate and also to obtain reduced power.

In general, there are three difficult issues in the PFD Design: 1) Blind Zone or Dead Zone. This issue arises when the PFD is unable to detect a slight phase difference in the inputs due to delay and circuit mismatching. 2) Jitter-Fluctuations of threshold crossings occur mainly due to the supply variations and substrate interference with the outputs. 3) Power consumption and Phase noise trade-off. Noise is an important and significant anxious parameter in the PFD performance. Phase noise performance is always inversely proportional to the power consumption of the device.

The Conventional PFD, which is shown in **Figure 2**, has the primary function as the NAND gate occupied by PFD, but the assignment state is different. Two D-Flip-flops (D = 1) with the clock signals are compared. Tristate Phase frequency detector finite state machine is shown in **Figure 3**.

The CP is nothing but the switching circuit used to generate dc voltages that are higher than the standard power supply. It is used to sink and source current into a loop filter based on the output of the phase frequency detector. The CP illustrated in **Figure 4** converts the up and down signal pulses from PFD into current pulses as there are capacitors in the loop filter. These current pulses change voltage drop on the loop filter impedance that is also the VCO control voltage. The CP design is mainly used to avoid the charge sharing effect. To minimize the effect caused by charge injection and clock

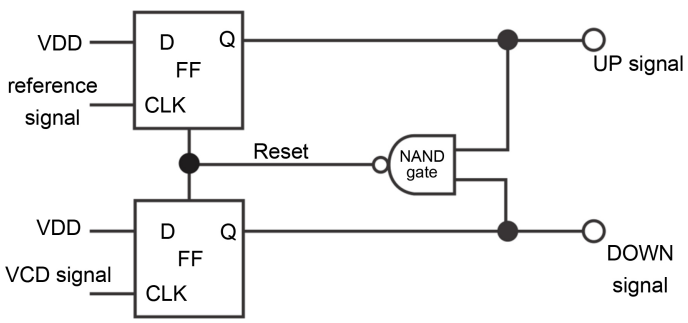


Figure 2. Conventional PFD.

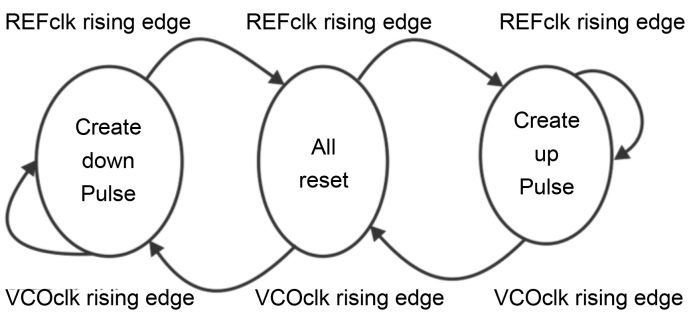


Figure 3. Tri state PFD finite state machine.

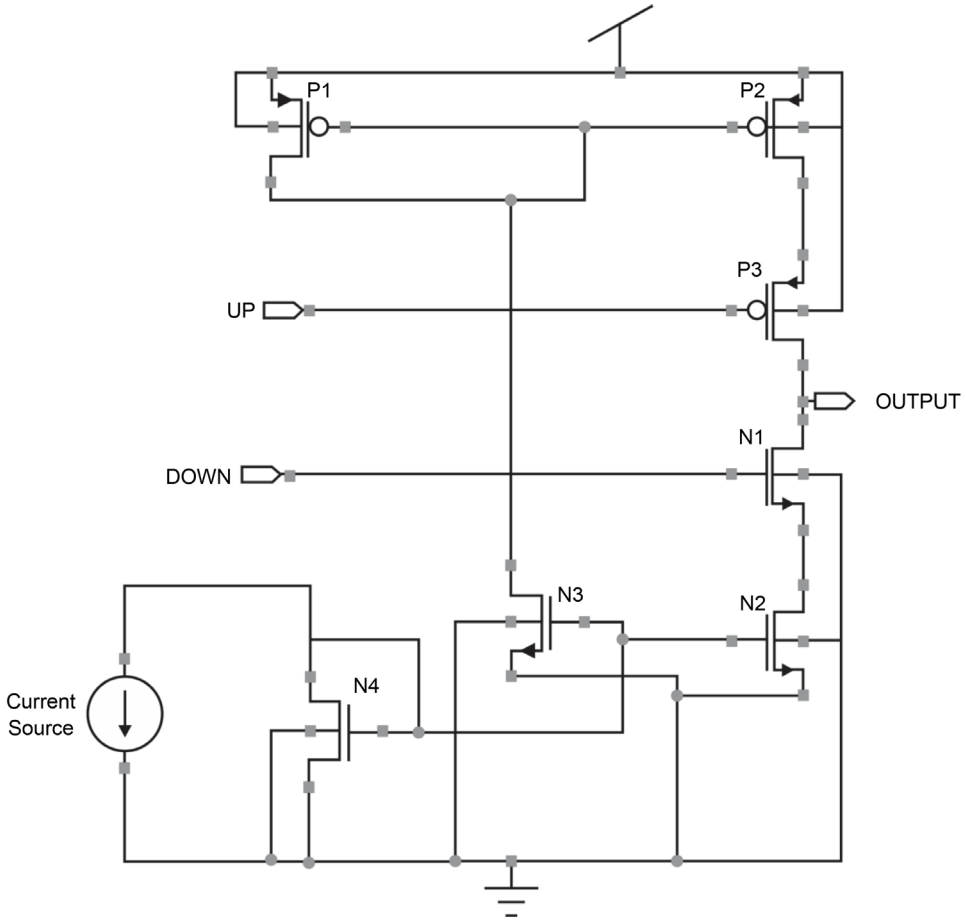


Figure 4. Charge pump circuit.

feed-through, the current values of up and down signals are matched. Further, it is designed in such a way that there is no time mismatch between up and down signals, and finally low power consumption is achieved [11].

A Loop-filter is nothing but the Low Pass Filter (LPF) integrates error current to generate VCO control voltage and suppresses the noise and unwanted phase detector outputs. The filter shown in **Figure 5** alters the ability of the loop to change frequencies instantly. If the filter has low cut off frequency, then the changes in tune voltage take place slowly. The VCO is unable to vary its frequency as soon, and this is due to the slow changes in the voltage level. Another important module in designing PLL is the VCO. A type of VCO called Ring Oscillator (RO) consists of some delay stages with a feedback system and to achieve the oscillation, the phase shift of 2π and unity voltage gain is required at the oscillating frequency.

Design of the Current starved VCO is similar to that of RO. From the schematic circuit of the VCO in **Figure 6**, the MOSFET M2 and M3 acts as an inverter, where M1 and M4 promote as current sources. The current sources M1 and M4 limit the current availability of the inverter M2 and M3. The MOSFET M5 and M6 illustrate each inverter/current source stage. The upper PMOS transistors are attached to the gate M6,

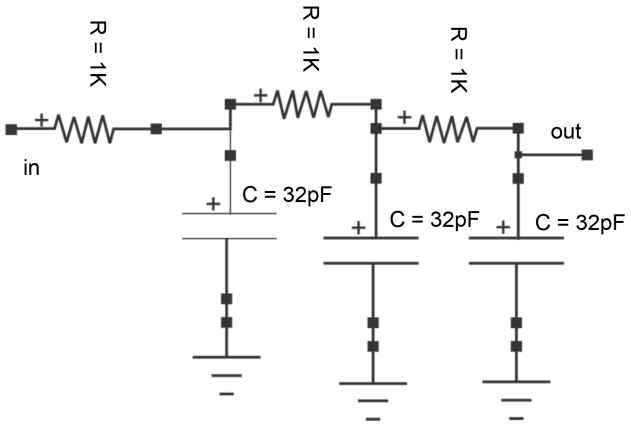


Figure 5. Low pass filter.

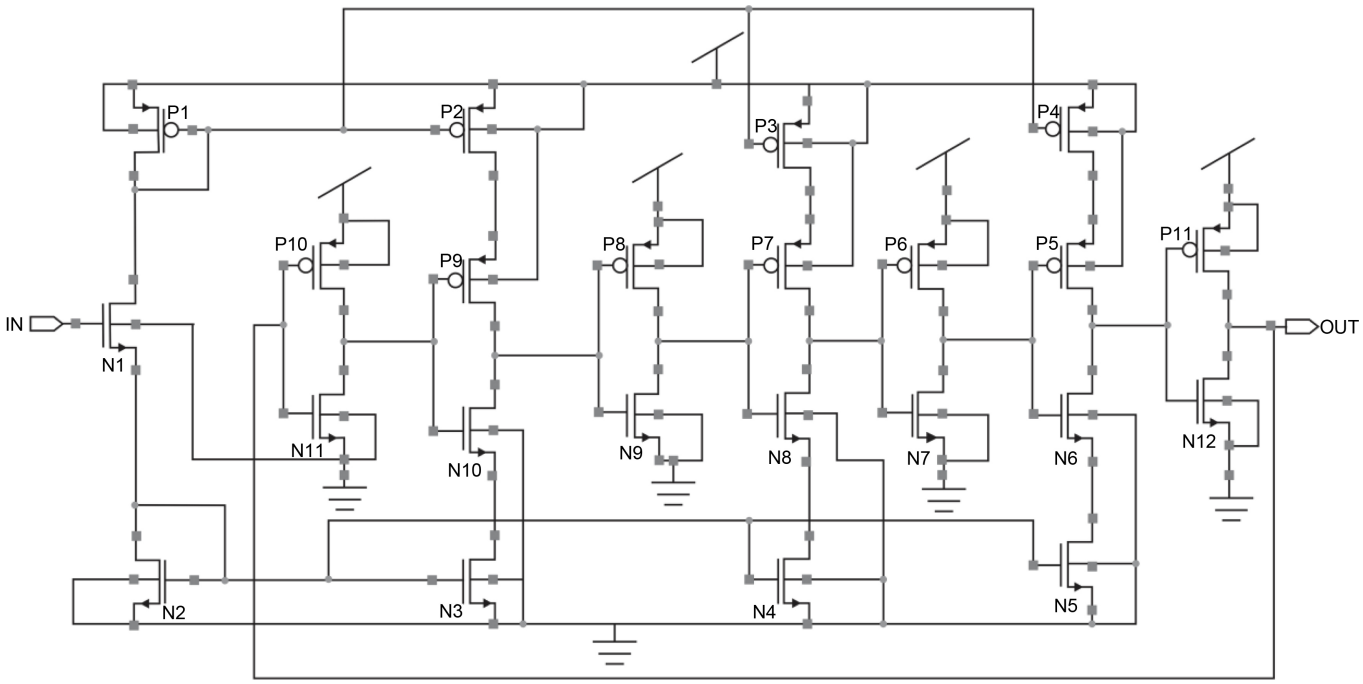


Figure 6. Current starved VCO.

and the source voltage is applied to the gates of all the lower NMOS transistors [12].

The FD by 2 is the first simple counter, which is easier to configure the memories with flip-flops. The input signal's frequency when fed to the FD circuit, it generates an output signal as half of the input frequency. Figure 7 illustrates the general structure of FD by 2.

The inverted output Q-bar is fed into the D input. It intends that at the rising edge of the clock signal output state flips. There are various types of FD. Figure 8 shows TSPC logic based FD by 2 [13]. This type of divider is suitable as compared to the static divider when it is applied at a high frequency. It has only nine transistors and the reduced number of interconnections. A clock signal is given as an input in order to achieve high-frequency operation. Since lower power consumption as the smaller area, FD is

used in the first stage of the PLL. Partition by 2/3 unit shown in Figure 9 consists of two toggle DFFs and additional logic gates. One way is used to reduce the delay and another is to reduce power consumption, where combining the logic gates and the FD 2/3 unit. The wideband 2/3 pre-scaler has the benefit of saving more than 50% of power during the divide-by-2 operation [14]. This paper reports a new proposal of a modified circuit for PFD in order to reduce the dead zone and combined with other modules to obtain PLL output. Further, the PLL characteristics are observed by adding two types of frequency dividers.

The remainder of the paper is organized as follows; Section 2 briefs the proposed circuit and the design of other modules followed by the simulation results and discussion in Section 3 and finally ended with Conclusion in Section 4.

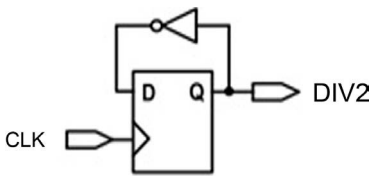


Figure 7. FD by 2 counter.

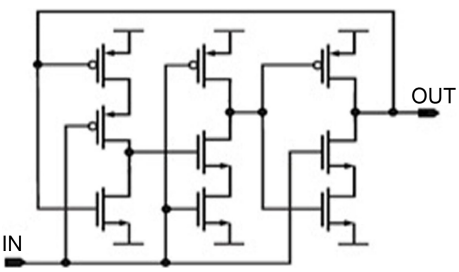


Figure 8. FD using TSPC logic.

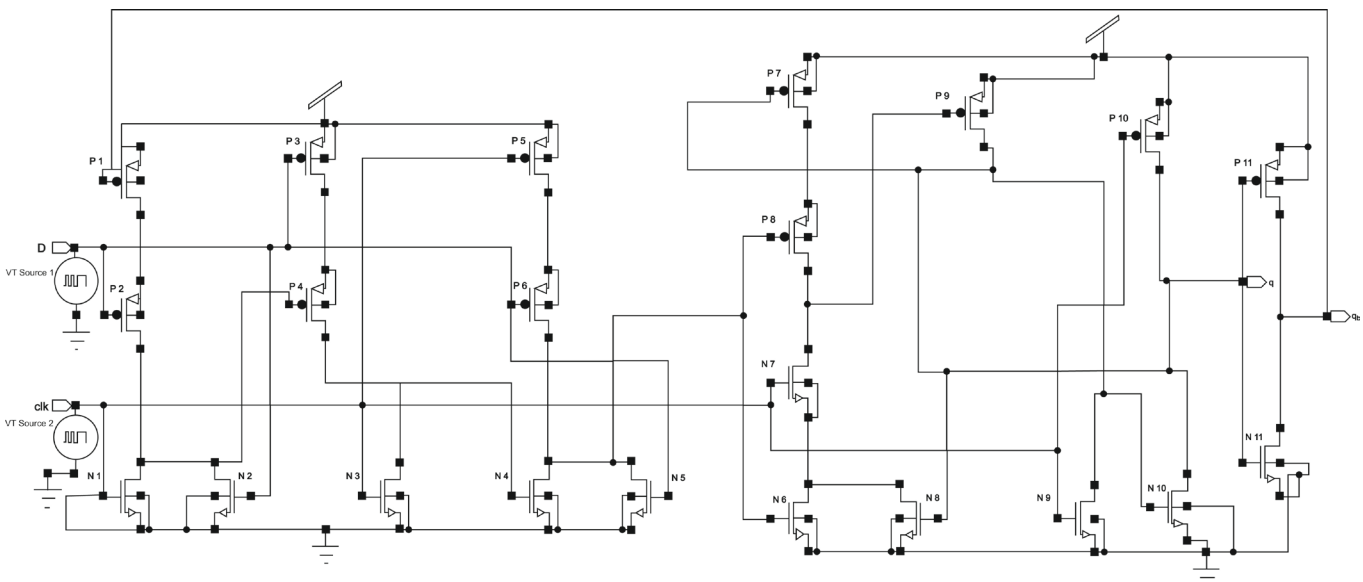


Figure 9. FD 2/3 unit.

2. Proposed PFD and the Other Modules Design

From the Literature survey [7], it is observed that the internal signal routing is required to reduce the dead zone in the PFD circuit. Based on that concept, the high-speed dynamic PFD is proposed (PPFD) and designed as shown in Figure 10. The reset path of PFD is eliminated by routing the PFD input connections to the flip-flop that is located next to it. The input of one flip-flop plays a role in developing reset signal for the other flip flop. Thereby the dead zone is eliminated and the power is decreased by reducing a transistor from the existing circuit of the High speed dynamic PFD [15]. Reducing the number of transistors, the area is decreased, and the speed of the circuit is increased. It overcomes the inaccuracy of the PFD output when the reference signal leads the VCO signal as the design is minimized. With the aid of smallest channel length in the circuit design, it confesses as an explicit device that is shrinking with the scaling of CMOS technology.

Figure 11 represents the top module of the PPFD. In PLL, the reference signal and the signal from the VCO are connected into the PPFD circuit. The result of the PPFD circuit is connected to the CP. The output of the CP is fed to the loop filter and finally it is applied to the VCO. The VCO frequency harmonizes to the in-out frequency of the loop. This process is a frequency pull in, and then the VCO phase is adjusted for the

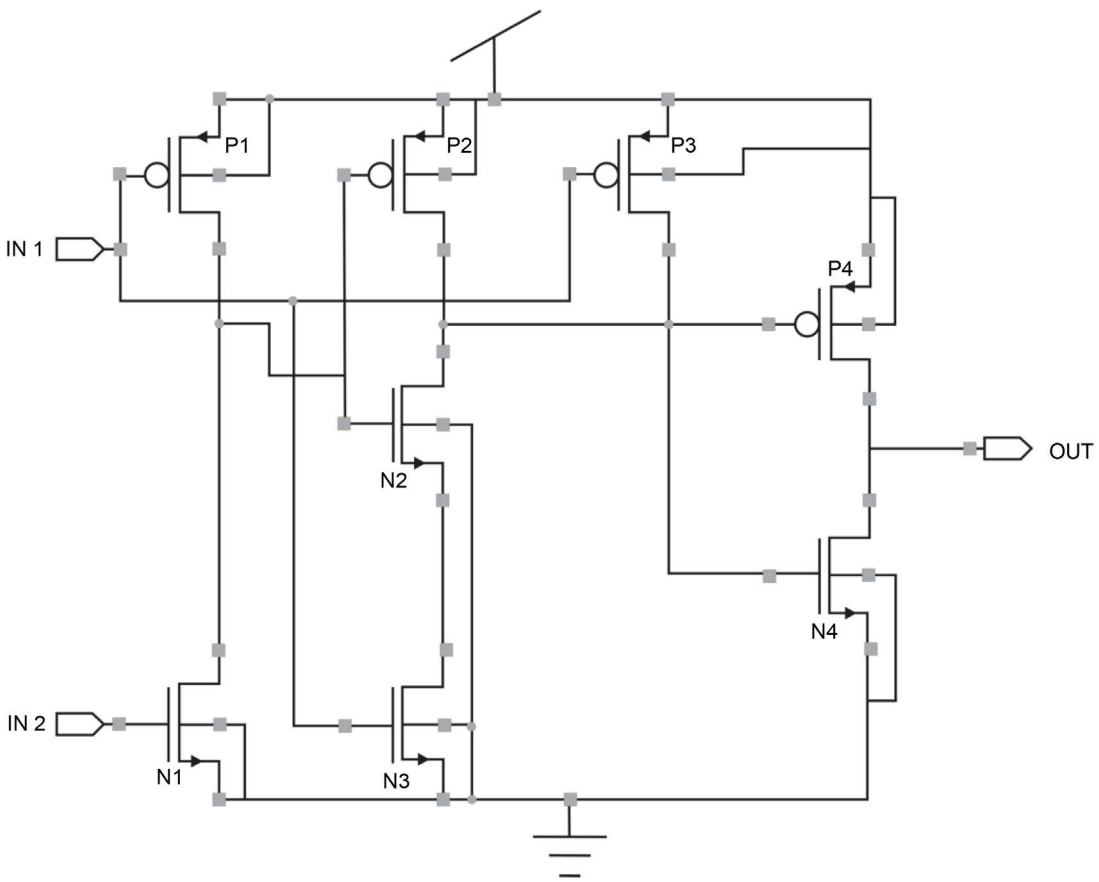


Figure 10. PPFD-dynamic schematic with inverter.

input phase. This operation is said to be a Phase lock-in. After addition, the PLL achieves the phase-locked condition, where PLL tracks the input. Under this condition, VCO frequency is equal to the input frequency. The overall PLL design is presented in Figure 12.

PLL operation is repeated with every external input pulse so that the feedback VCO and the external input clock are matched, the circuit then locks onto itself within a narrow frequency band. If the clock of entry varies slightly, the PLL frequency does not change. This narrow frequency band is the dead zone of the PPFD. Within this zone, the VCO signal and reference signal are so close in-phase that there are no correction pulses out of the PPFD circuit. Once the phase shifts out of this frequency band, the PPFD is correcting again. As the PLL design is functioning properly, it is extended further by connecting with Frequency divider (FD) blocks. The FD performs the frequency division by a factor of 2 which is illustrated in Figure 13 where it will divide the phase of the input signal by 2 as well. Figure 14 shows PLL with FD by 2/3 counter. The Frequency divider takes an input signal of a frequency and generates an output signal as 2/3 of the input frequency. The wideband single-phase clock 2/3 pre-scaler circuit consists of two D-flip-flops. In addition two NOR gates embedded in the Flip-flops. Here,

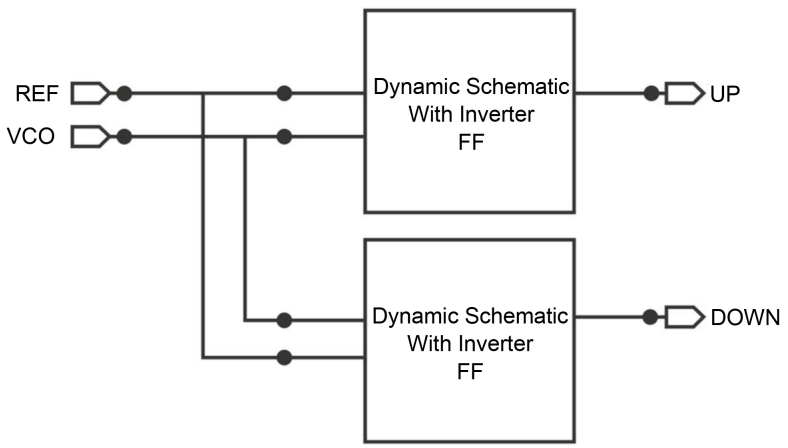


Figure 11. PPFD (top view).

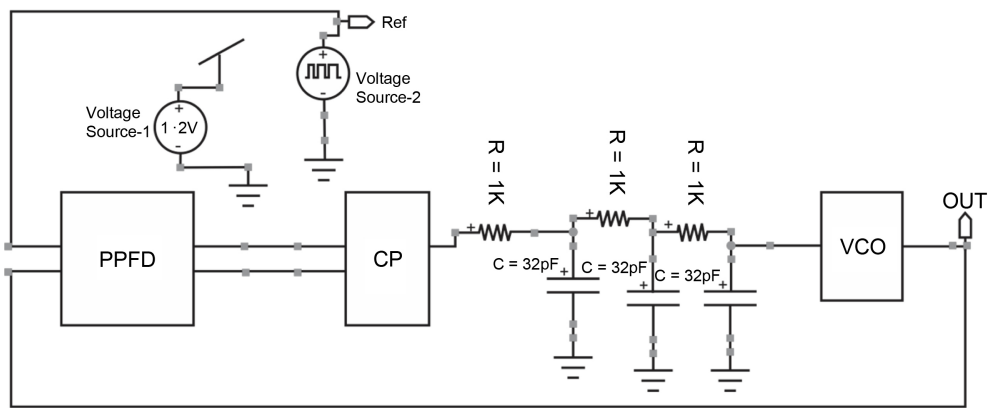


Figure 12. A PLL design.

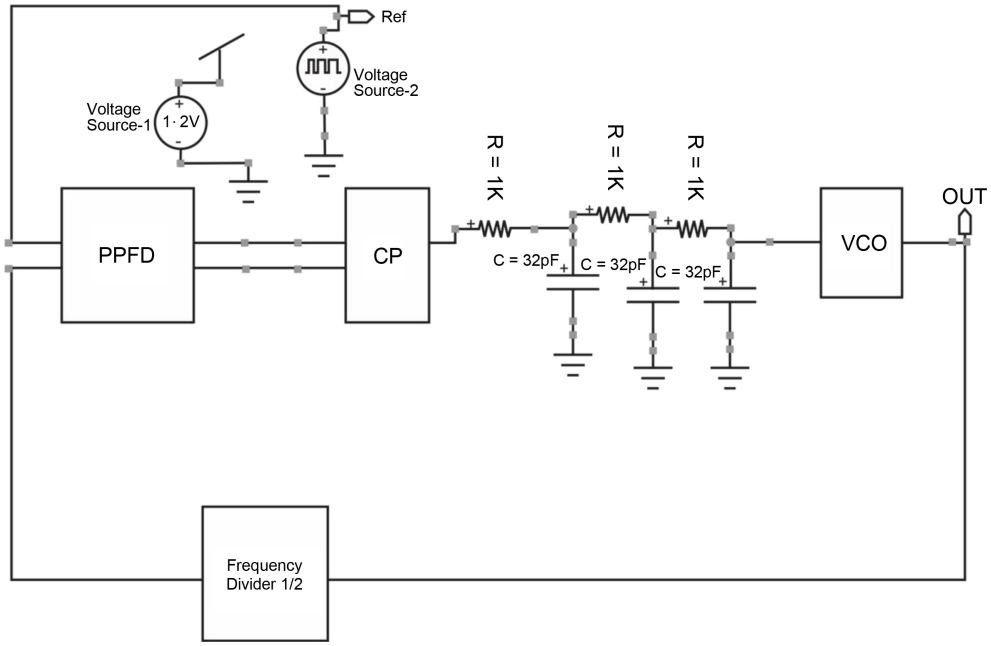


Figure 13. Phase locked loop with FD/2.

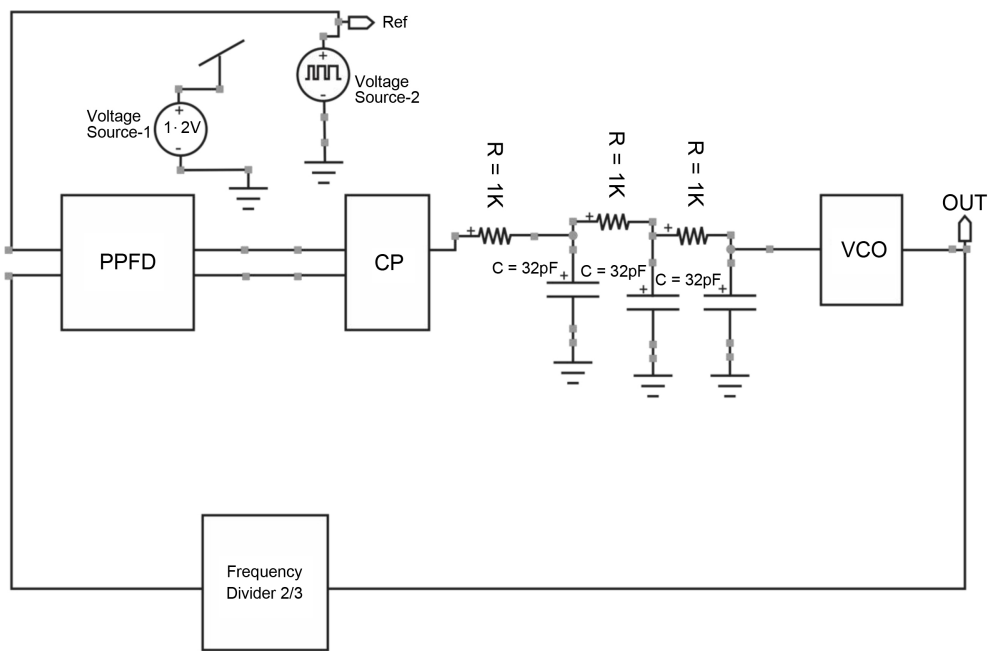


Figure 14. Phase locked loop with FD 2/3.

the transistors in DFF helps to eliminate the short-circuit power during the FD by-2 operation. Logic signal MC controls the switching of division ratios.

3. Results and Discussion

Each module in the PLL is designed and simulated (Pre-layout) using 0.18 μm CMOS process technology with the supply voltage of 1.8 V and 1.2 V in T spice Environment.

The width and the length of the transistors for both the NMOS and PMOS are fixed as 0.5 μm and 0.18 μm respectively. The simulated output waveform satisfies all the essential PFD criteria. The following simulated outputs show the PPFD's performance with the dead zone as a constraint. Figure 15(b) waveform indicates that the reference signal

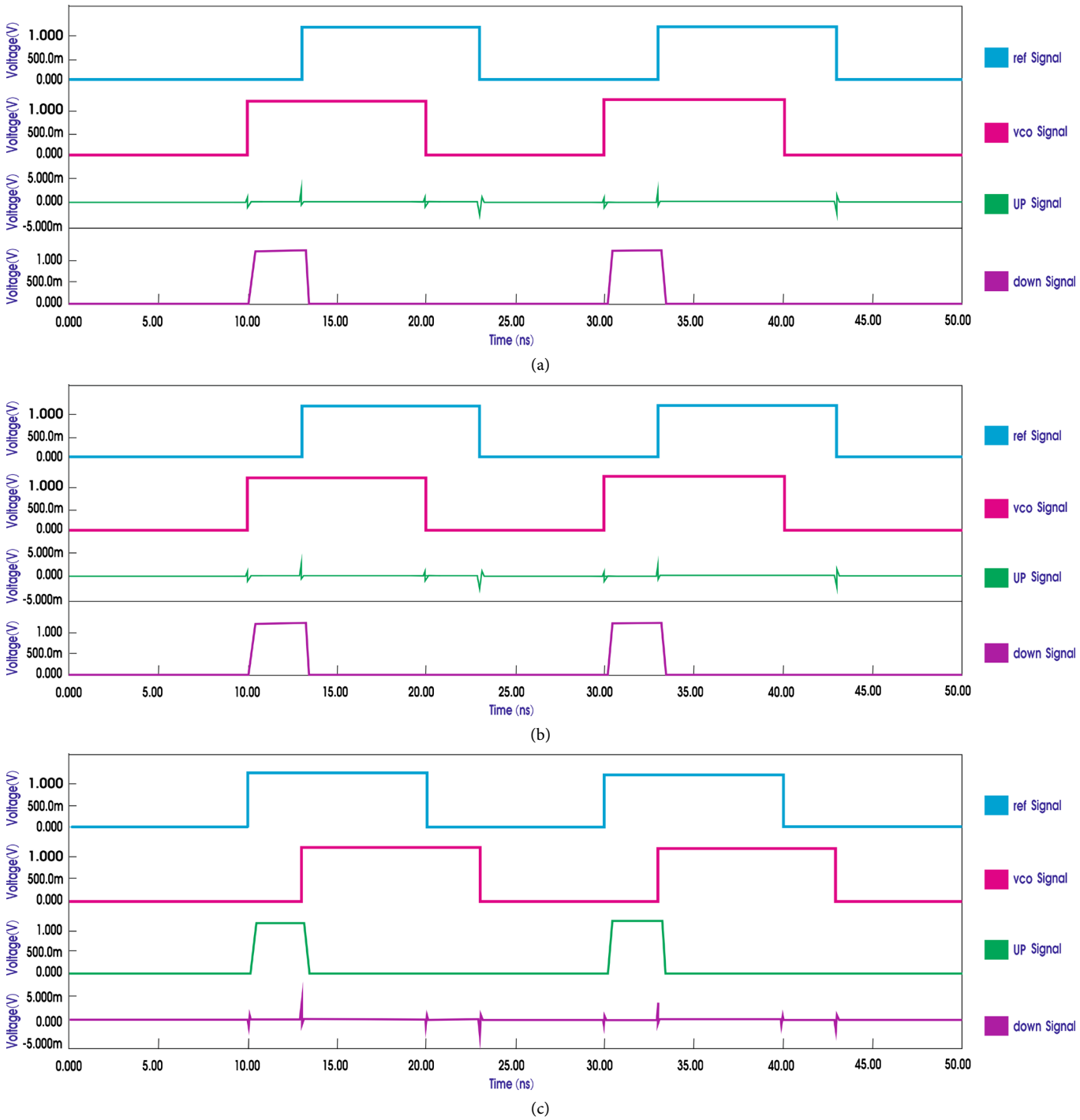


Figure 15. (a) PFD output waveforms when both reference and VCO signal are in phase. (b) PFD output waveforms when reference signal leads VCO signal by 3ns. (c) PFD output waveforms when reference signal lags VCO signal by 3ns.

leads the VCO signal by a delay of 3ns and the VCO signal leads the reference signal by a delay of 3ns as shown in Figure 15(c). Due to reset signal routing, PPFD is unable to detect the phase difference between two input signals even in phase with each other as illustrated in Figure 15(a).

In these graphs, a, b, c, d represent reference, VCO output, up and down signals (PFD Outputs) respectively. Here the input signals are varied as illustrated below and the dead zone is detected with the outputs obtained. It shows that the circuit produces output with zero dead zone. Since the circuit is verified with a low frequency operation, few small spikes for about peak to peak 5 mV is observed.

Decreasing the number of transistors in the reset path reduces the power from the existing one. Power dissipation of the PPFD for the supply voltage of 1.8 V is 85 pW and for 1.2 V is 40.8 pW. From the outputs it is observed that, the power supply dissipation is reduced with decrease in the supply voltage as expected due to the quadratic dependence on the supply voltage and also by the optimization of transistors both in width and gate length.

Figure 16 represents the operation of the PPFD with one of the output signals (up signal) for various input frequencies ranging from 1 GHz to 4 GHz. There is a consistency in the simulated output irrespective of the variation in the speed of the input frequencies. Modified PPFD circuit operates properly for low to high frequency ranges with both 1.8 V and 1.2 V power supply and it is proved that the higher sensitivity, better the detection when the frequency is varied. It also effectively senses both the input rising and falling edges. As power supply is lowered, low power dissipation is achieved. Figure 17(a) shows that the top level simulation of the PLL. It shows clearly the signals of up and down with free of dead zone. In order to justify the PLL output, overall module is extended with two FDs such as divide by 2 and divide 2 by 3. The outputs of the circuits are shown in Figure 17(b) and Figure 17(c) respectively. To extend, Monte Carlo simulations are performed for about ten sweep values for all the three PLL modules shown in Figures 18(a)-(c) respectively. The analysis is done based on variations of the threshold voltage in the 0.18 μm using T-Spice.

Table 1 illustrates the performance of the PPFD with preceding architectures. Even though most of the design has null dead zone, the number of transistors has been reduced.

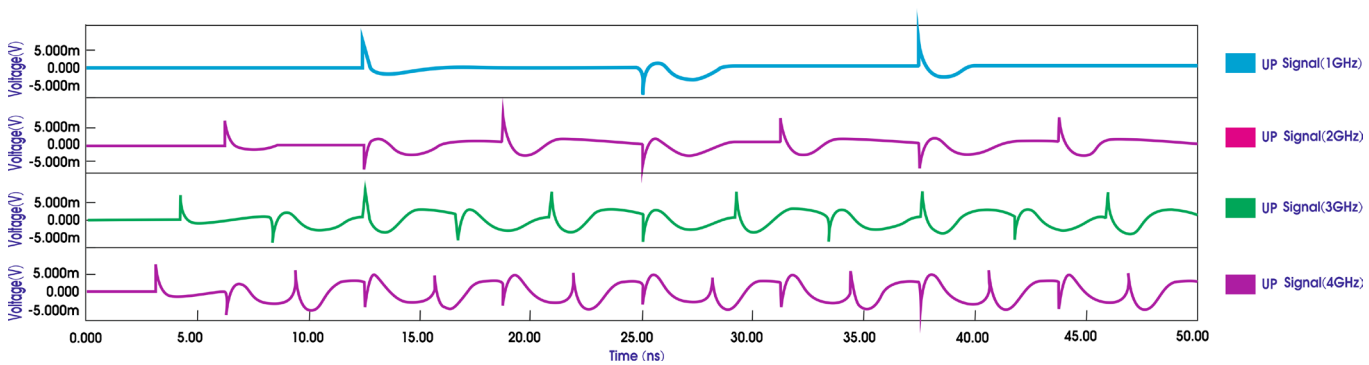


Figure 16. Waveform of up signal operated on matched inputs (locked) in the range of 1 GHz - 4 GHz.

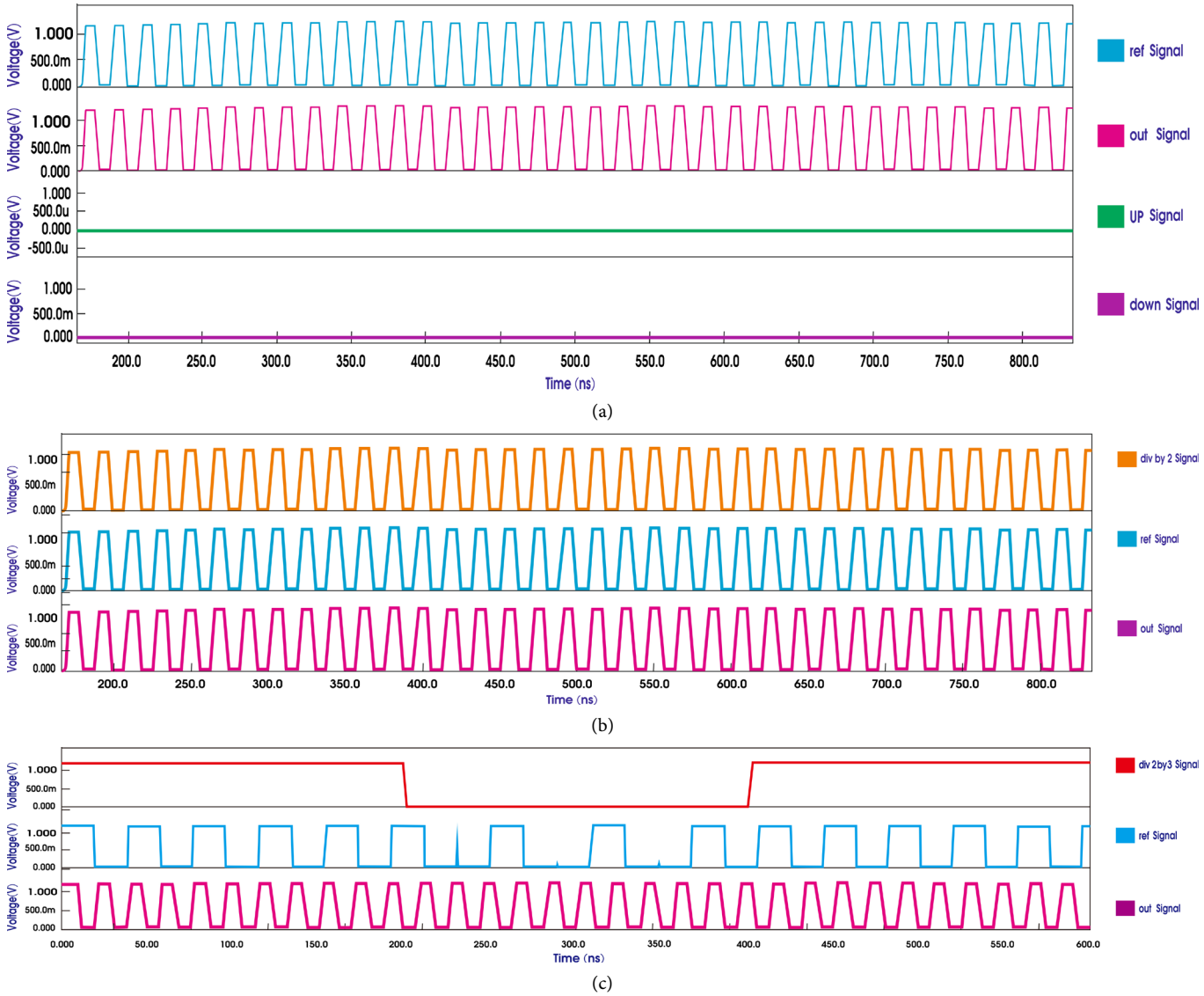
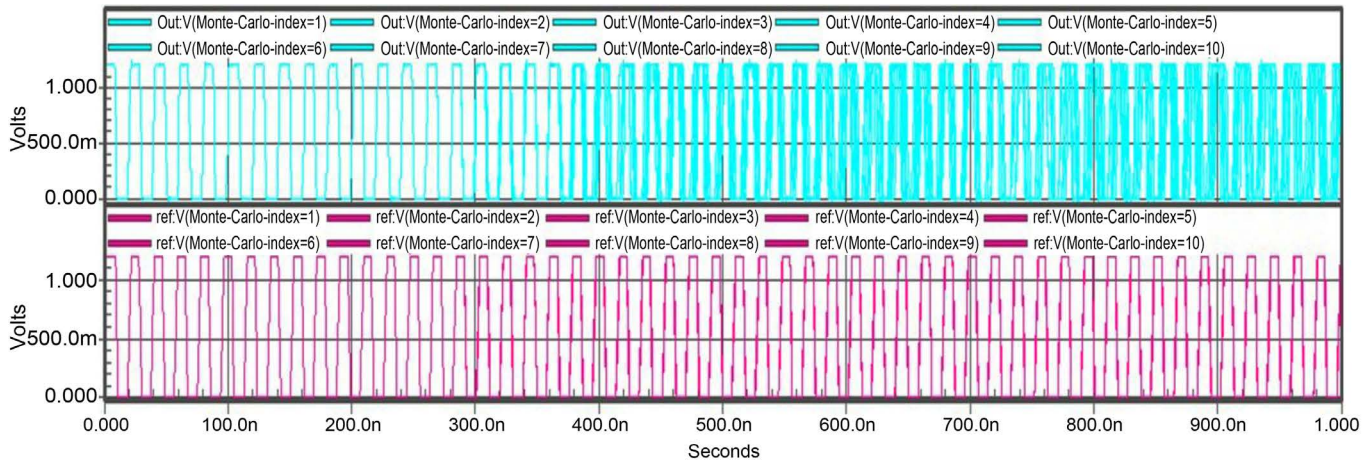


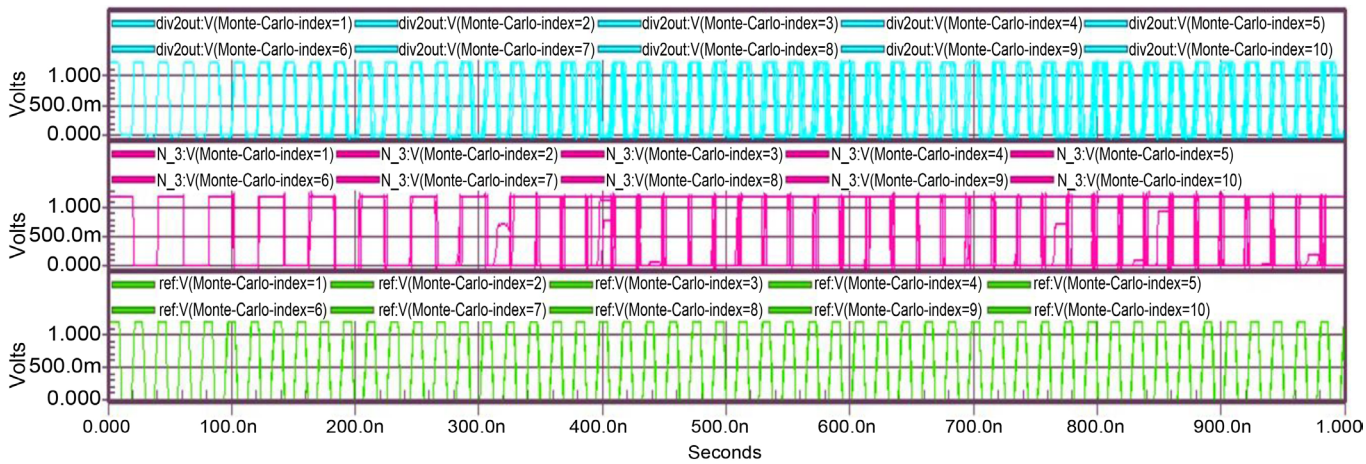
Figure 17. (a) Phase locked loop output with zero deadlock condition. (b) Phase locked loop output with divide by 2 counter. (c) Phase locked loop output with divide by 2/3 counter.

Fan *et al.* constructed PFD [16] with a power dissipation of 3 mW but uses digital circuitry for which the value is high. It even occupies large area on the chip as a result of the error amplifier circuitry. Hsu *et al.* designed PFD architectures [17] with smaller device sizes to reduce the power dissipation. Chen *et al.* designed PFD [18] with still lowering power dissipation by re-routing. Thakore *et al.* designed a PFD [19] that produces a power dissipation of 870 pW with 1.2 V power supply. Is mail *et al.* designed a PFD [20] with less number of transistor count, but it has limitation in detecting the input phase difference as the detection works on inputs negative edge of the reference signal. The proposed work gives a still lower power dissipation of 85 pW at 1.8 V and 40.8 pW at 1.2 V due to internal signal re-routing.

Table 2 shows the Power comparison between PLL and the FDs based PLL and it



(a)



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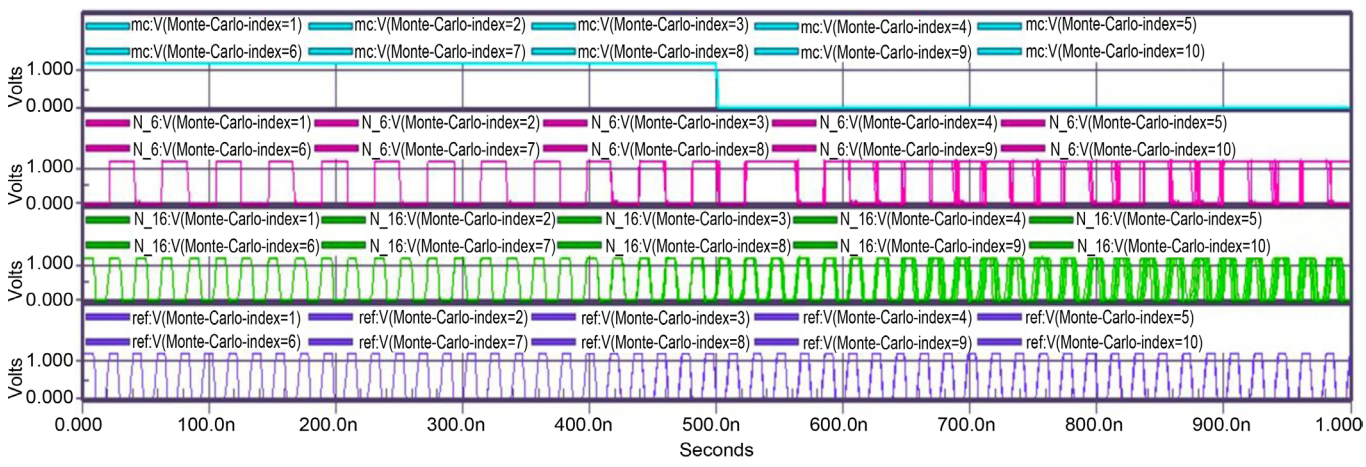


(c)

Figure 18. (a) Monte Carlo Simulation result of phase locked loop output. (b) Monte Carlo Simulation result of phase locked loop with divide by 2 counter output. (c) Monte Carlo Simulation result of phase locked loop with divide by 2/3 counter output.

infers that the FD 2 by 3 based PLL has lower power consumption due to reduction in switching nodes and optimization of transistor sizes compared to TSPC based FD/2.

Table 1. Comparison with previous work.

Reference Paper	CMOS Process	Power supply (V)	Total power dissipation (W)	Reference frequency (MHz)	Dead Zone (ps)	Transistor Count
[2]	0.18 µm	1.8	6.6 µ	50	0	12
[8]	0.18 µm	1.8	-	10 - 25	120	24
[9]	0.18 µm	1.8	870 p	50 - 100	2	18
[13]	0.18 µm	1.8	3 m	50	0	24
[15]	0.18 µm	1.8	1.56 m	50	-	22
[17]	0.18 µm	1.8	118 p	50	0	18
		1.2	59 p			
This work	0.18 µm	1.8	85 p	50 - 100	0	16
		1.2	40.8 p			

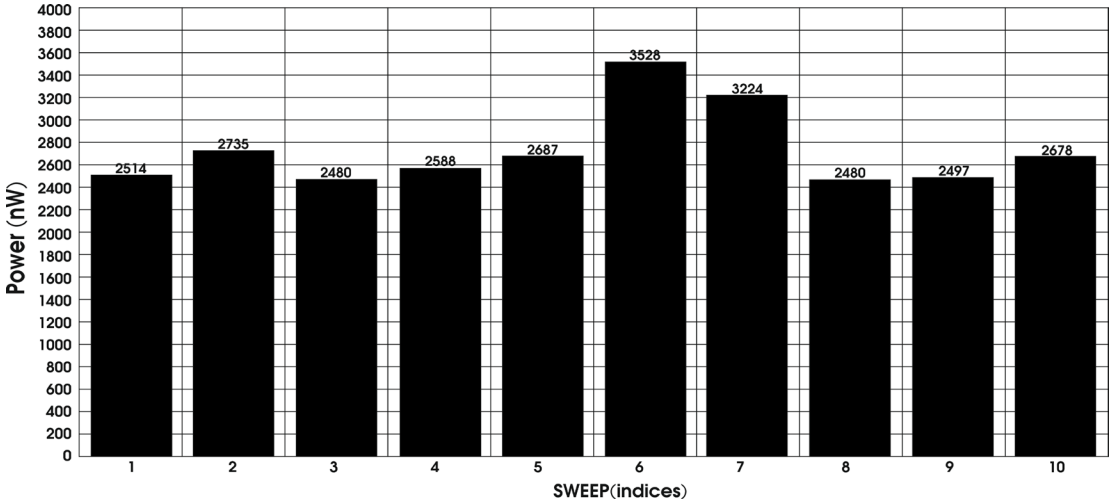
Table 2. Comparison of power.

Module	Average Power Consumed (µW)
PLL	2.48
PLL with divide by 2	1.53
PLL with divide by 2/3	0.65

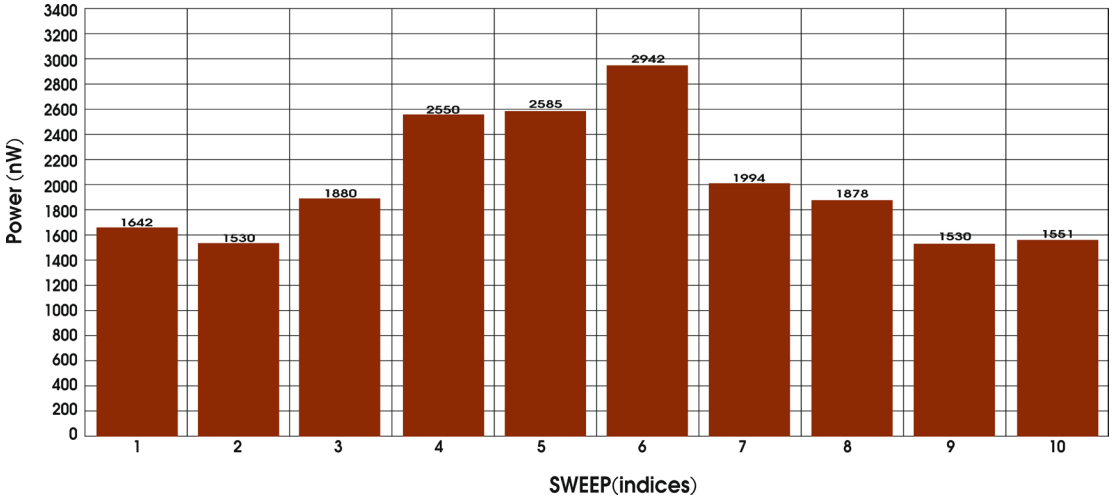
Further using the measurement results from Monte Carlo simulations, Power comparison is done for all the three PLL modules shown in Figures 19(a)-(c) respectively. Each graph represents the value of the power corresponding to its sweep value. Since number of transistors is reduced, area is minimised and such low power consumption is achieved.

4. Conclusion

In this work, a modified TSPC-logic based PFD circuit is designed with both the 1.8 V and 1.2 V power supply. The circuit maintains stability when operating at low as well as at high frequency variations. The dead zone is completely removed due to the internal signal routing in the proposed design. The obtained peak to peak spike values of 5 mV at low frequency are insignificant to the entire PLL performance. The total power dissipation is 85 pW for 1.8 V and 40.8 pW for 1.2 V. This is comparatively reduced with the existing circuits as the area is decreased to 16 MOS transistors. Overall, the PLL is configured in 0.18 µm CMOS technology with a T-spice environment and it is then connected with the frequency divider circuits (FD/2 & FD 2/3). From the comparisons, it shows that the low power consumed is about 0.65 µW for the PLL with FD2/3. In addition, Monte Carlo simulation is performed for the PLL circuits and the power values are analyzed. In order to extend the research work, Pass transistor logic based FDs can be used to reduce power. Therefore, the proposed circuit delivers the designers superior choice in establishing the high speed PLL devices.



(a)



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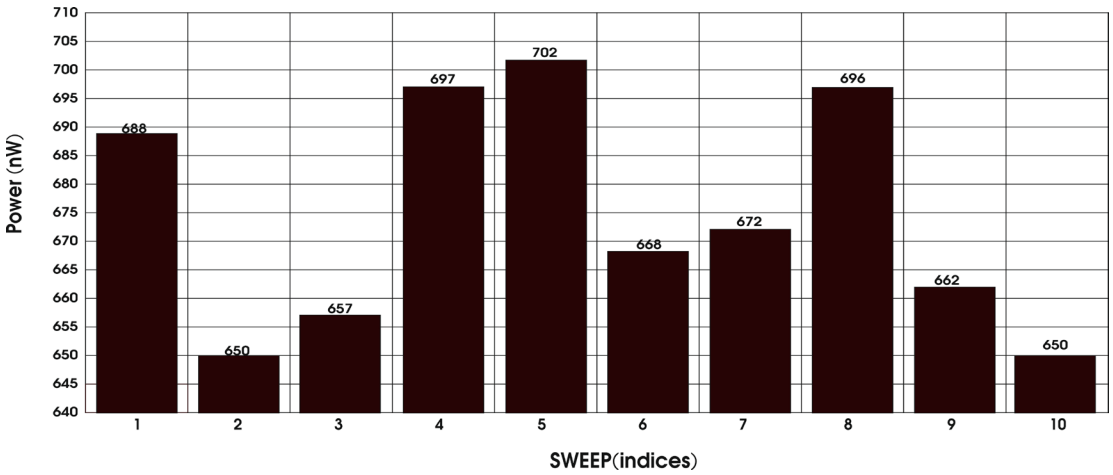

(c)

Figure 19. (a) Comparison of power in Monte Carlo Simulation result of the PLL. (b) Comparison of power in Monte Carlo Simulation result of the PLL with divide by 2. (c) Comparison of power in Monte Carlo Simulation result of the PLL with divide by 2/3.

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